UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Lab 2
Logic Gates

1 Motivation

In this lab you will get to build and test a simple combinational logic circuit using actual logic gates, and to measure the delay of various circuits. Additionally, this lab exercise will reorient you with respect to the lab instruments and give you experience using the logic analyzer feature of our oscilloscopes. The experience with the lab instruments, especially the logic analyzer, is critical for successful completion of the class project later in the semester.

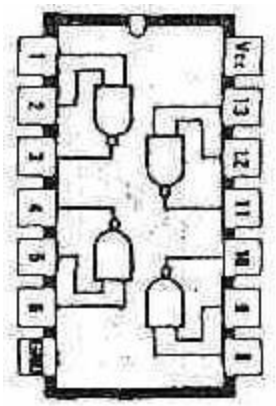
2 Introduction

In last week's lab we experimented with circuits using transistors as the basic building blocks, but in this week's lab we will use NAND gates. NAND gates are popular elements in CMOS logic circuits because they have a simple implementation; recall from last week that they can be built from only 4 transistors. Also, recall that the NAND gate is a "universal" logic element; any boolean expression or truth table can be implemented using only one or more NAND gates.

The NAND gates that we will be using come in plastic dual inline packages (DIPS) with 4 2-input gates per package. Their pinout is shown below:

4011
Quad 2-input NAND gates.

```
    +----------+            +-----------+      __
 1A |1  +--+ 14| VCC        | A | B |/Y |(/Y = AB)
 1B |2       13| 4B         |---+---+---|
/1Y |3       12| 4A         | 0 | 0 | 1 |
/2Y |4  4011 11| /4Y        | 0 | 1 | 1 |
 2A |5       10| /3Y        | 1 | 0 | 1 |
 2B |6        9| 3B         | 1 | 1 | 0 |
GND |7        8| 3A         +-----------+
    +----------+
```



The four NAND gates are labeled 1 though 4, the inputs, A and B, and the output Y. The "/" symbol is used to denote complement. This pinout guide should be interpreted looking down onto the package, with the pins pointing down. Orient the package so that the notch is at the top. **Vcc for this lab should be set to 5 volts**.

3 Prelab

1. Read and understand the entire lab handout.

2. Review the circuits involved in this lab. Make sure that you understand how they are supposed to work. Draw the circuits out.

3. Think through the experiments and what you will expect to see at each step.

4 Procedure

Part I: 2-input Decoder

A) Wire it up. Using several 4011 packages wire up a 2-input 4-output decoder circuit. Refer to the book or class notes for examples of decoder structures. Because we are using only NAND gates, it is simpler (and ok for this lab) to implement a decoder with complemented outputs.

B) Test it. The decoder can be tested exhaustively using two input signals driven from the waveform generator. One signal will be the "trigger output" and the other the "normal" signal output. As with the previous lab, offset one of these signals by a quarter cycle so as to have varying pairs of input values. Verify the function of your circuit by observing the outputs one at a time with the oscilloscope (while leaving the other oscilloscope channel on one of the inputs, as a reference).

C) After you have verified the correct function of your circuit use the logic analyzer function in the oscilloscope to capture the input waveforms and all four outputs, over all input combinations.

Part II: Gate Delay.

In this part we will build analytical models of gate delay based on measured values. For all of part II, configure the NAND gates as inverters by connecting the A input to Vcc. As in class, we will define the delay of a circuit as the time from the 50% point of the input waveform to the 50% point of the output waveform. For all of the delay measurements we will employ an extra gate to isolate the circuit under test from the signal generator. Do not connect the signal generator directly to the circuit under test; first send it through the extra gate.

A) Fanout test. Measure the delay though a gate with various numbers of other gates as fanout. Start with one gate connected to the output, then two, then three, and then four. From the measured delay, formulate an expression for the gate delay as a function of the number of fanout gates. Predict the delay for five fanout gates, and check it experimentally. Same for zero gates. Is all as expected?

B) Cascade test. Repeat the procedure from part A) but instead of connecting the extra gates in parallel (as fanout) connect them in cascade (a string). Measure the delay through this series of gates for one through four gates, then predict and verify five.

C) Ring oscillator. If you have time, wire a string of 5 gates in a loop (connect the output of the fifth back to the input of the first). Using the oscilloscope observe the waveform at any of the nodes along the string. What is its frequency? Is this what you expect?

5 Acknowledgement

Original lab by John Wawrzynek

6 Checkoff

Name: _____

Name: _____

Section: _____

Part I - Decoder

1.	Drawing of decoder circuit	TA:_____(10) _____(5)
2.	The logical analyzer display of your decoder test	TA:_____(20)_____(10)

Part II - Gate Delay

1.	Your drawings for the fanout and cascade test	TA:_____(10)_____(5)
2.	Your general formula for the delay and the data used to derive it	TA:_____(20)____(10)
3.	Delay measurement value for the cascade of five gates	TA:_____(20)____(10)
4.	The measured ring oscillator frequency	TA:_____(20)____(10)

Total

Total Score TA:_____