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Computer Science Division
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CS150
Fall 2001

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EECS 150 FINAL PROJECT REPORT

In this section, you will document what you have done in your project by writing a report. We know that you have spent countless hours on the project, so we will try to make the final project report as painless as possible. This document will describe the outline for the report that we want you to follow. The report should be at least 5 pages, with extra pages added for appendices. Your report should be written in one and a half spaced 12 point font.

We also want you to give us a soft copy of your Xilinx final project. To do this, create a new folder in the top directory and call it "FinalProject." Create an archive of your complete final project and place it in this directory. To create an archive, go to **File/Archive Project** in the Xilinx Project Manager. You only need to do this in one partner's directory, but make sure to note in the report the login name of the partner. (Do this in the last sentence of your introduction.)

The overall project report outline is as follows (max pages in parenthesis):

- I. Introduction (0.5 Page)
- II. Theory of Operation (1 Page)
- III. Control and Datapath Description (1.5 pages)
- IV. Design Decisions (2.5 pages)
- V. Evaluation (1.5 Page)
- VI. Conclusion (1 Page)
- VII. Appendix A: Control and Datapath Diagrams For Top Level and Each Subsystem (No page limit, but be reasonable)
- VIII. Appendix B: Project Checkpoint Check Off Sheets
- IX. Appendix C: Division of Work

I. Introduction

In this section, give us the "big picture" of your project. Describe your project in general terms. How does your project differ from other projects (i.e. what custom features did you add)? Did you make any changes to the specifications? Also, tell us the name of the directory that you placed your project schematics in.

II. Theory of Operation

Describe how your project works to someone who is not familiar with it. What do I need to do to get the project working? Which buttons correspond to play, pause, forward, etc...? What features are available? Include a diagram of the user interface with labels indicating features.

III. Control and Datapath Description

In this section, document your datapath in terms of their control signals and their timing behavior. Do this for the top level and then for each sub-system. The control and datapath descriptions should be high-level register transfer operations, not detailed control signals. How do different parts of your project interact with each other? Make sure to give a short description of your various controller's theory of operation. Did you use random logic, a RAM/ROM-based design, or some other strategy? Describe your approach for state assignment, if any. For RAM/ROM based designs, include a table showing the RAM/ROM contents and briefly describe what is happening in each RAM/ROM word. In addition, be sure to include in the appendix block diagrams with input/output signal names for each subsystem. The diagrams should be placed in Appendix A.1, Appendix A.2, Appendix A.3, and Appendix A.4, corresponding to each of the checkpoints.

IV. Design Decisions

Describe to us what decisions you made in designing your project and why you chose to implement the project the way you did. Ideally, you should first talk about overall design decisions, and then create sub-sections in which you write about your design decisions in each checkpoint. Put emphasis on the control and datapath design from section III, and talk about the implications of your decisions on timing, CLB count, etc...

V. Evaluation

In this section, we want you to tell us about the performance of your project. What is the critical path? Do all the buttons work? Do you hear static at the output? What is the range that you can adjust the volume and tone? If any part of your project does not work, explain what doesn't work and why in this section. In addition, note how many CLBs are used in your design. What percentage of the Xilinx component did your design consume?

VI. Conclusion

In this section, give a brief recap of your project. What did you learn from working on the project? What future work can be done? If you were able to do the project over again, what would be done differently? How might your project be improved upon? Also, this is where you can write about any problems that you had on the project, and how they were solved. Do you have any suggestions on how to improve the project

specification, checkpoints, and process for future CS150 classes? How many hours did you spend total on the project?

VII. Division of Work

In this section, we want to know what each individual's contribution was. This section should be organized by checkpoints. Within each checkpoint it should be broken down in to specific subsections. What role did each person play in each? Please attach this as Appendix C. You will also need to bring a copy of this to your final project debrief to give to the TA.