# Lab 6 – Nasty Realities

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## Outline

- Propagation Delays
- Capacitive Loading
- Transmission Lines
- Capacitive Coupling
- Why we care…
- Useful Tips: Approaching the Project
- Hidden Game



## Propagation Delays

- Observe propagation delays in this lab through transmission lines
- Propagation delays will exist in actual hardware.
- Build ring oscillator with the 74F04PC Chip. Observe results.




## Capacitive Loading

- Capacitive Loading affects propagation delays
- Fan-out loading increase propagation delay
- These issues are important in real world design.
- Simulate these loading by adding extra capacitors to ring oscillator

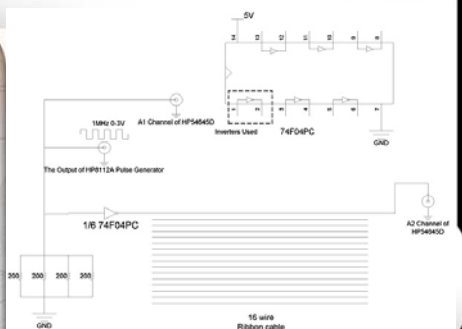


## Transmission Lines

- Models internal wires
- Lot of nasty realities occur in transmission lines
- “Parasitic” resistance, capacitance, and inductance occur in lines
- Observe transmission lines with a ribbon cable

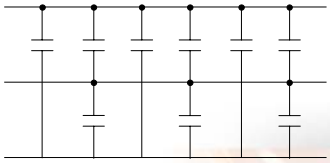


## Transmission Lines (cont’d)



## Capacitive Coupling

- Capacitance occurs between two wires (conductors)
- Closer the wire, the more the capacitive coupling



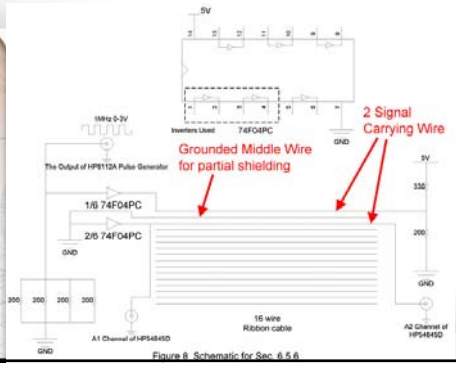


## Capacitive Coupling: Shielding

- Usually incasing the wire with some shield will reduce the capacitive coupling
- Partial shielding is usually enough
- Grounded wire between the two signal-carrying wires will shield



## Capacitive Coupling: Shielding






## Why we care…

- Propagation delays cannot be ignored when designing a real system
- Delays can affect timing signals – signals come in at wrong times
- Loading is important – will the gate driving the fan-out meet time specs – will it even switch?



## Why we care… (cont'd)

- Capacitive loading exists: deal with it
- Designing a digital system: power and timing are crucial
- In CS150, logic design is important – however designing a chip is more than just logic



## Why we care… (cont'd)

- Understand delays, capacitive loading, "parasitic" capacitance, etc.
- Helps minimize critical delay/path
- Faster logic – faster chip
- CS152, EE141 – these variables are important

## Approaching the Project

- Project starts after Lab 6
- Several checkpoints will be given
- Start early – do NOT wait for the last minute
- Allocate enough time for each checkpoint – never know the problems encountered with hardware



## Approaching the Project (cont'd)

- Design the data paths and high level schematic – understand it!
- Design the modules – logic inside them
- Design the FSMs – start with a diagram – really understand it!
- FSM – move to a transition table



## Approaching the Project (cont'd)

- FSM – develop Next State and Output logic
- FSM – begin to implement design
- Simulate all designs with software
- Debug designs on hardware with the board and oscilloscope
- NEVER be afraid to scrap your design and start over!



## Hidden Game