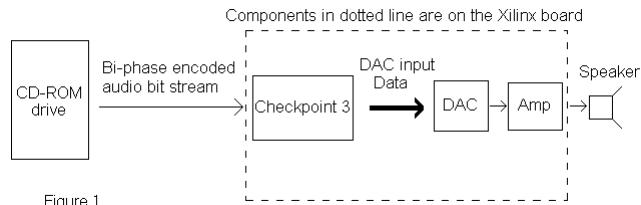


# Checkpoint 3

## Playing Music from your Xilinx Board

Converting a bi-phase encoded bit stream into a format that a dual channel digital to analog converter can recognize



## Inputs and Outputs

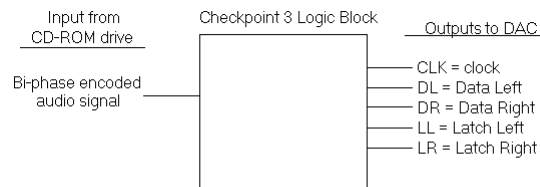


Figure 2 - Graphical representation of inputs and outputs

Note: Your logic block also uses an internal clock

# Bi-Phase Encoding

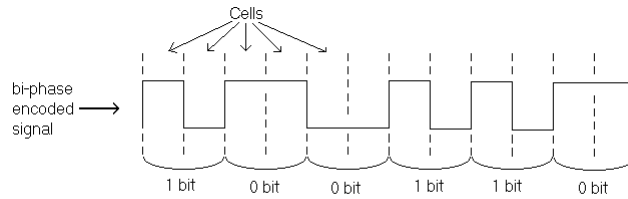


Figure 3

- Bi-phase encoded stream is composed of cells
- Every 2 cells represents 1 data bit

# Frames



Figure 6

- 16 bit audio samples sent in frames
- Assume garbage bits are sent between frames

# Preambles

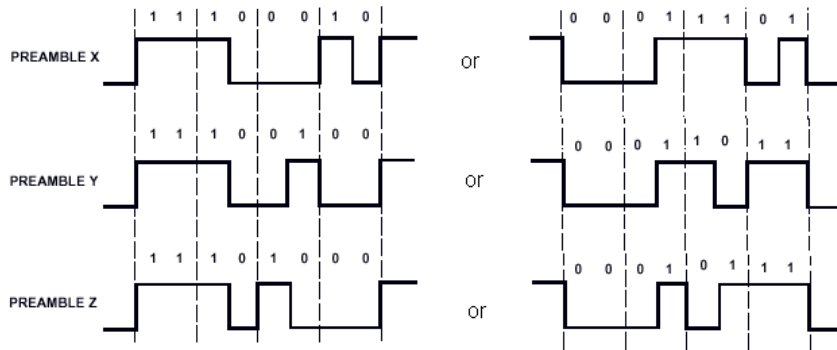


Figure 4

- 3 kinds of preambles
- Each has 8 cells
- Each has two representations

## What do the different preambles mean?

	BIPHASE PATTERNS	CHANNEL
X	11100010 OR 00011101	LEFT
Y	11100100 OR 00011011	RIGHT
Z	11101000 OR 00010111	LEFT

Figure 5

- The preamble tells you which channel the audio sample is for
- Left and right channels for stereo sound

# How to extract audio samples

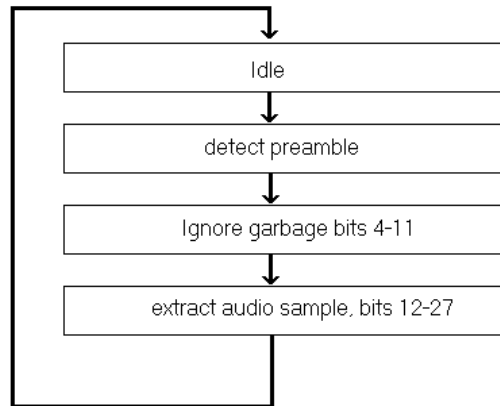


Figure 7

## A Minor Complication...

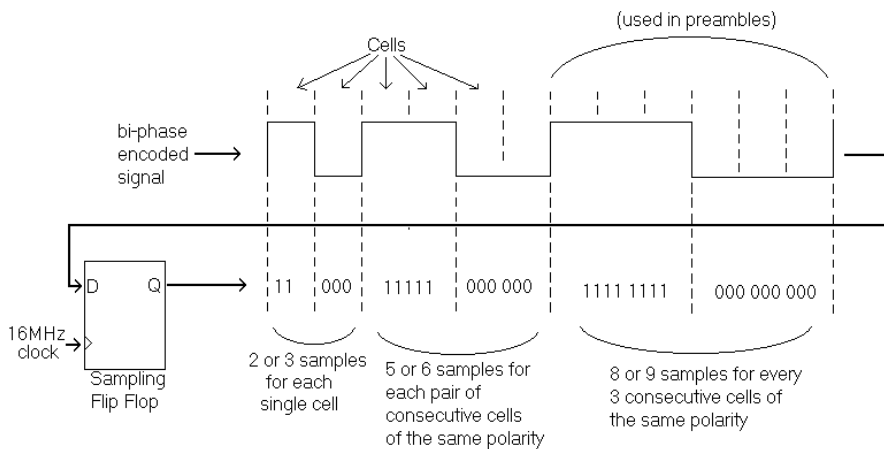


Figure 8

(Use an IFDI latch to sample the bi-phase encoded stream)

## How do we make a cell stream from a sampled bi-phase encoded stream?

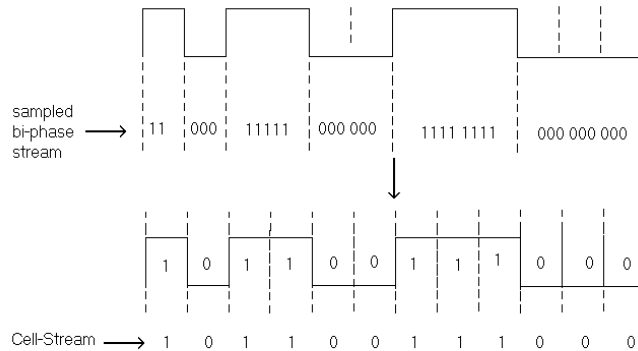


Figure 9

- 2-3 samples of the same polarity = 1 cell
- 4-5 samples of the same polarity = 2 cells
- 8-9 samples of the same polarity = 3 cells

## Outputting to the DAC

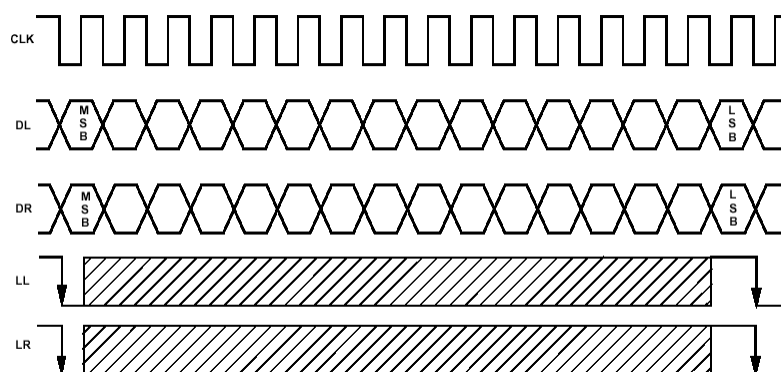


Figure 10

- Data is serially sent on the DL and DR data lines
- When the DAC it detects a falling edge on the LL or LR control lines, it latches onto the most recent 16 bits received

## How to create the LL and LR pulses

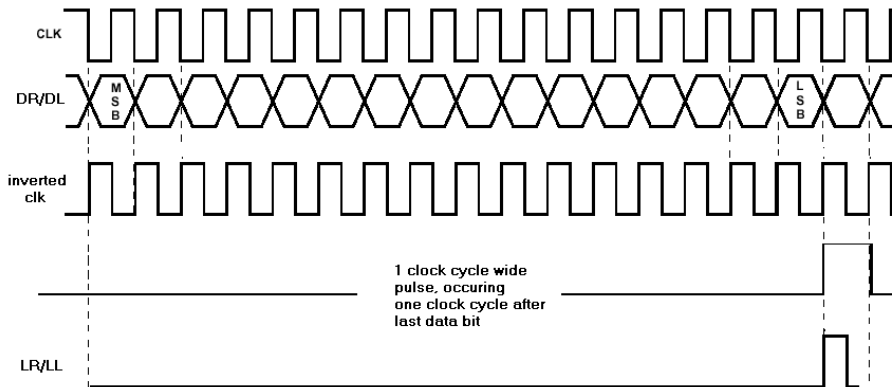


Figure 11

AND an inverted clock with a 1 clock cycle wide pulse occurring 1 clock cycle after the last data bit

## Wire wrapping

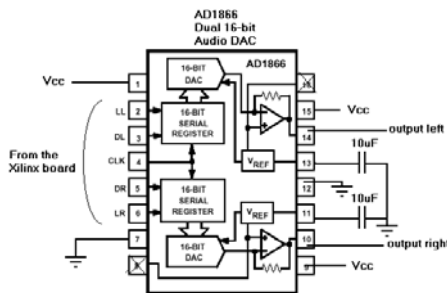


Figure 12

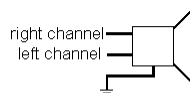


Figure 15- wire wrapping the audio jack

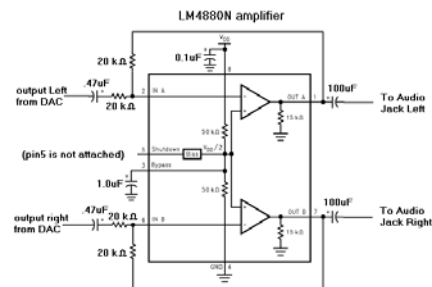


Figure 13

pin	function
61	DR
62	DL
68	LR
69	LL
78	CLK
79	input from CD-ROM

Figure 14 - Checkpoint 3 pinouts

Make sure you pick up 2 capacitor/resistor discrete packs

## Extra Credit

- Turned in 2 weeks early (11/2/01) = 120%
- Turned in 1 week early (11/9/01) = 110%
- Turned in on time (11/16/01) = 100%
- Turned in 1 week late (11/23/01) = 50%

## Tips

- Start early. Go for some extra credit, but don't burn yourself out. You should probably spend time in other classes too.
- Simulate all you logic using script files.
- Understand the checkpoint. Read this specification several times. If you need more clarification, please refer to the data sheets or ask me questions.
- **USE SCRIPT FILES!!!!!!**