Lab 3 Finite State Machine On Xilinx

Jimmy Su

Overview

- Schematics capture and simulation(lab 2)
- Add IO interface components
- Map netlists to implementation
- Download circuits to Xilinx board
- Debugging

Things to do before lab

- Have a working version of lab 2
- Finish the prelab questions for lab 3

We will use Xilinx 4010 chip

- Lab 2 was created under Xilinx 4005 chip model
- You need to create a new project under Xilinx 4010 model
- Then you need to reload your schematics from lab 2 to the new project

Xilinx Interface

- Interface components

IPAD OPAD

BUFG OBUF

IBUF

- Debounce circuit ensures ENTER and RESET go to high for exactly one clock cycle

Debounce Circuit

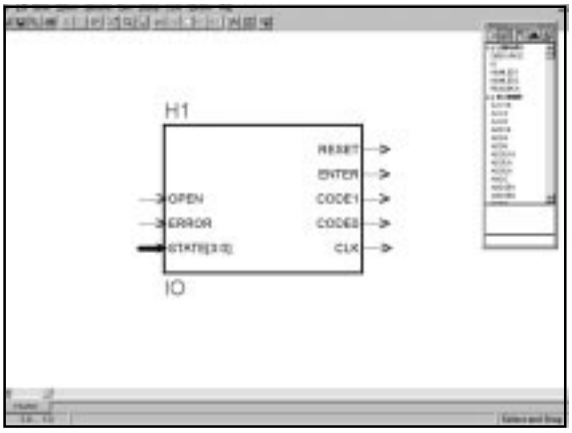
- After pressing a mechanical switch once, without debouncing the on-off connection might "make or break" several times before settling into a given position.

  Example:

  After the user entered the first combination, she pressed enter. The enter signal should go from 0 to 1. Without debouncing, the enter signal might have several transitions from 0 to 1. Debounce circuit ensures the enter signal stays high for exactly one cycle.
- Page 317 of text provides more information on debounce circuit.

We have done the interface for you

- You do not need to draw your own interface components on your schematic
- You need to add the library under u:\cs150\ to your project
- Name of library is “Library”
- We provide a macro called IO which contains all the interface components you need for this lab



Problems you might run into

- When you try to add the library to your project, you get access problems.
- This happened last semester when too many people tried to access the library.
- Alternative solution: Save your own copy of the library.

Implementation

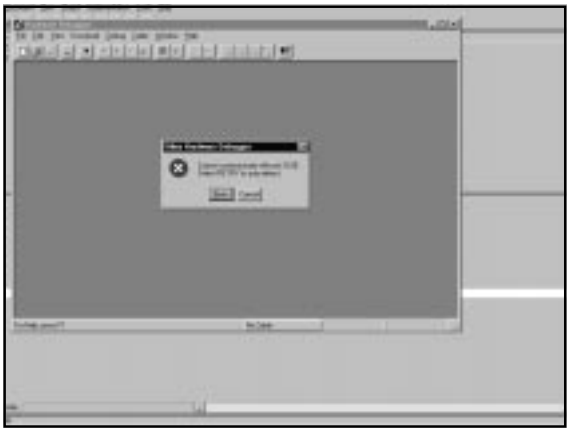
- Make sure your lab 2 schematics are in your project hierarchy
- On the project window, click on implementation
- If implementation is successful, the box under implementation turns black

Problems you might run into

- If you want to reimplement, you need to clear implementation data from your last implementation.

Download Circuit

- Power up the board
- Attach Xchecker to the board
- Click on the programming box(the box below implementation)
- A window pops up, select hardware debugger



Communication Problems

- Make sure the board has power
- Make sure Xchecker is attached in the correct orientation
- Check cable configuration. It should be Xchecker on com1.

Test Circuit

- The NUMLED on the right displays the state of the FSM
- NUMLED displays the state in hex
- State only has 3 bits. But hex needs 4 bits.
- State3(MSB) is wired to ground

Test Circuit II

- Make sure sw4-7 is closed
- Start the clock in the hardware debugger
- Watch internal signals in the hardware debugger