Final Project Report and Grading

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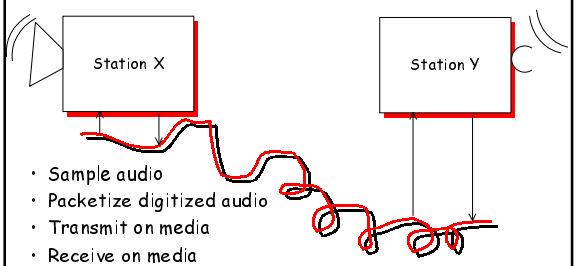
Final Project Timeline

- Early DEMO Extra Credit Deadline: 22 Nov
  - Baseline functionality sufficient
  - Get baseline working first; you can work on extra credit functionality AFTER the Early Demo
- Normal Credit DEMO Deadline: 1 Dec
  - You MUST DEMO everything--no extra credit available after 1 Dec deadline!
  - You will need to schedule a demo/debrief slot with your grading TA
- Penalty DEMO Deadline: No late demos after 8 December--hand in report on what you have
- Final Report Deadline: 8 December

Final Project Specification



- Sample audio
- Packetize digitized audio
- Transmit on media
- Receive on media
- Depacketize digitized audio
- Play back audio

Final Project Specification

- Checkpoint #1: SRAM/FIFOs
- Checkpoint #2: UART XMIT/RECEIVE
- Checkpoint #3: ADC/DAC Audio Interface
- Checkpoint #4: Packetizer/Depacketizer

You have all of the major pieces in hand!

Your mission: determine the overall control state machine, and any other "glue" you need among the components

Putting It Together

- Audio Transmission
  - Audio input from ADC sampled @ 2KHz; 8-bit unsigned integer samples (Checkpoint #3)
  - Input audio buffered in SRAM/FIFO (Checkpoint #1)
  - Audio bytes in FIFO formatted as packet
  - Detect wire available for transmission; send packet to destination station (Checkpoint #2, #4)

Putting It Together

- Audio Reception
  - Each station receives every packet sent
  - If not for this station, it is ignored
  - If for this station, buffer packet in FIFO
  - Once buffer reaches threshold, output audio samples to DAC @2 KHz

Basic User Interface

- Dipswitches (Header<7:0>)
  - Header<7:6>
    - » Basic Mode: 00, 2 KHz samples
    - » Extra Credit: 01, Hi Res samples (4 KHz)
    - » 10, 11 available for your own extra credit!
  - Header<5:3>: Destination Station ID
  - Header<2:0>: Source Station ID
- Push Buttons (two)
  - Both pressed = Reset
  - Define your own use of the individual PBs
- Left NumLED=Sender ID last received stream
- Right NumLED=DAC inputs

Rules for Extra Credit

- Must demo a working baseline design before any credit obtained for EC features
- Must demo baseline functionality by Wed, 22 November to obtain early demo EC
- Must demo all baseline *and* attempted EC functionality by final demo deadline, 1 December; No credit for EC functions after 1 December!
- Absolute late baseline demo cut-off date is 8 December; 50% penalty on late projects;
- NOTE: Reports must be handed in 8 December; No late reports accepted!

Extra Credit Suggestions

- *Most Compact Design* (smallest CLB count)
- *Broadcast Mode:* Wildcard delivery; one to many
- *Output Audio Interpolation for Better Output Audio Quality*: linearly interpolate between packets
- *Multiple Sample Rate Under Different Modes*: Hi/lo res audio (4K vs. 2Khz samples)
- *Digital Audio Mixing to Support Multiple Incoming Streams:* digitally combine incoming samples from multiple speakers
- *Call User Interface* (handshaking for calls): UI for call set-up
- *Your Good Idea for a Feature Here*

Final Report Format (Due 8 December): 5 Page Limit!

- 1. Introduction (0.5 pages)
- 2. Theory of Operation (0.5 pages)
- 3. Control Description (1 page)
- 4. Datapath Design (1 page)
- 5. Control Design (0.5 page)
- 6. Evaluation (1 page)
- 7. Lessons Learned and Conclusions (0.5 page)
- Appendix A: Control State Diagram
- Appendix B.1: SRAM/FIFO Subsystem Schematics
- Appendix B.2: UART Transmitter/Receiver Schematics
- Appendix B.3: Audio Interface Schematics
- Appendix B.4: Packet Transmission/Reception Schematics
- Appendix C: Controller Schematics
- Appendix D: Project Checkpoint Check-off Sheets

Final Report

- Introduction
  - What is the function of your project, in general terms? Any differences from original spec (e.g., EC work).
  - What aspects of your implementation make you particularly proud?
  - Why did you choose to implement that aspect of your design in that way?

Final Report

- Theory of Operation
  - Describe how your project would be used by someone not intimately familiar with it
  - What do you do on power up? How do you reset it? What is the detailed procedure for getting it going?
  - What assumptions about the supporting hardware environment are you making, e.g., memory system organization?
  - What are the detailed timing constraints on your processor, e.g., clock frequency or period and duty cycle?

Final Report

- Control Description
  - Describe basic control sequencing of your system, including user interface. E.g., state diagram, a program-like description, or similar method
- Datapath Design
  - Any changes to the checkpoints?
  - Schematics in the appendices
- Control Design
  - How does your control work? State assignments?
  - Detailed documentation in the appendices

Final Report

- Evaluation
  - What is your critical path? What is the maximum speed you can transmit/receive data?
  - Include number of Xilinx CLBs used in design. What percentage of the Xilinx component did your design consume?
- •Lessons Learned and Conclusions
  - What have you learned from you experience implementing your project? What would you do differently?
  - Include suggestions for improving the project!

Grading Criterion

- Design & Demonstration (50 pts. + 10 extra credit pts.)
  - Exceptional (50 pts.): A+
  - Outstanding (40 pts.): A/A-
  - Very Good (30 pts.): B+/B
  - Good (20 pts.): B-/C+
  - Fair (10 pts.): C/C-
  - Poor (0 pts.): F
- Early Demo Bonus (+ 10 pts.)

Grading Criterion

- Checkpoints (20 pts. + 4 extra credit pts.)
  - Checkpoint #1 (5 pts. + 1 pt. early bonus)
  - Checkpoint #2 (5 pts. + 1 pt. early bonus)
  - Checkpoint #3 (5 pts. + 1 pt. early bonus)
  - Checkpoint #4 (5 pts. + 1 pt. early bonus)
  - No points for using Norm's implementation!
- Oral Project Debrief (20 pts.)
- Written Project Report (10 pts.)
- Extra Credit (+20 pts. MAX)
  - Includes early bonuses and additional functionality