

**University of California at Berkeley**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Sciences**

EECS150  
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## Check Point 3, Audio Interfaces

### 1 Objectives

The objective of this lab is to provide you guys an interface for getting digitized audio samples from the A/D converter, and an interface to output digitized samples to a D/A converter.

Since the focus of this project is on the network functionality. I'll provide you with macros that take care of most of the interface logic to the A/D, and D/A. This will give you practice in integrating your modules with other people's design (as opposed to designing the whole thing yourself).

### 2 High Level Overview

#### A/D, D/A converters

The A/D converter is the chip that converts an analog voltage into a digitized number. In our case this converter takes a 2V peak-to-peak signal and converts it to an 8bit unsigned number. The value of the 8bit number depends on the voltage at the input signal at the beginning of the conversion.  
(for more info on the A/D chip look for the PDF spec file on [www.national.com/pf/AD/ADC08161.html](http://www.national.com/pf/AD/ADC08161.html))

The D/A is the chip that converts a 16bit 2's compliment number to an analog output voltage. The output voltage then goes through an audio op-amp to give it enough current to drive speakers, or headphones. (these little op-amps are pretty strong so if you are going to use a headphone please don't put it up to your ear until you hear how loud it gets.) Also, as you can see the format of the digital samples are not the same. This means that you will have to make the conversion somewhere in your design. For this project, audio samples will be kept as 8bit unsigned number, so your conversion to 16bit 2's compliment number should not happen until you are going to output a sample to the D/A.  
(this spec for this chip should be on the class webpage, towards the bottom)

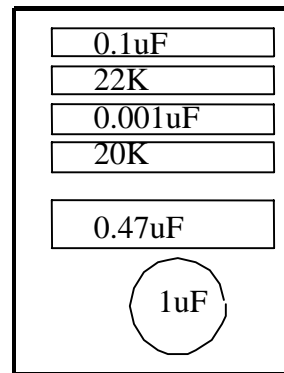
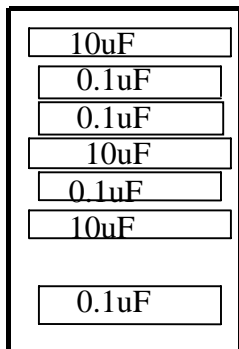
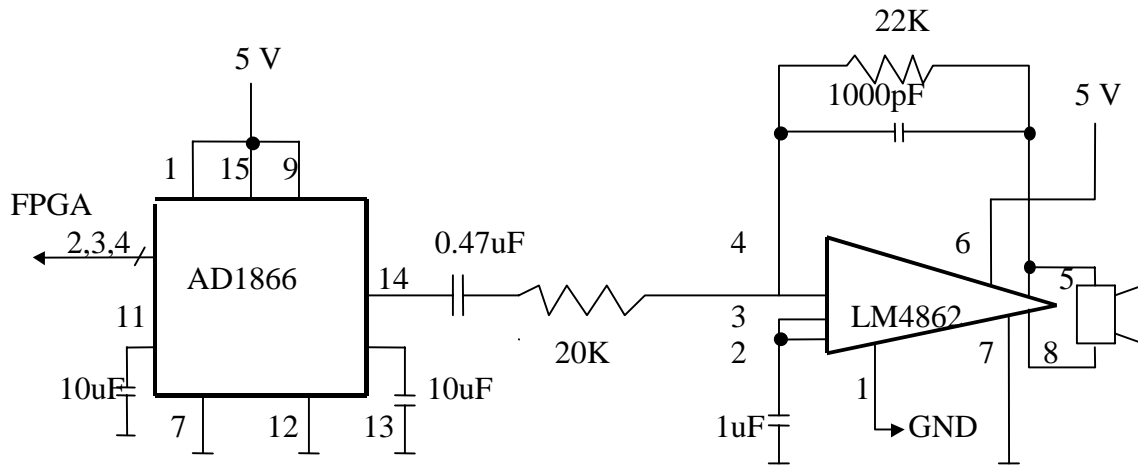
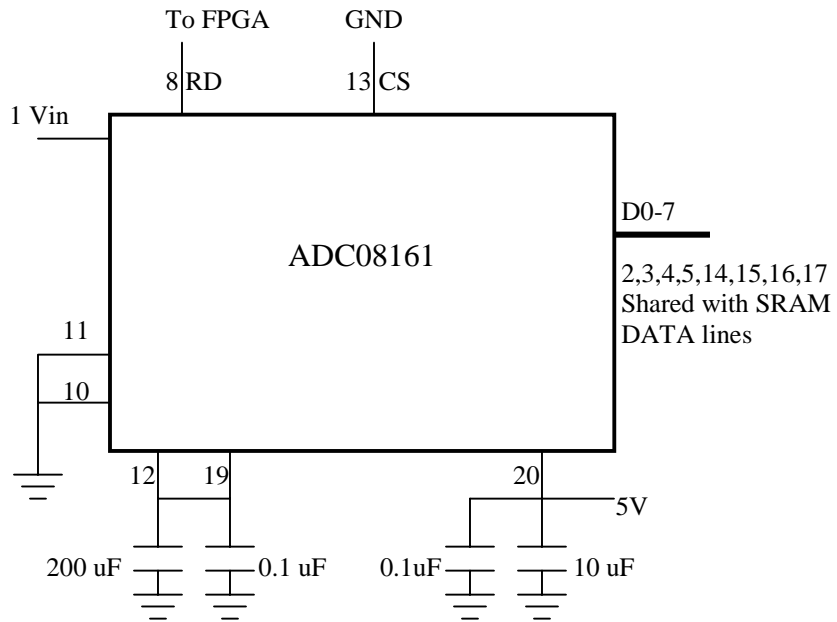
### 2 Chip Wirings

Signal	FPGA Pin
DAC LD	49
DAC LL	50
Amp SHUTDOWN	GND
DAC CLK (8MHz)	51

#### Pin connections for DAC and amplifier

Signal	FPGA Pin
RD	18
CS	GND
D0-7	SRAM IO0-7
Mode, WR, INT OFL	No Connection

#### Pin connections for A/D converter



### **3 Test Circuits**

For the test circuit please use the library file in U:\cs150\chk\_pt3\... there is also an schematic for testing the circuit. Please also read the Specs for the D/A and A/D.

When you are testing the circuit, use the signal generator in the lab to generate a signal in the audible frequency range. Connect the ground of the signal out to the board's ground. Then connect the output signal from the signal generator to the Vin of the A/D converter. Use the oscilloscope to verify that the input waveform from of the A/D looks like the output waveform of the D/A.

Name \_\_\_\_\_

Name \_\_\_\_\_

Lab Section (Check one)

M:  AM      T:  AM      W:  AM  
      PM       PM       PM

Th: \_\_\_\_\_  
          PM

### Check-offs

For this Check point 3 we only ask that you test your design for the correct wire wrapping with the provided TA schematics, and Explain the following questions to your Lab TA.

- According the A/D Spec how many ns does the RD need to be low for correct operation of a pipelined read?

TA: \_\_\_\_\_ (15%)

- How does the DAC know when to shift a bit in from LD?

TA: \_\_\_\_\_ (15%)

- When does the DAC present the 16bit value from it's internal shift-register to it's digital to analog conversion unit?

TA: \_\_\_\_\_ (15%)

- How would you go about writing the output of the D/A into SRAM? What control signal do you need to assert, when?

TA: \_\_\_\_\_ (15%)

- How fast is the A/D sampling the input Voltage?

TA: \_\_\_\_\_ (15%)

- Read the spec for the D/A and A/D converter and explain the TA provided schematics and what it's doing.

TA: \_\_\_\_\_ (25%)

**Turned in on time**

TA: \_\_\_\_\_ (×100%)

**Turned in 1 week late**

TA: \_\_\_\_\_ (×50%)