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EECS 150 R. H. Katz
Fall 2000

Problem Set # 7 (Assigned 19 October, Due 27 October)

1. In lecture 06-SeqImpl, slides 34-35, we presented a Moore Machine and Mealy Machine description for a simple sequence detector that would output a 1 whenever the bit sequence 01 or 10 has been seen in the input bit stream. Assume positive edge-triggered state flipflops and that the input changes on the falling edge of the clock.
   (a) Draw timing diagrams for how these two state machines behave for the input stream 001011010.
   (b) If the Mealy Machine is implemented as a SYNCHRONOUS MEALY MACHINE, draw the timing diagram for this sequence.
   (c) If the timing behaviors are different for the MOORE, MEALY, and SYNCHRONOUS MEALY machines, explain the reason why.
2. Design a MEALY MACHINE sequence detector state machine that outputs a 1 whenever its input stream is a 4-bit bit serial palindrome, i.e., the last two bits are mirror images of the first two bits in the 4-bit sequence. An example of the machine's correct behavior is shown below:
   Input: 0000 0110 1010 0011 1001 …
   Output: 0001 0001 0000 0000 0001 …
3. Given the following MOORE MACHINE State Transition Table, use the Implication Chart method to minimize the number of states. Draw the resulting *minimized* state diagram.

Current State	Next State				Output
	00	01	10	11	
0	1	2	0	5	0
1	0	2	3	1	1
2	5	2	4	3	1
3	5	1	0	2	0
4	0	2	5	1	1
5	5	4	0	2	0

4. Given the following MEALY MACHINE State Transition Table, perform three different state assignments and develop the minimized Next State and Output Boolean functions according the following specifications:
   (a) Assign states sequentially: A=00, B=01, C=10, D=11
   (b) Assign states using 1 Hot Encoding: A=1000, B=0100, C=0010, D=0001 (6 Variable K-maps!)
   (c) Assign states using the heuristics presented in 06-SeqImpl, Slide #69
   (d) Which yields the best implementation and why?

Current State	Next State				Output			
	00	01	10	11	00	01	10	11
A	A	B	D	C	0	1	0	1
B	B	A	B	C	0	0	0	1
C	A	D	D	C	0	0	0	1
D	A	B	B	C	0	0	0	1