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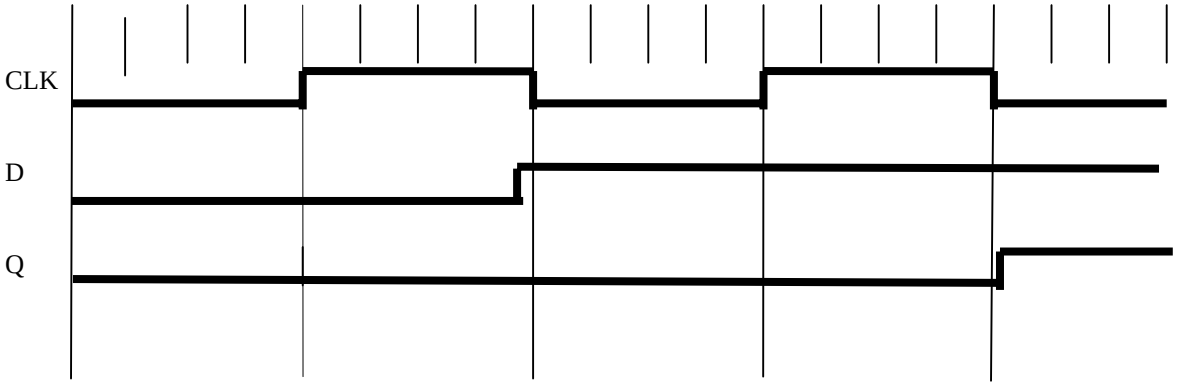
EECS 150 R. H. Katz
Fall 2000

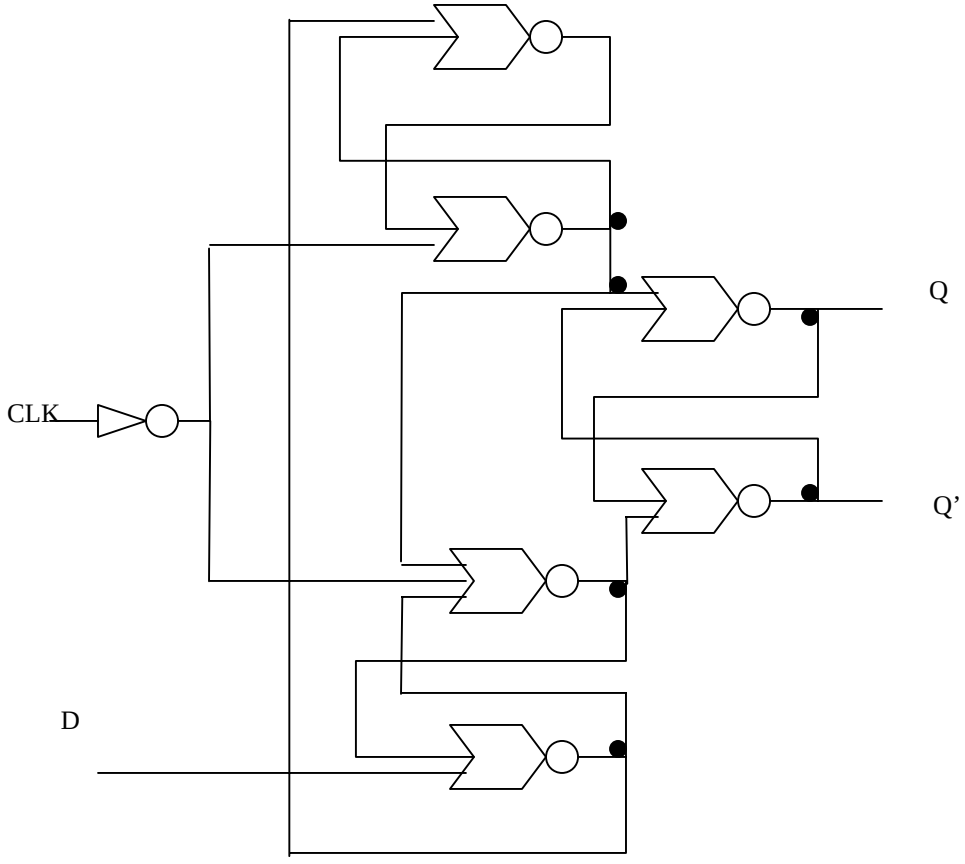
Solution Set # 5

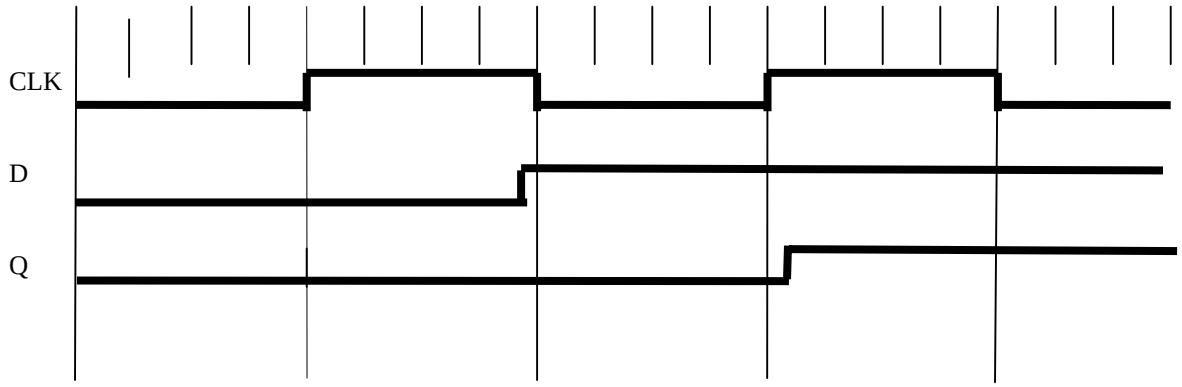
1. In lecture, we briefly presented a design for a *negative edge-triggered D flip-flop*.
   (a) Create a timing diagram that illustrates the potential problems that happen when the data input D changes (too) close to the falling edge. That is, illustrate a situation in which the input change is not latched by the flip-flop.



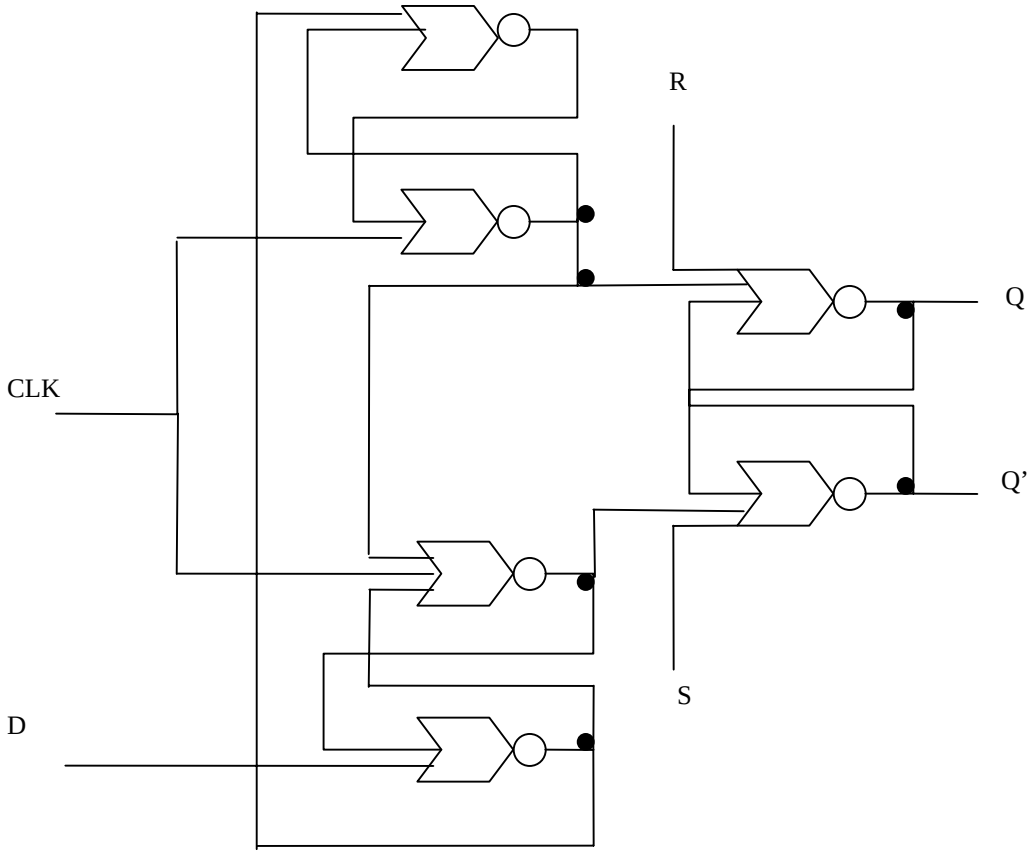
D transitions too close to the falling edge, and the high value is not latched. The D input is seen only after another falling edge occurs.

   (b) Modify the design of the flip-flop to make it *positive edge-triggered*. Include a timing waveform that illustrates how your flip-flop implementation works.

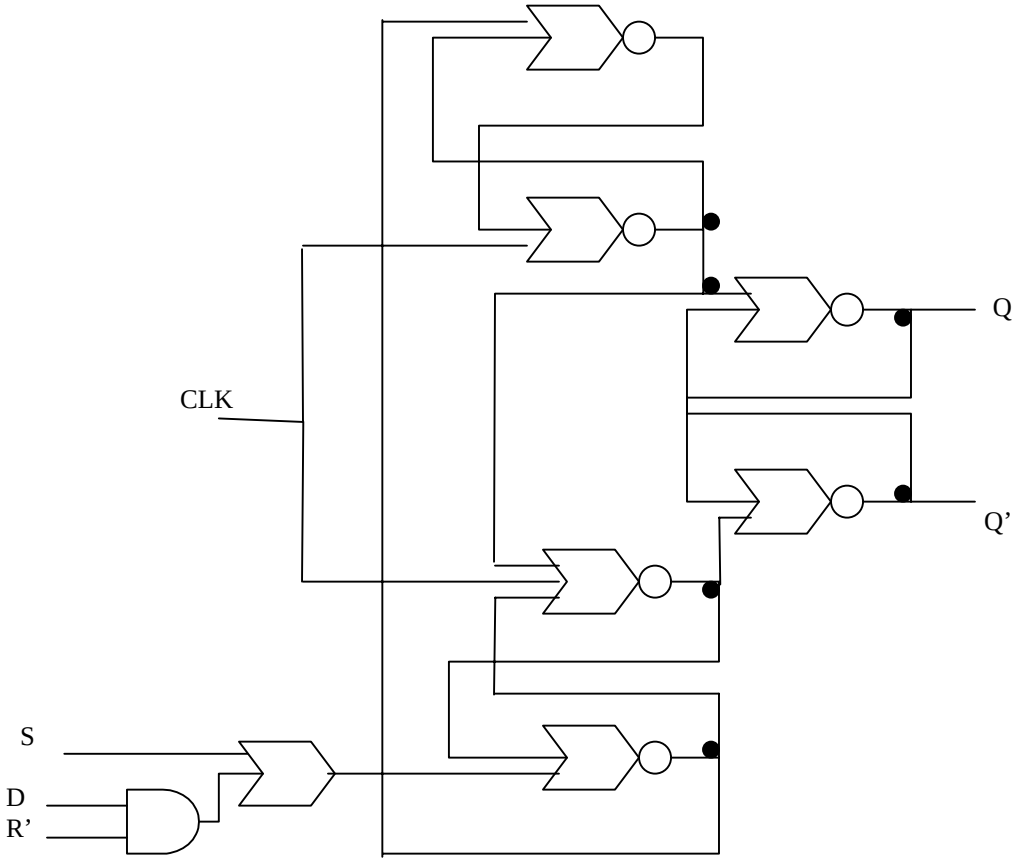




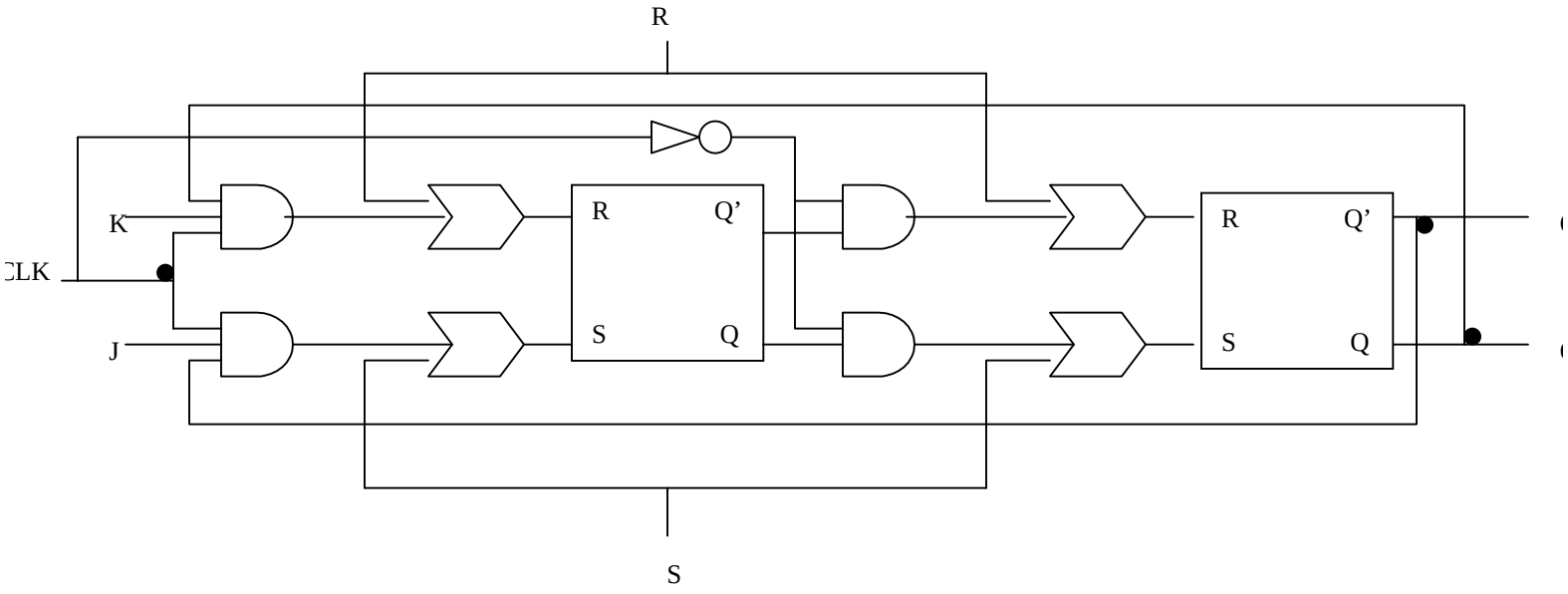
(c) Add to the negative edge-triggered flip-flop the inputs R (Reset) and S (Set). When the former is asserted, independent of the clock, the flip-flop state is forced to zero. When Set is asserted, the state is forced to one.



(d) Modify your answer to part (c) so that the Rest and Set input only take effect on the falling edge of the clock.



2. In lecture, we presented a Master-Slave flip-flop.
   (a) How would you add asynchronous (i.e., independent of the clock) set and reset signals to initialize the flip-flop to a one or zero respectively?

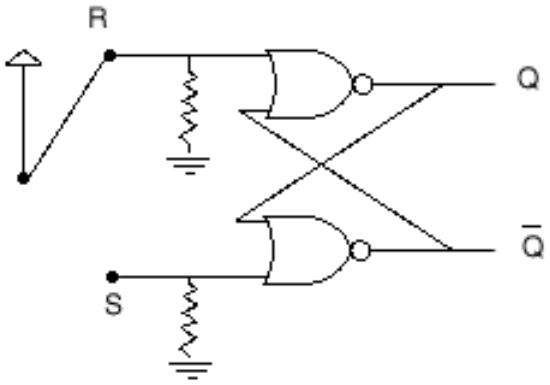


(b) Master-Slave flip-flops exhibit the phenomena of “ones catching.” Explain what it is and why it happens. Is it possible for a Master-Slave flip-flop to “catch zeros”? Justify your answer!

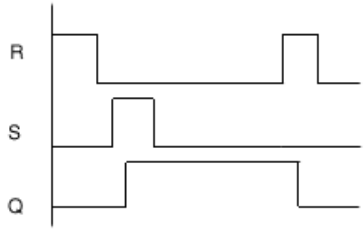
An RS latch is made of two NOR gates that hold state when the inputs are 0. If Set transitions to 1 then it gets set. If it subsequently transitions back to 0 it is still set at 1. If the Set glitches and jumps to 1 and then back to 0 quickly the 1 will still be held by the latch. It catches the one even though it may be a quick transition.

A flipflop may catch zeros if it is made of NAND gates where 1’s will make the latch hold state and a zero will set the latch. If there is a glitch, the latch may catch a zero, therefore it is possible for a Master-Slave flip-flop to do “zeros catching.”

3) The circuit shown below can be used as a debouncer. Once the switch is set to S, the output will become high. Then, even if the switch disconnects with S the output will keep its current value.



The timing diagram shown below shows the circuit's behavior:

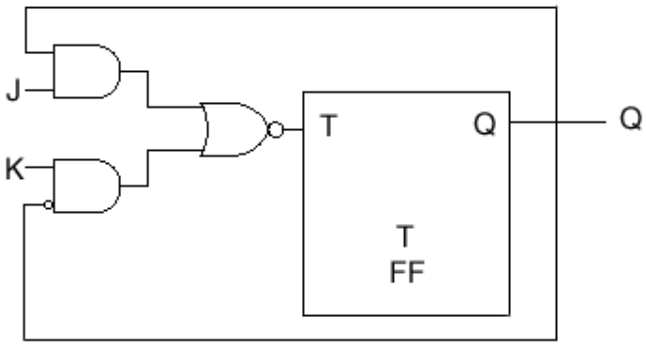


4a) Q+ = Q XOR T

Q	T	Q+
0	0	0
0	1	1
1	0	1
1	1	0

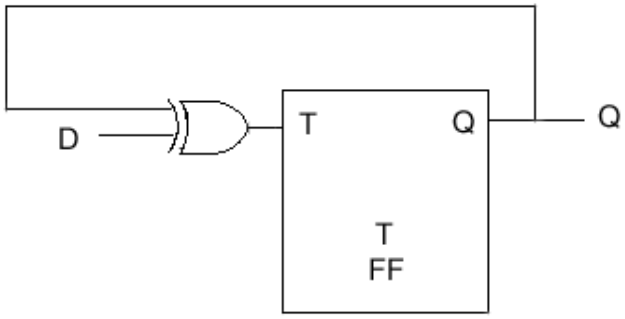
4b) JK: T = JQ' + KQ

J	K	Q	Q+	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1



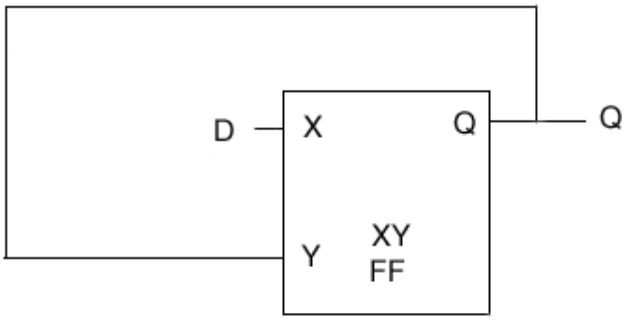
D: T = D XOR Q

D	Q	Q+	T
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0



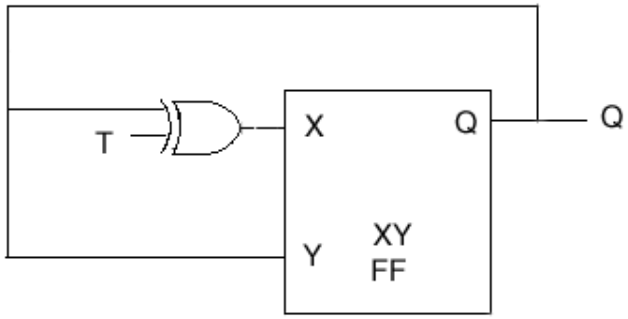
5a) X = D ; Y = Q

D	Q	Q+	X	Y
0	0	0	0	0
0	1	0	0	1
1	0	1	1	0
1	1	1	1	1



5b) X = T XOR Q ; Y = Q

T	Q	Q+	X	Y
0	0	0	0	0
0	1	1	1	1
1	0	1	1	0
1	1	0	0	1



5c) X = J + Q ; Y = K'Q

J	K	Q	Q+	X	Y
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	0	1	0