

**University of California at Berkeley**  
**College of Engineering**  
**Department of Electrical Engineering and Computer Science**

EECS 150  
Fall 2000

R. H. Katz

**Problem Set # 5 (Assigned 5 October, Due 13 October)**

1. In lecture, we briefly presented a design for a *negative edge-triggered D flip-flop*.
  - (a) Create a timing diagram that illustrates the potential problems that happen when the data input D changes (too) close to the falling edge. That is, illustrate a situation in which the input change is not latched by the flip-flop.
  - (b) Modify the design of the flip-flop to make it *positive edge-triggered*. Include a timing waveform that illustrates how your flip-flop implementation works.
  - (c) Add to the negative edge-triggered flip-flop the inputs R (Reset) and S (Set). When the former is asserted, independent of the clock, the flip-flop state is forced to zero. When Set is asserted, the state is forced to one.
  - (d) Modify your answer to part (c) so that the Rest and Set input only take effect on the falling edge of the clock.
2. In lecture, we presented a Master-Slave flip-flop.
  - (a) How would you add asynchronous (i.e., independent of the clock) set and reset signals to initialize the flip-flop to a one or zero respectively?
  - (b) Master-Slave flip-flops exhibit the phenomena of “ones catching.” Explain what it is and why it happens. Is it possible for a Master-Slave flip-flop to “catch zeros”? Justify your answer!
3. Describe how to use an R-S latch to debounce a mechanical switch. Explain why your solution works through the use of a timing diagram.
4. A Toggle flip-flop is a device with a single input T such that when T is true, the flip-flop will toggle its state when the clock arrives. When T is false, the flip-flop holds its state.
  - (a) Give an excitation table and characteristic equation for the T flip-flop.
  - (b) A J-K flip-flop behaves exactly like an R-S flip-flop, except that the inputs  $J=K=1$  causes the flip-flop to toggle its state. Show how to implement D and J-K flip-flops using a single T flip-flop and additional combinational logic at the T input.
5. Consider a new (and slightly weird) kind of flip-flop dubbed the X-Y flip-flop. When  $X=Y=0$ , the flip-flop is set to zero. When  $X=1, Y=1$ , the flip-flop is set to one. When  $X \neq Y$ , the flip-flop complements its state.
  - (a) Show how to implement a D flip-flop using the X-Y flip-flop.
  - (b) Show how to implement a T flip-flop using the X-Y flip-flop.
  - (c) Show how to implement a J-K flip-flop using the X-Y flip-flop.