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EECS 150 R. H. Katz
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Problem Set # 4 - Solution

1a) Inputs: n_of_d[1:0]
n_of_n[2:0]
Outputs: d_out[1:0]
n_out[2:0]
no_change

b) The d_out bits tell how many dimes should be given: 00 for none, 01 for one, and 10 for two. Three dimes should never be given so 11 is undefined.
The n_out bits are similar to dimes_out: 000 for none, 001 for one, 010 for two, 011 for three, 101 for four, and 110 for five. Anything else is undefined.
no_change will be 1 if it is not possible to return change and 0 if it is. If no_change is 1, we don't care about all the other outputs. I'm assuming that the larger system will ignore the other output signals when no_change is 1.

c)

n_of_d1	n_of_d0	n_of_n2	n_of_n1	n_of_n0	d_out1	d_out0	n_out2	n_out1	n_out0	no_change
0	0	0	0	0	x	x	x	x	x	1
0	0	0	0	1	x	x	x	x	x	1
0	0	0	1	0	x	x	x	x	x	1
0	0	0	1	1	x	x	x	x	x	1
0	0	1	0	0	x	x	x	x	x	1
0	0	1	0	1	x	x	1	0	1	0
0	0	1	1	0	x	x	1	0	1	0
0	0	1	1	1	x	x	1	0	1	0
0	1	0	0	0	x	x	x	x	x	1
0	1	0	0	1	x	x	x	x	x	1
0	1	0	1	0	x	x	x	x	x	1
0	1	0	1	1	0	1	0	1	1	0
0	1	1	0	0	0	1	0	1	1	0
0	1	1	0	1	0	1	0	1	1	0
0	1	1	1	0	0	1	0	1	1	0
0	1	1	1	1	0	1	0	1	1	0
1	0	0	0	0	x	x	x	x	x	1
1	0	0	0	1	1	0	0	0	1	0
1	0	0	1	0	1	0	0	0	1	0
1	0	0	1	1	1	0	0	0	1	0
1	0	1	0	0	1	0	0	0	1	0
1	0	1	0	1	1	0	0	0	1	0

1	0	1	1	0	1	0	0	0	1	0
1	0	1	1	1	1	0	0	0	1	0
1	1	0	0	0	x	x	x	x	x	1
1	1	0	0	1	1	0	0	0	1	0
1	1	0	1	0	1	0	0	0	1	0
1	1	0	1	1	1	0	0	0	1	0
1	1	1	0	0	1	0	0	0	1	0
1	1	1	0	1	1	0	0	0	1	0
1	1	1	1	0	1	0	0	0	1	0
1	1	1	1	1	1	0	0	0	1	0

d_out1:

n_of_d1=0

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	0	0	0	0
10	x	x	0	x

n_of_d1=1

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	1	1	1
01	1	1	1	1
11	1	1	1	1
10	x	1	1	1

d_out1 = n_of_d1

d_out0:

n_of_d1=0

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	1	1	1	1
10	x	x	1	x

n_of_d1=1

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	0	0	0
01	0	0	0	0
11	0	0	0	0
10	x	0	0	0

d_out0 = n_of_d1'

n_out2:

n_of_d1=0

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	x	x	x
01	x	1	1	1
11	0	0	0	0
10	x	x	0	x

n_of_d1=1

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	0	0	0
01	0	0	0	0
11	0	0	0	0
10	x	0	0	0

n_out2 = n_of_d1'·n_of_d0

n_out1:

n_of_d1=0

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	x	x	x
01	x	0	0	0
11	1	1	1	1
10	x	x	1	x

n_of_d1=1

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	1	1	1
01	1	1	1	1
11	1	1	1	1
10	x	1	1	1

d_out1 = n_of_d1 + n_of_d0

n_out0:

n_of_d1=0

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	x	x	x
01	x	1	1	1
11	x	x	x	x
10	x	x	x	x

n_of_d1=1

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	x	1	1	1
01	1	1	1	1
11	1	1	1	1
10	x	1	1	1

n_out0 = 1

no_change:

n_of_d1=0

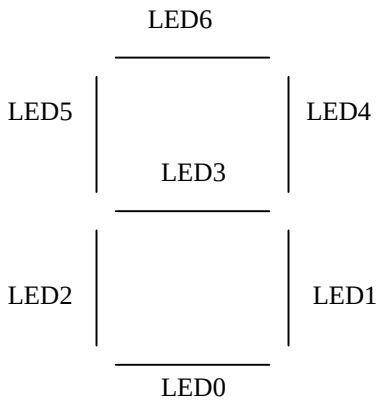
n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	1	1	1	1
01	1	0	0	0
11	1	1	1	1
10	1	1	1	1

n_of_d1=1

n_of_d0|n_of_n2 \ n_of_n1|n_of_n0	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	0	0	0	0
10	1	0	0	0

no_change = n_of_d1'·n_of_d0 + n_of_d1'·n_of_n2' +
n_of_d1'·n_of_n1·n_of_n0 + n_of_n2'·n_of_n1'·n_of_n0'

2) This is the way I am labeling the display:



A	B	C	D	L6	L5	L4	L3	L2	L1	L0
0	0	0	0	1	1	1	0	1	1	1
0	0	0	1	1	0	0	0	0	0	0
0	0	1	0	1	0	0	1	0	0	0
0	0	1	1	1	0	0	1	0	0	1
0	1	0	0	0	1	1	1	0	0	0
0	1	0	1	0	0	0	1	1	1	0
0	1	1	0	0	0	1	1	1	0	0
0	1	1	1	0	1	0	1	0	1	0
1	0	0	0	0	1	1	0	1	1	0
1	0	0	1	0	1	1	1	1	1	0
1	0	1	0	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X

L6:

AB \ CD	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	X	X	X	X
10	0	0	X	X

L6 = A’B’

L5:

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	0	1	0
11	X	X	X	X
10	1	1	X	X

L5 = A + C’D’ + BCD

L4:

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	0	0	1
11	X	X	X	X
10	1	1	X	X

L4 = A + C’D’ + BCD’

L3:

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	1	1
11	X	X	X	X
10	0	1	X	X

L3 = C + B + AD

L2:

AB \ CD	00	01	11	10
00	1	0	0	0
01	0	1	0	1
11	X	X	X	X
10	1	1	X	X

L2 = A + B’C’D’ + BC’D + BCD’

L1:

AB \ CD	00	01	11	10
00	1	0	0	0
01	0	1	1	0
11	X	X	X	X
10	1	1	X	X

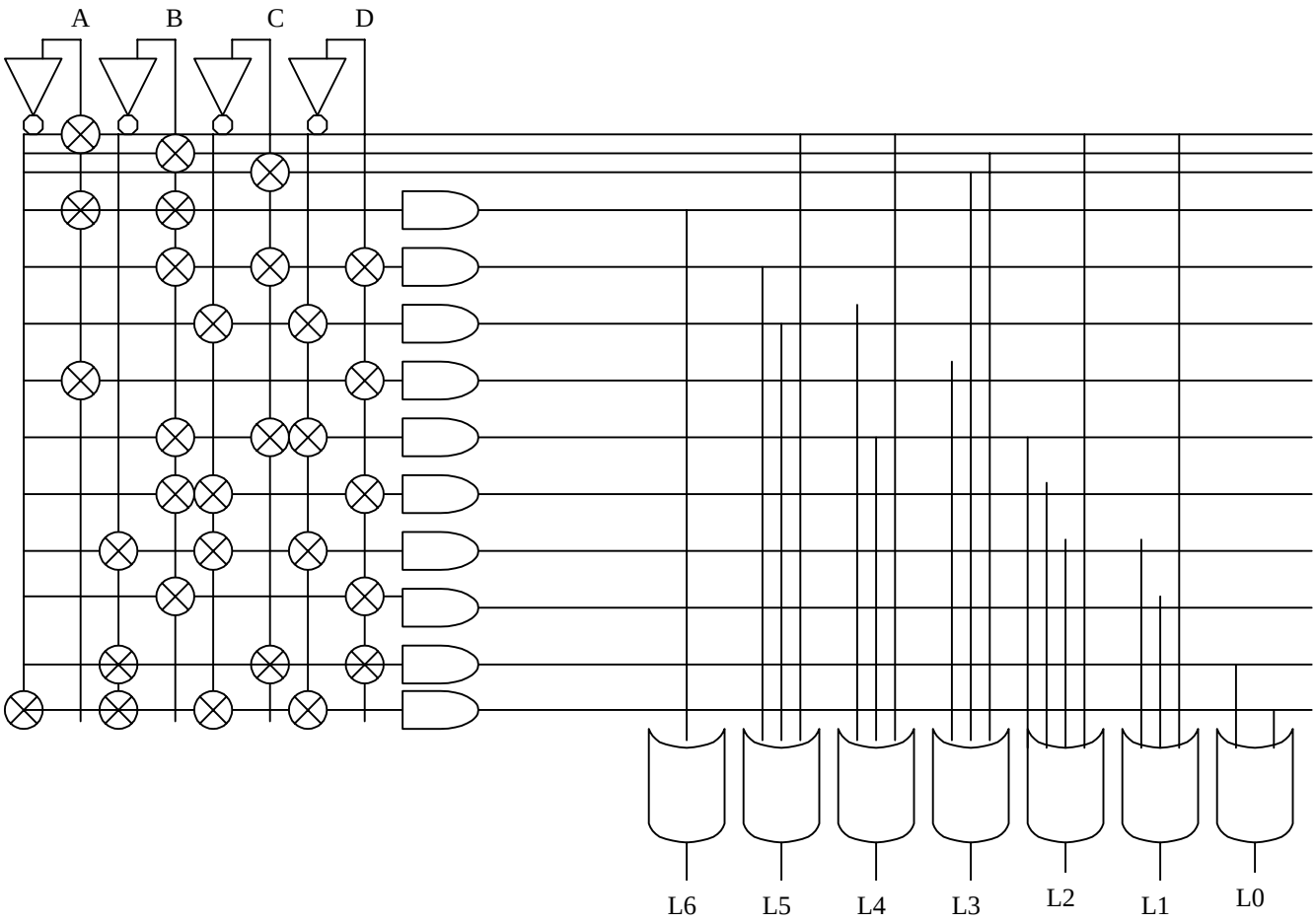
L1 = A + BD + B’C’D

L0:

AB \ CD	00	01	11	10
00	1	0	1	0
01	0	0	0	0
11	X	X	X	X
10	0	0	X	X

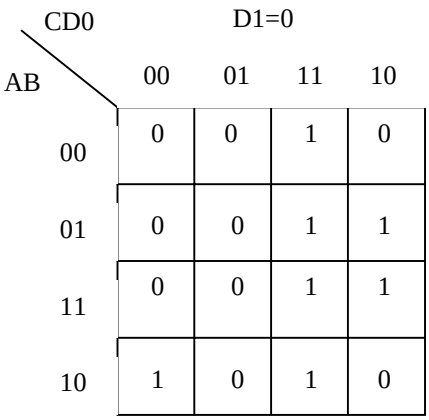
L0 = A’B’C’D’ + B’CD

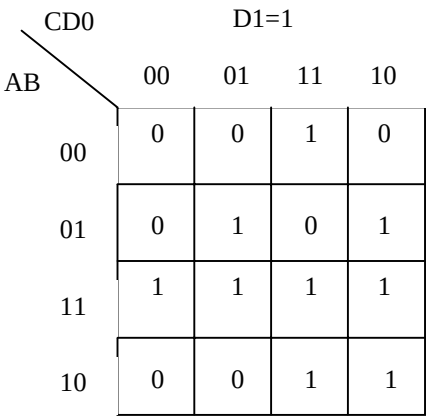
L5 AND L6



3a)

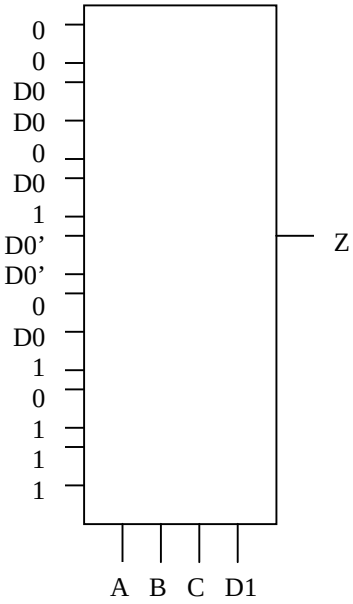
A	B	C	D0	D1	Z
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

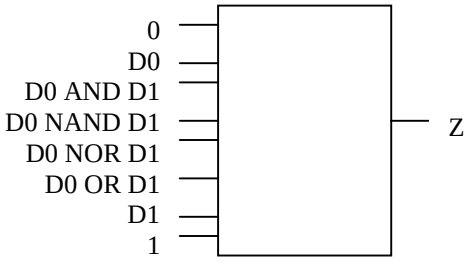




Z = AB’C’D0’D1’ + BCD1’ + B’CD0 + BC’D0D1 + ABD1 + BCD0’ + ACD1

b, c)





d) In terms of logic gates, the implementation in part a) will be the best.