UNIVERSITY OF CALIFORNIA AT BERKELEY
COLLEGE OF ENGINEERING
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Using Project Navigator

Overview

Xilinx Project Navigator is an Integrated Development Environment for digital logic design projects with Xilinx FPGAs and CPLDs. Project Navigator provides a simple way to centrally manage the files in your project as well as automatically invoking all of the other CAD tools.

Please note that Project Navigator is not perfect. As with most any professional CAD tool, it in continuously being updated and improved. There are some known problems, mostly notably: **No project or file may have a space in the path or filename.**

There are six main steps to using Project Navigator, as detailed below.

1. Create a Project
2. Add Files to Your Project
3. Using ModelSim from Project Navigator
4. Synthesize, Place and Route
5. Program the CaLinx board
6. Clean the Project for Archiving

Detailed Instructions: Step 1 – Create a Project

1. Start by opening **Project Navigator** from the Desktop.
    a. You can also find project navigator on the start menu.
    b. Click **OK** to get rid of the **Tip of the Day**
2. Go to **File -> New Project**
3. **New Project – Name, Location and Top-Level Module**
    a. Give the project some kind of **apropriate name** which describes it.
        i. Remember spaces are not allowed.
    b. Set the project location to **C:\users\cs150-xxx**, Project Navigator will automatically create a subdirectory for your project.
    c. Set the **Top-Level Module Type** to **HDL**
    d. Click **Next**

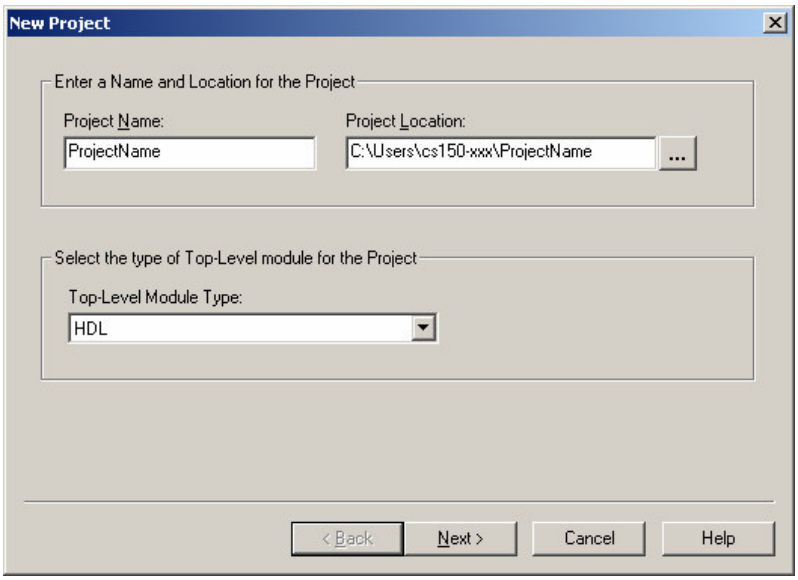

Figure 1: New Project – Name, Location and Top-Level Module

4. **New Project – Device and Design Flow**
   a. Device Family: **VirtexE**
   b. Device: **xcv2000e**
   c. Package: **fg680**
   d. Speed Grade: **-6**
   e. Synthesis Tool: **Synplify Pro (VHDL/Verilog)**
   f. Simulator: **Modelsim**
   g. Generated Simulation Language: **Verilog**
   h. Click **Next**

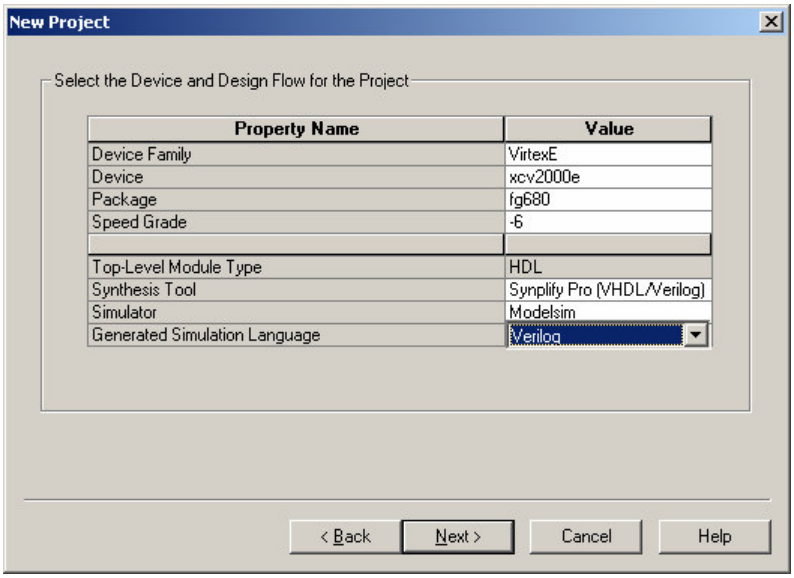

Figure 2: New Project – Device and Design Flow

5. **New Project – Create New Source**

a. We do not encourage you to create new files in Project Navigator. By keeping your verilog and project files separate you can easily create new projects and keep track of your files.

6. **New Project – Add Existing Sources**
   a. You should keep your Verilog source files in a subdirectory of **C:\users\cs150-xxx separate from your project**. Please use good sense and make sure to keep your files organized, **CVS is a good idea**. Using an old file or losing a file can waste **days** of your time. For an example of good organization see figure 3 below.

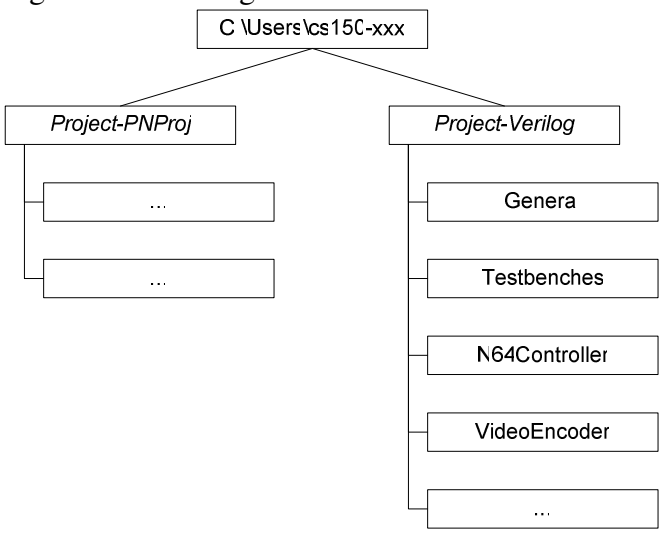

Figure3: Example Directory Structure

   b. During this step you should add **Const.V** if you are using any of our modules which require it.
      i. Anything that is not a testbench, including Const.V, is a **Verilog Design File**.
      ii. Make sure that the **Copy to Project** box is **checked**, for this file **and ONLY this file**.
   c. Click **Next**

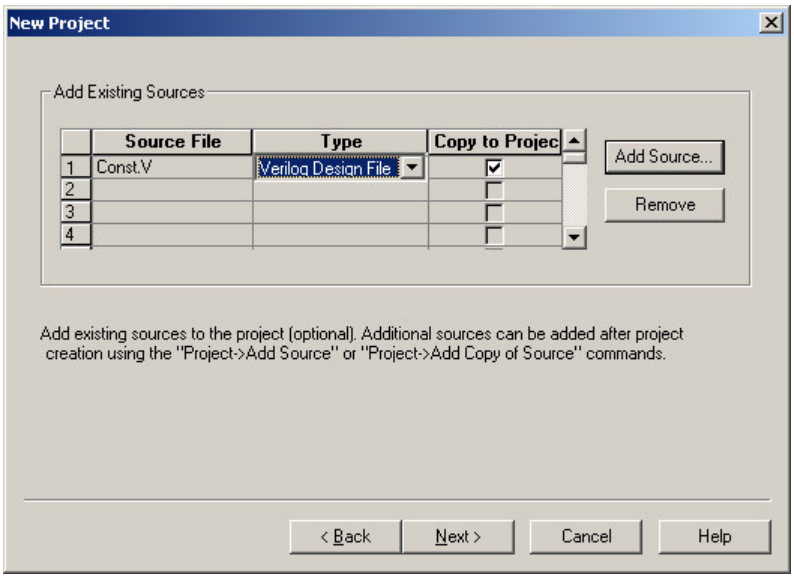

Figure 4: New Project – Add Existing Sources

7. **New Project – Information**
   a. Please make sure to double check the information displayed in this screen.

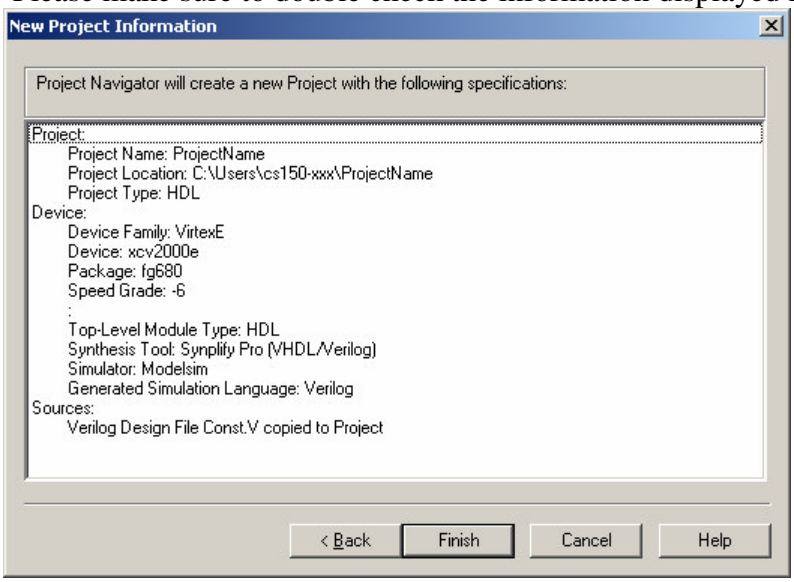

Figure 5: New Project - Information

8. You should now have a new project with only a copy of **Const.V** added to it.

Detailed Instructions: Step 2 – Add Files to Your Project

1. **Right-click** in the **Sources in Project** box and select **Add Source** from the drop down meny.
   a. The Sources in Project box is in the upper left of the Project Navigator main window.

   b. By select **Add Source** instead of Add Copy of Source, you can avoid having duplicate files and accidentally using an old version of a file.
2. **Navigate to the folder** that contains your **Verilog source code**.
3. Select the various verilog files as required by your project.
   a. You can use **Shift-Click** to select a range of files.
   b. You can use **Control-Click** to select or deselect individual files.
4. **Click Open** to add these files to your project.
   a. Any of your verilog meant for **synthesis** should be a **Verilog Design File**
   b. Your **testbenches** should be **Verilog Test Fixture File**s
   c. As files are added they will appear in the **Sources in Project** box
   d. If there are errors in your source files, Project Navigator will warn you in the **Console/Log at the bottom of the screen**.
   e. Project Navigator will attempt to construct a tree of all the modules in the files you add, showing which modules are instantiated where.
   f. Modules listed with a **?** next to them are missing.

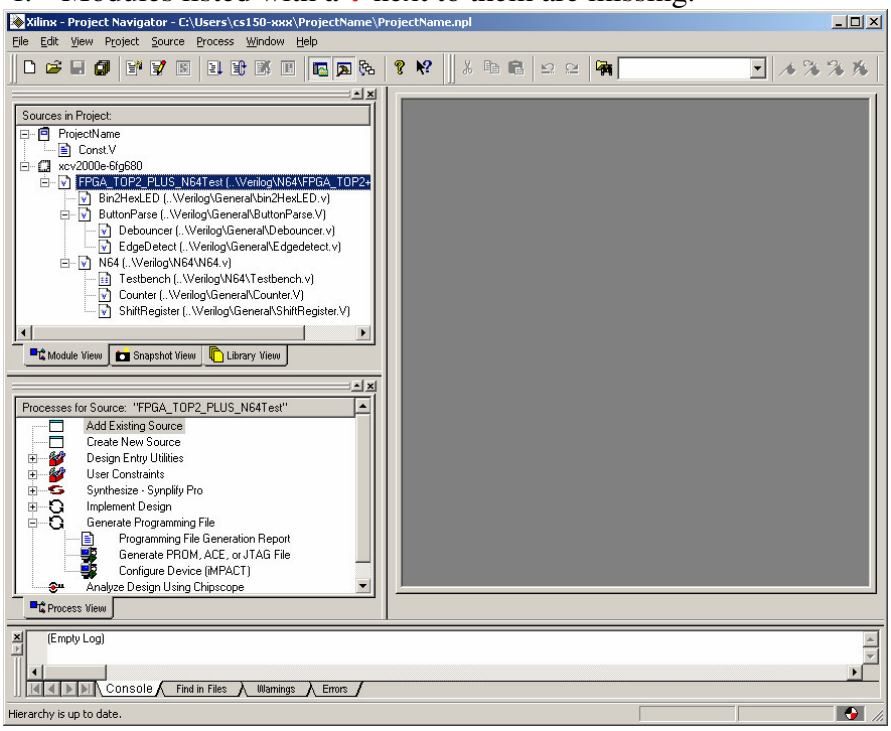

Figure 6: Project Navigator with Verilog Source Files

5. Repeat steps 1-4 **until all your Verilog files have been added**.

Detailed Instructions: Step 3 – Using ModelSim from Project Navigator

1. Please note that while this is certainly convenient, it is **highly recommended** that you read the **ModelSim Tutorial** and learn to use ModelSim well, it is a relatively easy tool to work with, but requires a little practice.
   a. http://www-inst.eecs.berkeley.edu/~cs150/fa04/Documents.htm#Tutorials
2. **Select the testbench** you want to use in the **Sources in Project** box.

a. Note that due to a design flaw in Project Navigator testbenches which instantiate multiple modules cannot be automatically launched.

3. If you are simulating our modules, you will want to declare the MODELSIM flag during the Verilog compilation process. This is a relatively complex exercise.
   a. Go to the **Edit -> Preferences** menu in Project Navigator.
      i. Navigate to the **Processes** tab.
      ii. Set the **Property Display Level** to **Advanced**

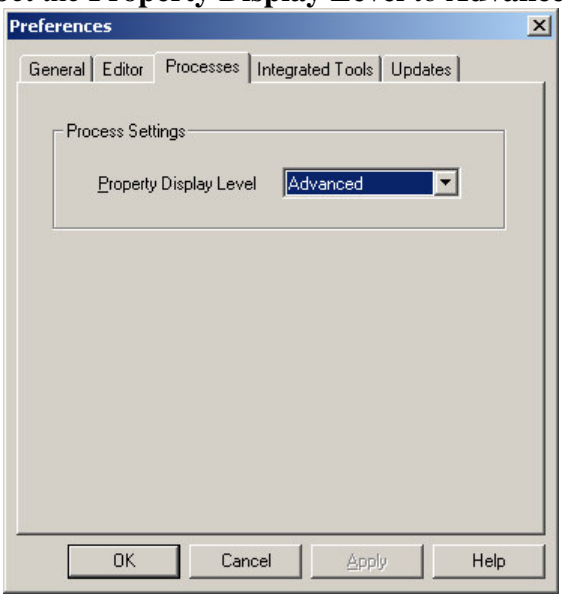

Figure 7: Setting Property Display Level to Advanced

      iii. Click **OK**
   b. **Right-Click** on **ModelSim Simulator -> Simulate Behavioral Model** process in the **Processes for Source** box
      i. Make sure the correct testbench is still selected in the **Sources in Project** box
      ii. Select **Properties** from the popup menu
      iii. In the **Other VLOG Command Line Options** box type **+define+MODELSIM**, taking care to keep the capitalization and the plusses.

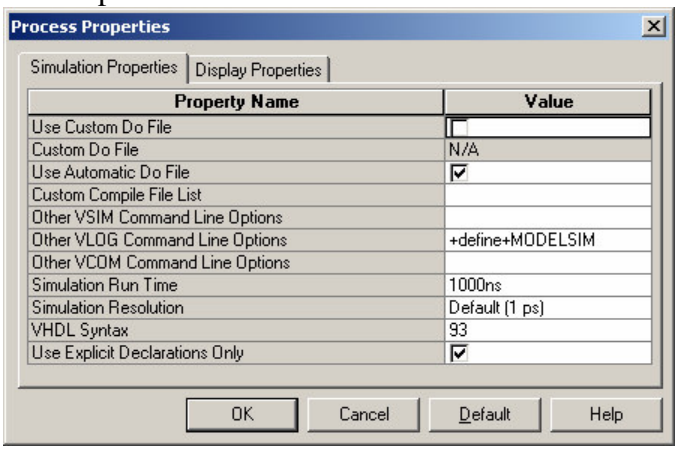

Figure 8: Defining the MODELSIM Simulation Flag

iv. Feel free to examine the other options. For example **Simulation Run Time**
v. Click **OK**

4. **Double-Click** on the **Simulate Behavioral Model** process in the **Processes for Source** box
   a. Make sure the correct testbench is still selected in the **Sources in Project** box
   b. This will launch ModelSim, compile your Verilog files, open a wave window and run the simulation.

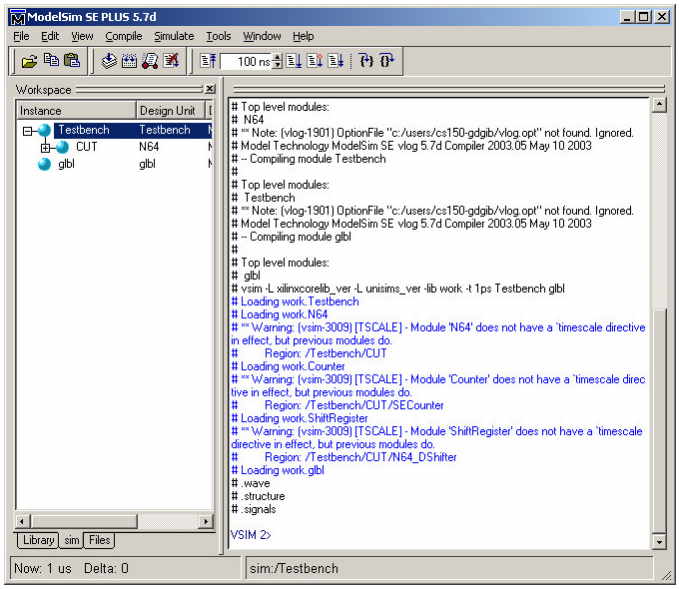

Figure 9a: The Main ModelSim Window (Sim Tab and Command Line)

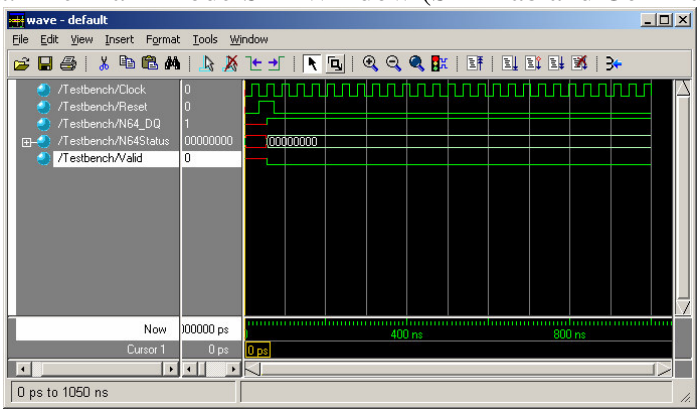

Figure 9b: A ModelSim Wave Window

5. For more information on ModelSim, please refer to the ModelSim Tutorial.

Detailed Instructions: Step 4 – Synthesize, Place and Route

1. Xilinx Project Navigator was designed primarily to manage this step, the **Processes for Source** box is the primary way to access all of the tools and reports generated during the implementation process.

   a. A **V** means that that step in the implementation process completed successfully.
   b. A **!** means that that step has warnings, which you may need to look into. Most of the warnings given by Project Navigator can be safely ignored.
      i. Design Rule Check or DRC violations are very serious and cannot be ignored.
   c. A **X** means that that step failed and you will need to examine the error log (at the bottom of the Project Navigator Window) to see why.
   d. A **?** means that something has been changed since the last time that step was run, and it should therefore be rerun.
2. Select the **top level Verilog module** in the **Sources in Project** box.
   a. This will almost always be **FPGA_TOP2.v** or **FPGA_TOP2+.v**
   b. **Do not synthesize anything but the top level module**
3. If you are using **Black Boxes**
   a. **Right-click** on the **Implement Design** step and select **Properties**
   b. Navigate to the **Translate Properties** tab
   c. Set the **Macro Search Path** to the directory which **contains your black boxes**

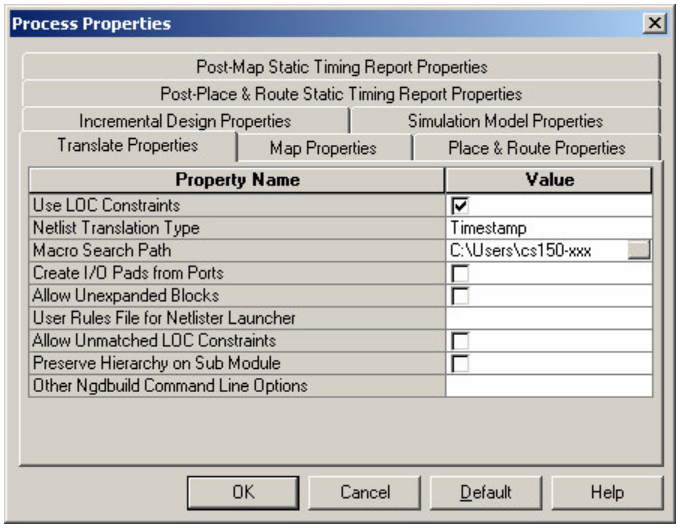

Figure 10: Setting the Macro Search Path

4. **Double-Click Generate Programming File** step in the **Processes for Source** box.
   a. This will cause Project Navigator to attempt to synthesize, place, route and generate a bitfile from the Verilog you have given it.
5. If there are **synthesis errors**
   a. **Double-Click View Synthesis Report** under **Synthesize – Synplify Pro**. This will launch Synplify Pro, and allow you to peruse the error and warning logs at the bottom of the window
   b. **You may wish to examine the Synthesis warnings even if there are no errors, the warnings may explain a particular bug or problem you are seeing.**
6. If there are **errors in other steps**

a. Under each implementation step there is a **Log File** which you can double click on. This will bring up a text file showing any and all errors and warnings generated during that step.

7. If all goes well, proceed to **step 5**.

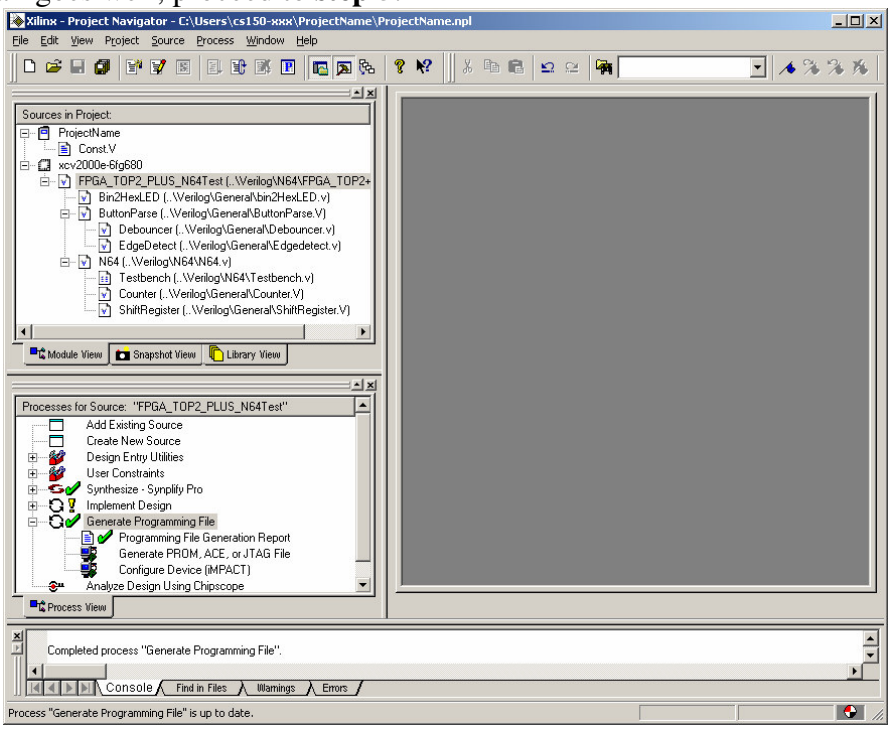

Figure 11: Project Navigator, Implementation Successful

Detailed Instructions: Step 5 – Program the CaLinx Board

1. Make sure that the the **Parallel Cable IV** is connected to the **Slave Serial** port on the CaLinx board and that the CaLinx board is on.
   a. The little light on the Parallel Cable IV will turn **green** when the cable detects that it is connected to a **powered Xilinx chip**.
   b. The power switch for the CaLinx board is in the upper right of the board.
2. Run **iMPACT** from **Project Navigator**
   a. Select **Slave Serial Mode**
   b. When it asks for a file select **FPGA_TOP2.bit**, or whatever bitfile you wish to use.
   c. **Right click** on the picture of the FPGA and select **program**

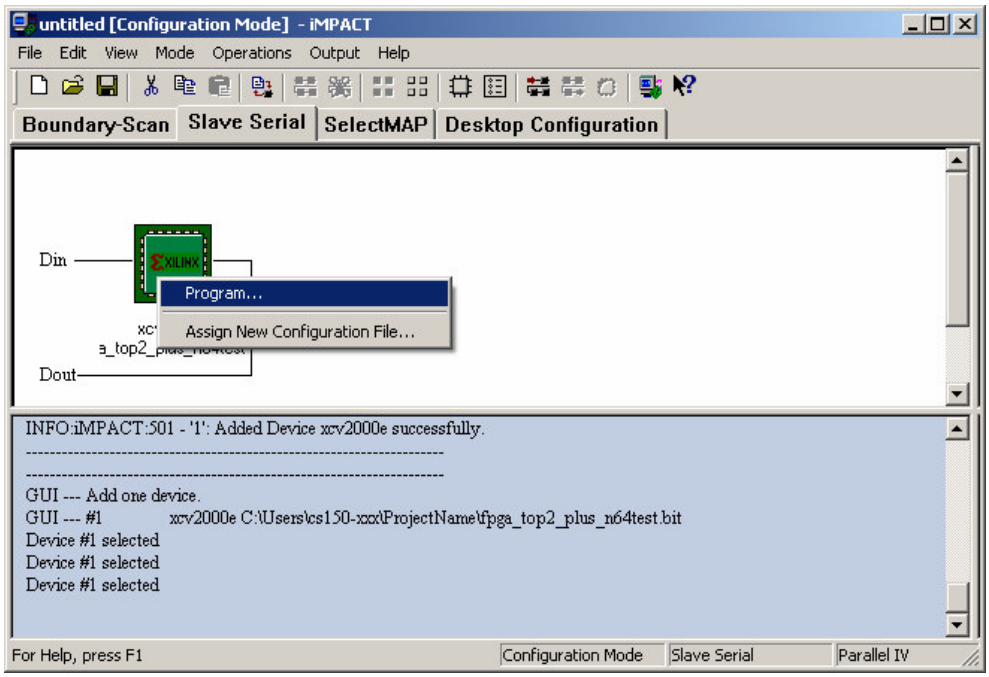

Figure 12: iMPACT

Detailed Instructions: Step 6 – Clean the Project for Archiving

1. Go to the **Project Menu** and select **Cleanup Project Files**
   a. Click **Yes** in the dialog box that pops up.
   b. None of your verilog will be deleted.
2. This will delete all of the unnecessary temporary files that Project Navigator and Synplify generate during the implementation process
3. After this step, remember to copy your Verilog and project back to your U:\ drive for permanent storage.

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