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Using ModelSim

Overview

ModelSim is a very powerful simulation environment, and as such can be difficult to master. Thankfully with the advent of **Xilinx Project Navigator 6.2i**, the Xilinx tools can take care of launching **ModelSim** to simulate most projects. However, a rather large flaw in Xilinx Project Navigator 6.2i is **its inability to correctly handle test-benches which instantiate multiple modules**.

To correctly simulate a test bench which instantiates multiple modules, you will need to create and use a **ModelSim project manually**. The steps are fairly simple:

1. Create a directory for your project
2. Start ModelSim and create a new project
3. Add all your verilog to the project
4. Compile your verilog files
5. Start the simulation
6. Add signals to the wave window
7. Recompile changed verilog files
8. **Restart/Run the simulation**

Detailed Instructions: Step 1 – Create a directory for your project

1. Because **ModelSim** creates rather large output files you should **not** save your **ModelSim** projects to the U:\ drive, it is a simple matter to **recreate the project** anyway.
2. **Create** a subdirectory in **C:\Users\cs150-xxx**, perhaps something like **C:\Users\cs150-xxx\Simulation**
3. When you are done simulating **delete this entire directory**, this will remove the ModelSim project and all of its temporary files. Obviously **your verilog should be elsewhere**.

Detailed Instructions: Step 2 – Start ModelSim and Create a Project

1. **Start ModelSim** from the desktop.
2. At the main ModelSim window go to **File -> New -> Project**
    a. Enter a **project name,** this is for your reference only
    b. Set the **Project Location** to the directory you created in **Step1** above.
    c. You can leave the **Default Library Name** as **work**
    d. Click **OK**
3. Continue with **Step3** below.

Detailed Instructions: Step 3 – Add Your Verilog to the Project

1. Click **Add Existing File** to add your verilog to the project.
    a. Click **Browse** to locate the verilog files you wish to add.
    b. **Note:** you can add multiple files at a time by using **Shift-Click** or **Control-Click** to select them all at once.
    c. Leave **Add File as Type** on **default**.
    d. Leave **Folder** as **Top Level**
    e. You will almost certainly want to select **Reference from current location**, otherwise you will end up with multiple copies of the same verilog file floating around, a sure way to lose something.
        i. Note that you will want to select **Copy to project directory** for the **Const.V** include file, otherwise ModelSim will not be able to find it.
    f. Click **OK**
2. Repeat this until all of the necessary verilog files have been added to the project.
    a. If you are simulating a project involving **Xilinx library components** you will need to **add C:\Xilinx\Verilog\src\glbl.v to your project**
3. Click **Close**

Detailed Instructions: Step 4 – Compile your verilog files

1. The **project pane** on the left of the main ModelSim window should list all of the files in your project with an icon next to each one.
    a. A **?** means that the file has **not been compiled** since the last edit.
    b. An **X** means that the file could not be compiled, it has an error.
        i. Double clicking the **X** will bring up a list of **errors** with line numbers
        ii. **Control-G** in notepad lets you jump to a specific line number
    c. A **V** means that the file has been compiled **successfully**.
2. Use **Shift-Click** to select **all of your verilog files**, and then **Right-Click** and select **Properties**
    a. Go to the **Verilog** tab
    b. Click the **Marco** button
    c. Enter **MODELSIM** into the **Macro Name** box, leaving the **Value** box empty.
    d. Click **OK** until you get to the **ModelSim Main Window**
3. **Right-Click** in the **Project Pane** and select **Compile -> Compile Out-of-Date**, this will attempt to compile all of the files with **?** next to them.
4. If you **change any verilog** source files you must **recompile them before restarting** the simulation. (See Step 4.3 above)

Detailed Instructions: Step 5 – Start the Simulation

1. Go to **Simulate -> Simulate** to bring up the simulation dialog box.
    a. Alternatively you may use the **vsim** command. See the ModelSim manual for more information. This will be much faster and easier.
2. Go to the **Libraries** tab.
    a. Click **Add** to add a new **search library**.
    b. Navigate to **C:\ModelTech_5.8d\unisims_ver** and then click **OK**, this will add the **unisims_ver** library to your project.
    c. Click **Add** to add a new **search library**.
    d. Navigate to **C:\ModelTech_5.8d\XilinxCoreLib_ver** and then click **OK**, this will add the **XilinxCoreLib_ver** library to your project.
3. Go to the **Design** tab.
    a. Click the **plus** next to the **work** library.
    b. Find your **testbench** and select it.
    c. If you are simulating a project involving **Xilinx library components** you will need to **add a space and then "glbl" to the simulate box** in the lower left.
    d. Click **Load**.
4. Your design should now be loaded and ready to simulate.
    a. If your design does not load, reread the above steps carefully.
    b. You should also check for errors and warnings from ModelSim, both are indicative of potential problems with your code.

Detailed Instructions: Step 6 – Add Signals to the Wave Window

1. With the simulation running, the **Sim Panel** should be visible on the left hand side of the **ModelSim Main Window**.
    a. The **Sim Panel** shows the hierarchy of all the modules in your project.
    b. **Clicking the plus** next to a module will show the modules instantiated within it.
2. You should add as many signals as you might need to the ModelSim window.
3. To add all signals from a module
    a. **Right-Click** on a module in the **Sim Panel** and select **Add –> Add to Wave**.
    b. This will add all of the signals from that module to the **Wave Window**.
    c. Please, look at signals inside your modules rather than just in the testbench.
    d. Remember that when debugging you cannot see too few signals.
4. To add individual signals
    a. Go to the **Signals Window**
        i. If it is not visible, use the **View -> Signals** window to display it
    b. **Drag the signals** you wish to see to the **Wave Window**
5. You can view busses in any number system, rather than just binary.
    a. Select a signal, or **group of signals**
    b. **Right-Click** on them and select **Radix -> Hexadecimal** to display those signals in hex.

c. This can allow you to see significantly more data on one screen and can make it easier to read.

Detailed Instructions: Step 7 – Recompile Changed Verilog Files

1. When you have fixed bugs, or simply made changes you must **recompile your verilog files**
2. Near the bottom left of the **ModelSim Main Window** are tabs for the **Project** and **Sim panes**.
3. Navigate to the **Project Pane**
4. **Right-Click** anywhere in the pane and select **Compile -> Compile Out-of-Date** to recompile the modified files (Which should have **?** next to them)

Detailed Instructions: Step 8 – Restart/Run the Simulation

1. You must do this any time to make changes such as:
   a. **Changing/recompiling verilog**
   b. **Adding new signals to the wave window.**
2. At the command prompt type "**restart –f; run 100us**" this will run your simulation
   a. **restart –f** tells ModelSim that it needs to start the simulation over from the beginning, that is to say at time 0.
   b. **run 100us** tells ModelSim to run the simulation for 100 micro-seconds. **100ns** would be 100 nano-seconds. **100ms** would be 100 milli-seconds.
3. Note that if you cannot see all of the necessary information, you may run the simulation for additional time.
   a. Example: (total running time: 110us)
   restart –f; run 100us
   run 10us

RevC - 9/14/2004	Greg Gibeling	Updated for ModelSimSE 5.8d Added instructions for handling glbl.v dependancy
RevB - 7/1/2004	Greg Gibeling	Added instructions for using Const.V Added instructions for defining the MODELSIM flag Added more information about Signals/Waves Minor editing
RevA	Greg Gibeling	Original