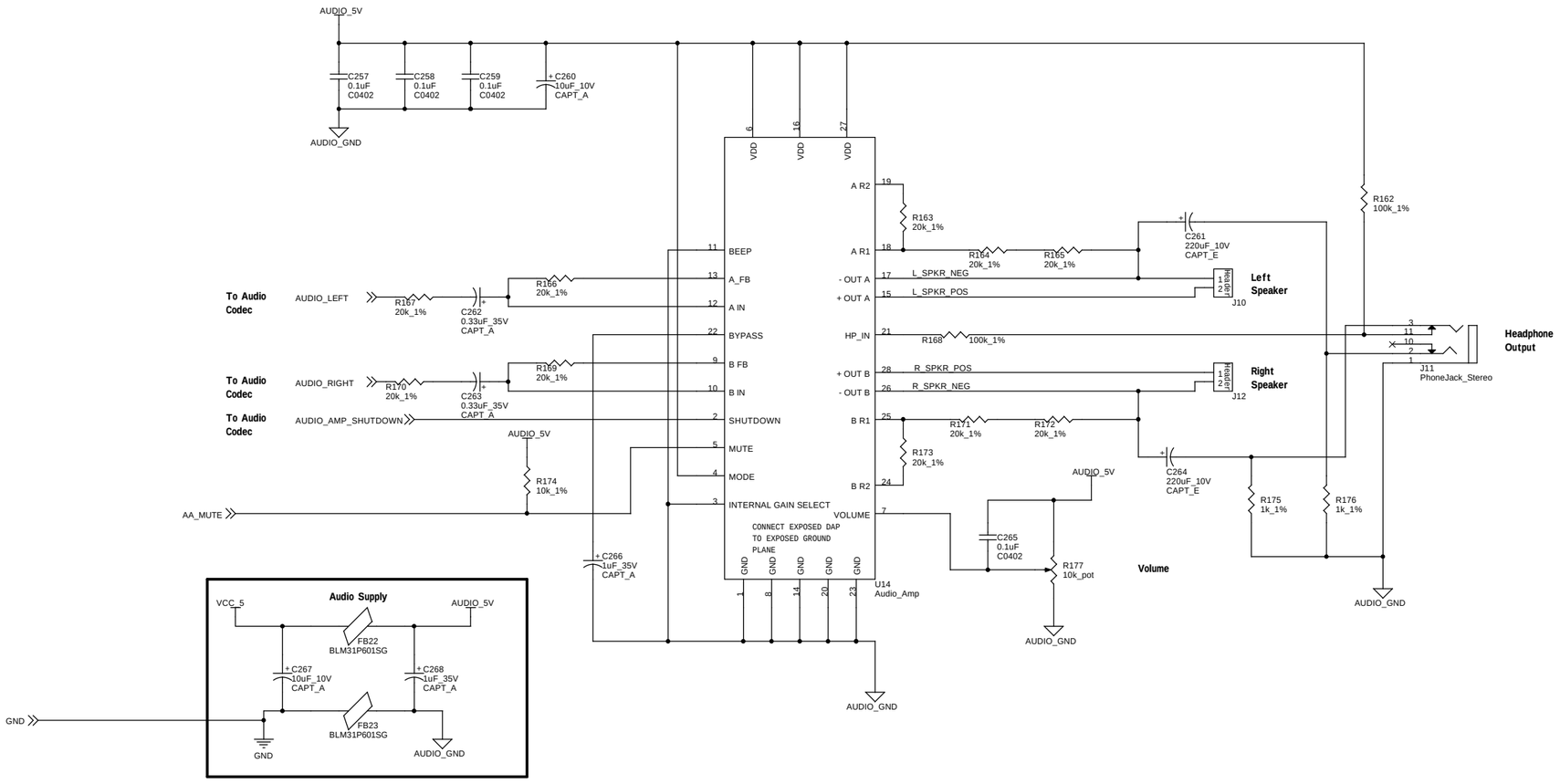
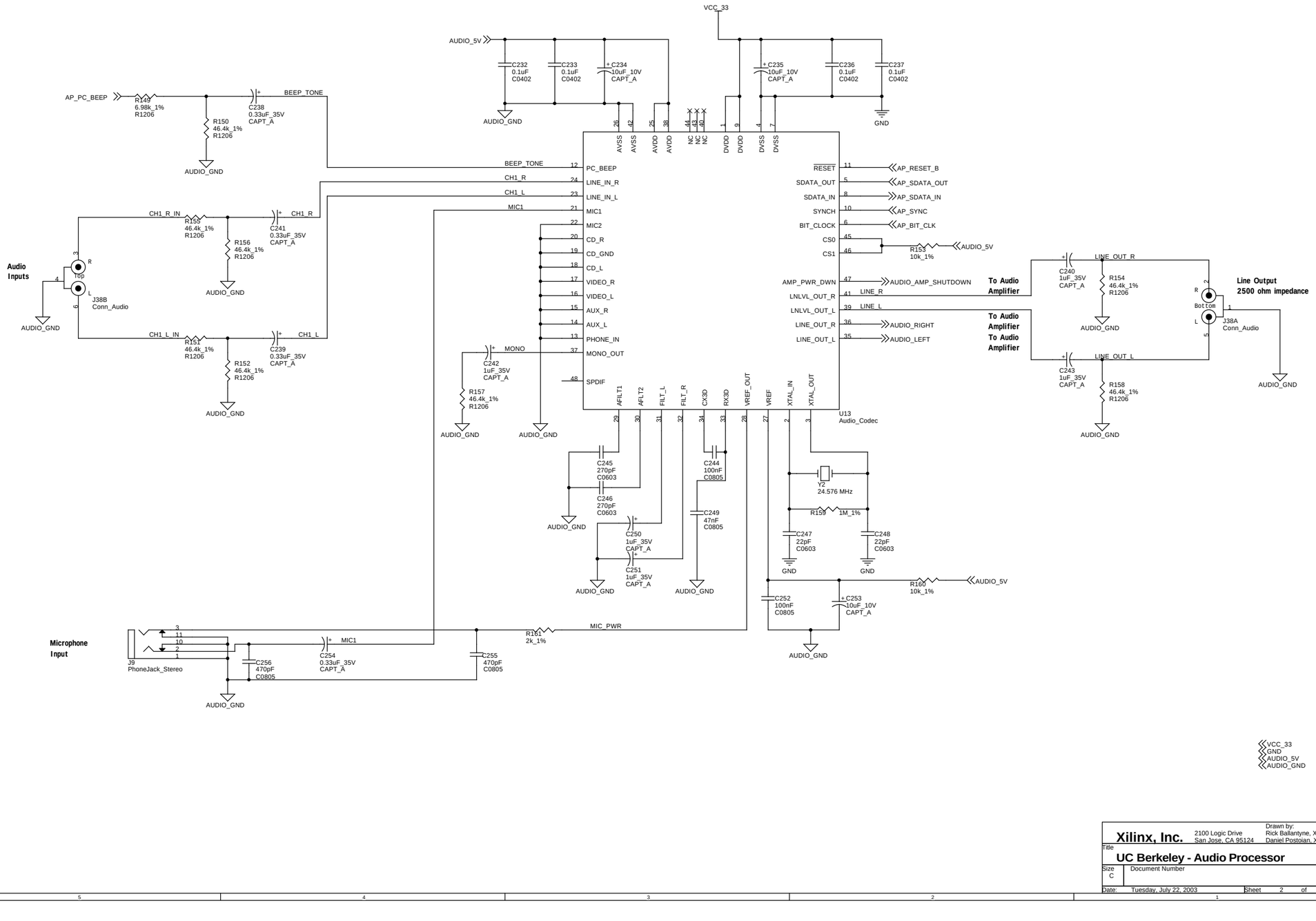
NOTES:
ALL AA_* OFF PAGE CONNECTORS GO TO FPGA BANK 2.



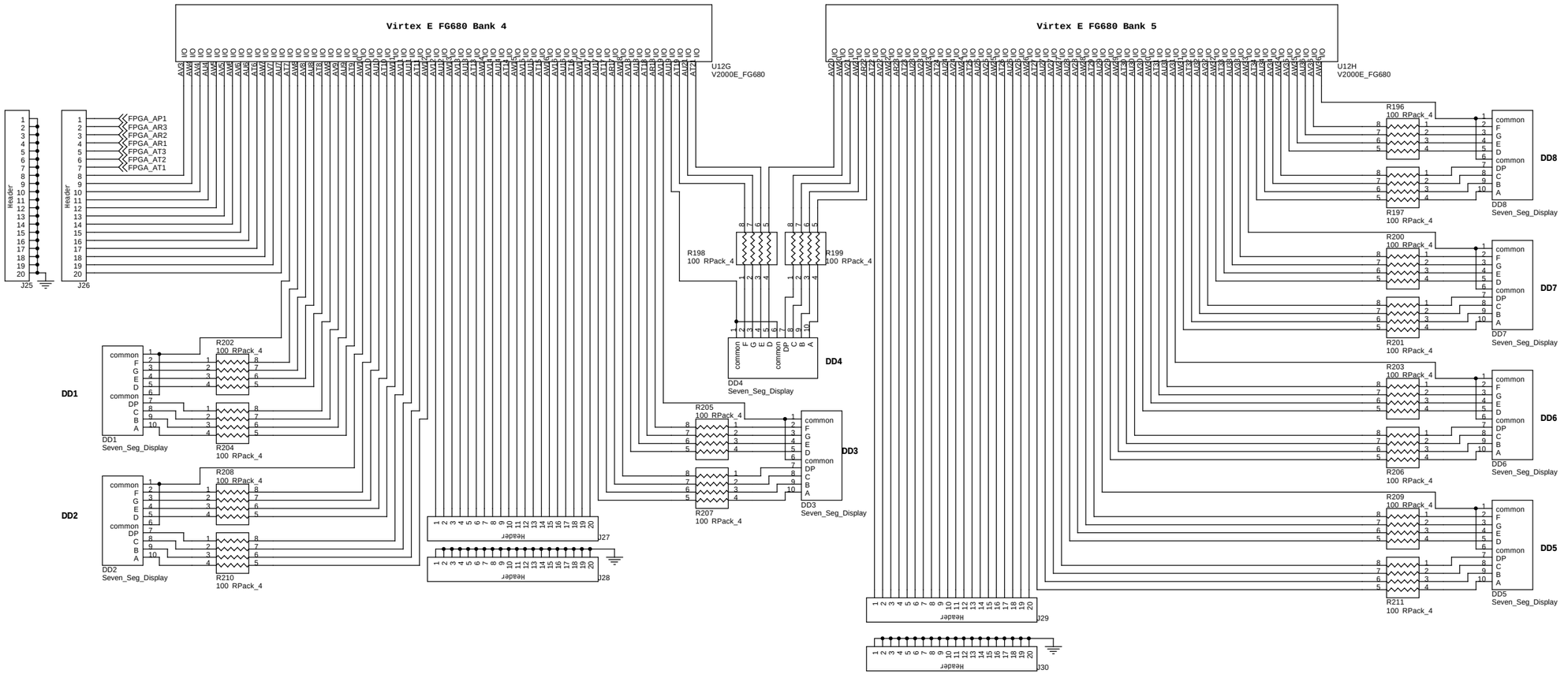
VCC_5
GND
AUDIO_5V
AUDIO_GND

Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn by: Rick Ballantyne, Xilinx Labs Daniel Postoian, Xilinx APD	
Title: **UC Berkeley - Audio Power Amplifier**			
Size: C	Document Number		Rev: C.1
Date: Tuesday, July 22, 2003	Sheet 1 of 15		

NOTES:
ALL AP_* OFF PAGE CONNECTORS GO TO FPGA BANK 1.



Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn by: Rick Ballantyne, Xilinx Labs Daniel Postoian, Xilinx APD	
Title: **UC Berkeley - Audio Processor**			
Size: C	Document Number		Rev: C.1
Date: Tuesday, July 22, 2003	Sheet 2 of 15		

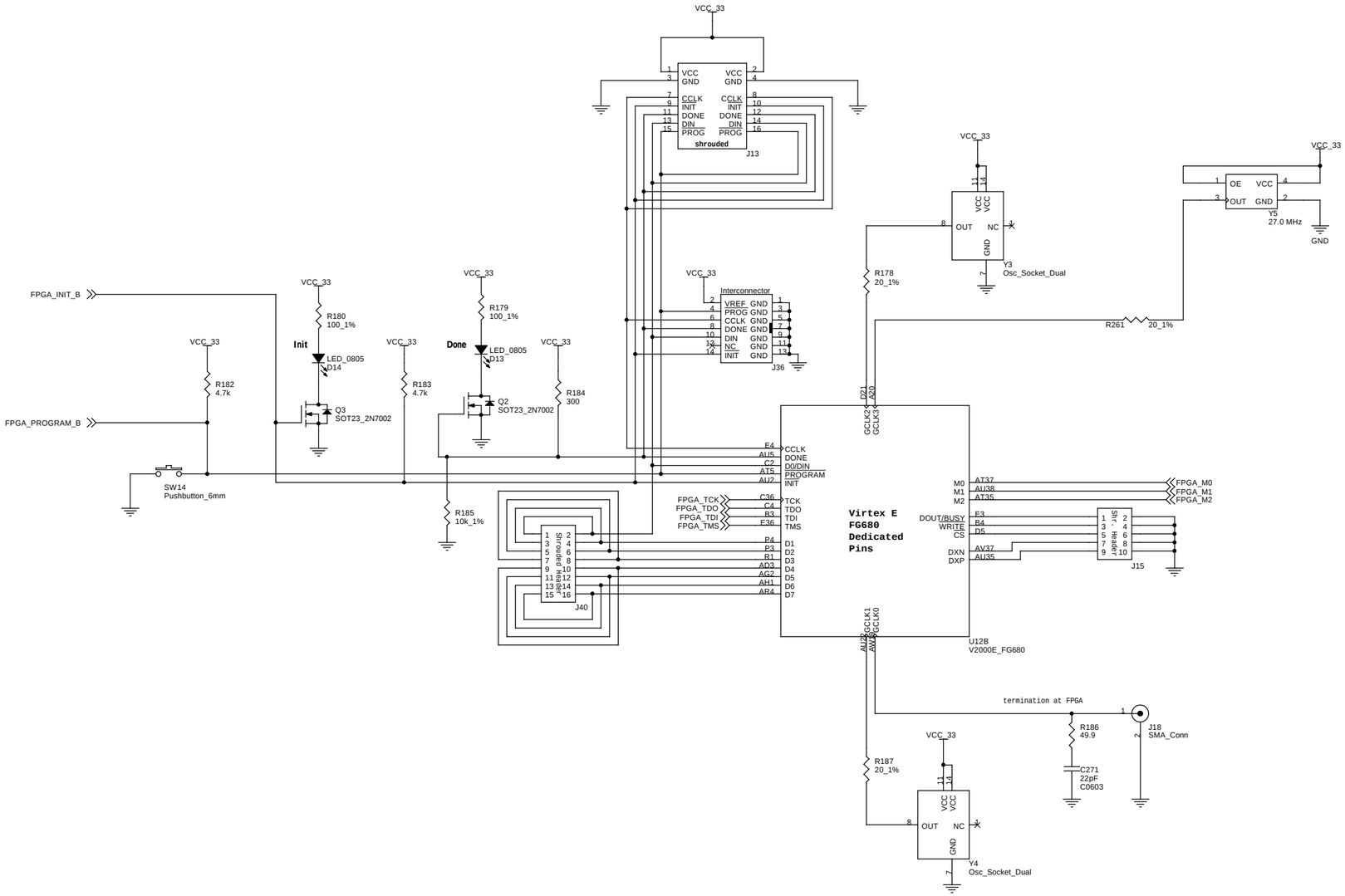


Seven Segment Displays

Display DD1	FPGA Pin Number	Display DD2	FPGA Pin Number	Display DD3	FPGA Pin Number	Display DD4	FPGA Pin Number	Display DD5	FPGA Pin Number	Display DD6	FPGA Pin Number	Display DD7	FPGA Pin Number	Display DD8	FPGA Pin Number
A	AT9	A	AW12	A	AU17	A	AR22	A	AT27	A	AV29	A	AW31	A	AT34
B	AU9	B	AT11	B	AT17	B	AW21	B	AU27	B	AW29	B	AT32	B	AU34
C	AV9	C	AU11	C	AR17	C	AV21	C	AV27	C	AT30	C	AU32	C	AV34
D	AT8	D	AW11	D	AV18	D	AV20	D	AU28	D	AV30	D	AW32	D	AV35
E	AU8	E	AT10	E	AU18	E	AT21	E	AV28	E	AW30	E	AT33	E	AW35
F	AW8	F	AV10	F	AR18	F	AT19	F	AT29	F	AU31	F	AV33	F	AV36
G	AV8	G	AU10	G	AT18	G	AU21	G	AW28	G	AT31	G	AU33	G	AU36
Common Point	AT7	Common Point	AW10	Common Point	AV19	Common Point	AU19	Common Point	AU29	Common Point	AV31	Common Point	AW33	Common Point	AW36
	AW9		AV11		AW18		AW20		AW27		AU30		AV32		AW34

Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn By: Daniel Postoian, Xilinx APD		
Title: UC Berkeley - FPGA Banks 4 & 5				
Size: C	Document Number		Rev: C.1	
Date: Tuesday, July 22, 2003	Sheet 3 of 15			

2003 CHANGES:
MOVED Y5 FROM VIDEO ENCODER PAGE & CHANGED THE MANNER OF ITS CONNECTION SUCH THAT IT GOES SOLELY TO THE FPGA. THE OTHER PINS PREVIOUSLY DRIVEN BY Y5 ARE NOW TO BE DRIVEN BY FPGA I/O PINS.



VCC_33
GND

Xilinx, Inc.	2100 Logic Drive, San Jose, CA 95124	Drawn By: Daniel Postoian, Xilinx APD	
Title: UC Berkeley - FPGA Dedicated Pins			
Size: C	Document Number		Rev: C.1
Date: Tuesday, July 22, 2003	Sheet 4 of 15		

2003 CHANGES

ADDED VE_CLKIN CONNECTION TO VIDEO ENCODER

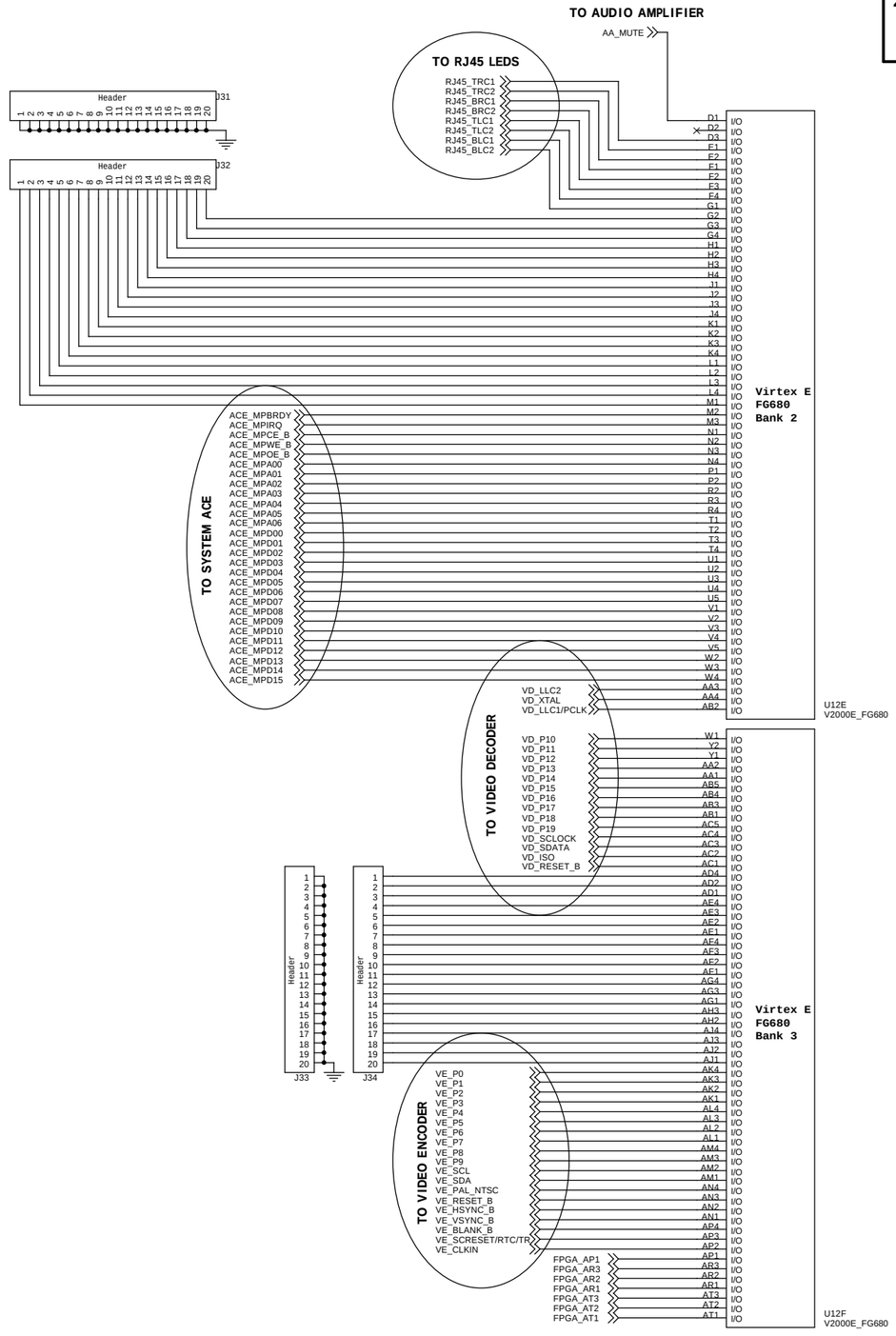
ADDED VD_XTAL CONNECTION TO VIDEO DECODER

SystemACE		
ACE Pin Name	ACE Pin Number	FPGA Pin Number
MPA00	70	N4
MPA01	69	P1
MPA02	68	P2
MPA03	67	R2
MPA04	45	R3
MPA05	44	R4
MPA06	43	T1
MPBRDY	39	M2
MPCE_B	42	N1
MPD00	66	T2
MPD01	65	T3
MPD02	63	T4
MPD03	62	U1
MPD04	61	U2
MPD05	60	U3
MPD06	59	U4
MPD07	58	U5
MPD08	56	V1
MPD09	53	V2
MPD10	52	V3
MPD11	51	V4
MPD12	50	V5
MPD13	49	W2
MPD14	48	W3
MPD15	47	W4
MPIRQ	41	M3
MPOE_B	77	N3
MPWE_B	76	N2

Audio Amplifier		
Audio Amp Pin Name	Audio Amp Pin Number	FPGA Pin Number
MUTE	5	D1

Video Decoder		
Video Decoder Pin Name	Video Decoder Pin Number	FPGA Pin Number
ISO	65	AC2
LLC1/PCLK	27	AB2
LLC2	26	AA3
P10	18	W1
P11	17	Y2
P12	8	Y1
P13	7	AA2
P14	6	AA1
P15	5	AB5
P16	76	AB4
P17	75	AB3
P18	74	AB1
P19	73	AC5
RESET_B	64	AC1
SCLOCK	68	AC4
SDATA	67	AC3
XTAL	29	AA4

Video Encoder		
Video Encoder Pin Name	Video Encoder Pin Number	FPGA Pin Number
BLANK_B	25	AP4
CLKIN	36	AP2
HSYNC_B	24	AN2
P0	1	AK4
P1	2	AK3
P2	3	AK2
P3	4	AK1
P4	5	AL4
P5	6	AL3
P6	7	AL2
P7	8	AL1
P8	9	AM4
P9	10	AM3
PAL_NTSC	59	AN4
RESET_B	60	AN3
SCL	39	AM2
SCRESET/RTC/TR	41	AP3
SDA	40	AM1
VSYNC_B	23	AN1



Xilinx, Inc.	2100 Logic Drive, San Jose, CA 95124	Drawn By: Daniel Postoian, Xilinx APD	
Title: UC Berkeley - FPGA Banks 2 & 3			
Size: C	Document Number		Rev: C.1
Date: Tuesday, July 22, 2003	Sheet 5 of 15		

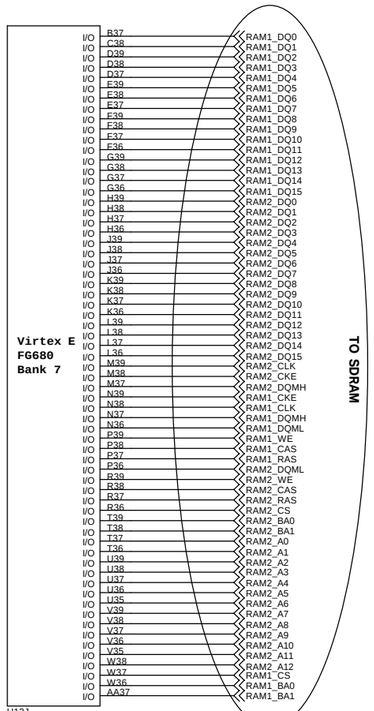
2003 CHANGES:

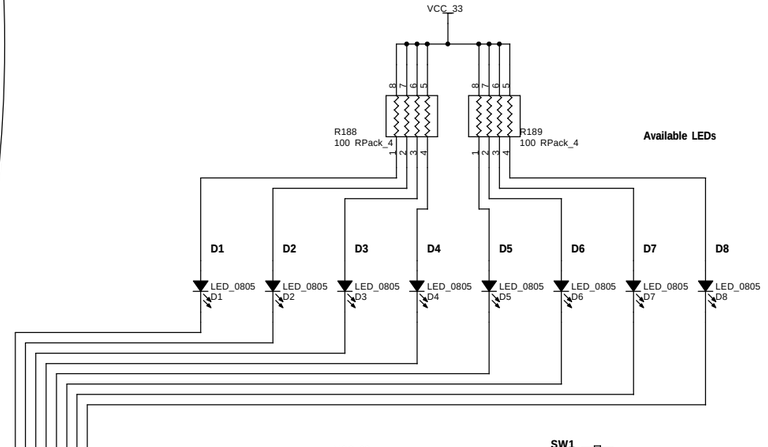
CHANGED PINOUT FOR SDRAM THROUGH SEPARATION OF ADDRESS BUS & CONTROL LINES

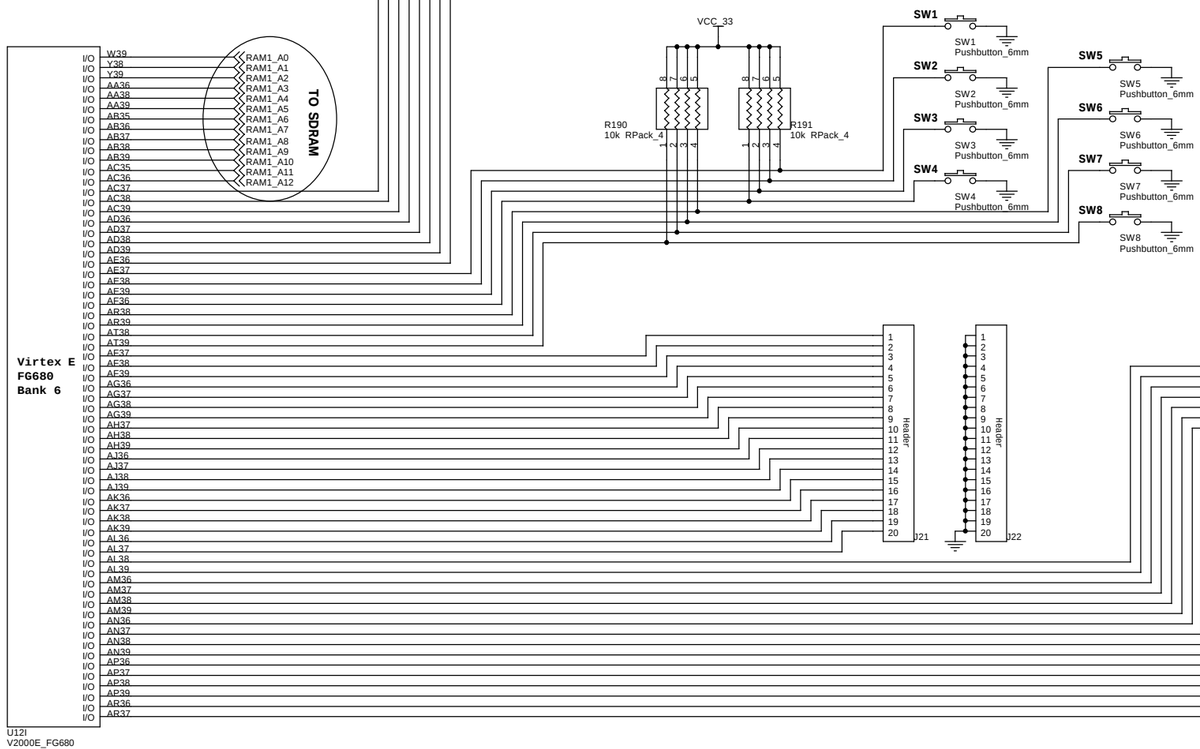
CHANGED PINOUT FOR LEDS

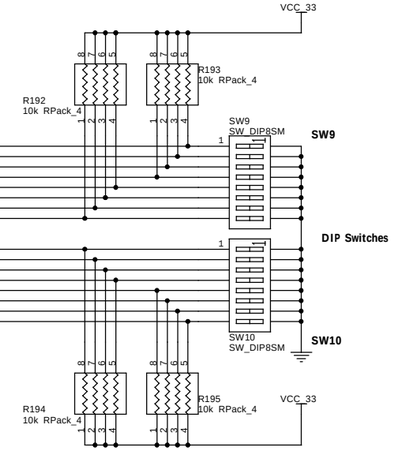
CHANGED PINOUT FOR DIP SWITCHES

CHANGED PINOUT FOR PUSHBUTTON SWITCHES









SDRAM FIRST CHIP [U6]

SDRAM Pin Name	SDRAM Pin Number	FPGA Pin Number
A0	23	W39
A1	24	Y38
A2	25	Y39
A3	26	AA36
A4	29	AA38
A5	30	AA39
A6	31	AB35
A7	32	AB36
A8	33	AB37
A9	34	AB38
A10	22	AB39
A11	35	AC35
A12	36	AC36
BA0	20	W36
BA1	21	AA37
CAS	17	P38
CKE	37	N39
CLK	38	N38
CS	19	W37
DQ0	2	B37
DQ1	4	C38
DQ2	5	D39
DQ3	7	D38
DQ4	8	D37
DQ5	10	E39
DQ6	11	E38
DQ7	13	E37
DQ8	42	F39
DQ9	44	F38
DQ10	45	F37
DQ11	47	F36
DQ12	48	G39
DQ13	50	G38
DQ14	51	G37
DQ15	53	G36
DQMH	39	N37
DQML	15	N36
RAS	18	P37
WE	16	P39

SDRAM SECOND CHIP [U7]

SDRAM Pin Name	SDRAM Pin Number	FPGA Pin Number
A0	23	T37
A1	24	T36
A2	25	U39
A3	26	U38
A4	29	U37
A5	30	U36
A6	31	U35
A7	32	V39
A8	33	V38
A9	34	V37
A10	22	V36
A11	35	V35
A12	36	W38
BA0	20	T39
BA1	21	T38
CAS	17	R38
CKE	37	M38
CLK	38	M39
CS	19	R36
DQ0	2	H39
DQ1	4	H38
DQ2	5	H37
DQ3	7	H36
DQ4	8	J39
DQ5	10	J38
DQ6	11	J37
DQ7	13	J36
DQ8	42	K39
DQ9	44	K38
DQ10	45	K37
DQ11	47	K36
DQ12	48	L39
DQ13	50	L38
DQ14	51	L37
DQ15	53	L36
DQMH	39	M37
DQML	15	P36
RAS	18	R37
WE	16	R39

LEDs (Active Low)

LED Number	FPGA Pin Number
D1	AC37
D2	AC38
D3	AC39
D4	AD36
D5	AD37
D6	AD38
D7	AD39
D8	AE36

DIP Switches (Active Low)

Switch Number	FPGA Pin Number
SW9-1	AL38
SW9-2	AL39
SW9-3	AM36
SW9-4	AM37
SW9-5	AM38
SW9-6	AM39
SW9-7	AN36
SW9-8	AN37
SW10-1	AN38
SW10-2	AN39
SW10-3	AP36
SW10-4	AP37
SW10-5	AP38
SW10-6	AP39
SW10-7	AR36
SW10-8	AR37

Pushbutton Switches (Active Low)

Switch Number	FPGA Pin Number
SW1	AE37
SW2	AE38
SW3	AE39
SW4	AF36
SW5	AR38
SW6	AR39
SW7	AT38
SW8	AT39

Xilinx, Inc. 2100 Logic Drive, San Jose, CA 95124 — Drawn By: Daniel Postoian, Xilinx APD

Title: **UC Berkeley - FPGA Bank 6 & 7**

Size: C — Document Number — Rev: **C.1**

Date: Tuesday, July 22, 2003 — Sheet 6 of 15

Ethernet Transceiver		
Transceiver Pin Name	Transceiver Pin Number	FPGA Pin Number
ADD2	18	C15
ADD3	19	D15
ADD4	20	A16
AUTOENA	111	C35
BYPSCR	113	B35
CFG_0	116	A36
CFG_1	115	B36
CFG_2	114	A35
COL0	37	B19
COL1	57	A23
COL2	75	A27
COL3	93	D32
CRS0	38	C19
CRS1	58	D24
CRS2	76	C28
CRS3	94	C32
FDE	110	D35
LED0_0	11	A14
LED0_1	12	B14
LED0_2	13	C14
LED1_0	8	B13
LED1_1	9	C13
LED1_2	10	D13
LED2_0	4	B12
LED2_1	5	C12
LED2_2	6	A13
LED3_0	1	C11
LED3_1	2	D11
LED3_2	3	A12
LEDCLK	15	D14
LEDDAT	16	A15
LEDENA	17	B15
MDC	99	D33
MDDIS	100	C33
MDINT	98	A32
MDIO	97	B32
PWRDN	102	B33
RESET	109	A34
RXD0_0	26	A17
RXD0_1	25	D16
RXD0_2	24	C16
RXD0_3	23	B16
RXD1_0	45	B21
RXD1_1	44	B20
RXD1_2	43	C21
RXD1_3	42	D19
RXD2_0	64	D25
RXD2_1	63	A24
RXD2_2	62	B24

Ethernet Transceiver (cont.)		
Transceiver Pin Name	Transceiver Pin Number	FPGA Pin Number
RXD2_3	61	C24
RXD3_0	82	C29
RXD3_1	81	D29
RXD3_2	80	A28
RXD3_3	79	B28
RX_CLK0	28	C17
RX_CLK1	47	E22
RX_CLK2	66	B25
RX_CLK3	84	A29
RX_DV0	27	B17
RX_DV1	46	A21
RX_DV2	65	C25
RX_DV3	83	B29
RX_ER0	29	D17
RX_ER1	48	D22
RX_ER2	67	A25
RX_ER3	85	D30
TRSTE0	106	B34
TRSTE1	105	C34
TRSTE2	104	D34
TRSTE3	103	A33
TX_CLK0	31	A18
TX_CLK1	50	B22
TX_CLK2	69	C26
TX_CLK3	87	B30
TXD0_0	33	C18
TXD0_1	34	D18
TXD0_2	35	E18
TXD0_3	36	A19
TXD1_0	52	E23
TXD1_1	53	D23
TXD1_2	54	C23
TXD1_3	55	B23
TXD2_0	71	A26
TXD2_1	72	D27
TXD2_2	73	C27
TXD2_3	74	B27
TXD3_0	89	D31
TXD3_1	90	C31
TXD3_2	91	B31
TXD3_3	92	A31
TX_EN0	32	B18
TX_EN1	51	A22
TX_EN2	70	B26
TX_EN3	88	A30
TX_ER0	30	E17
TX_ER1	49	C22
TX_ER2	68	D26
TX_ER3	86	C30

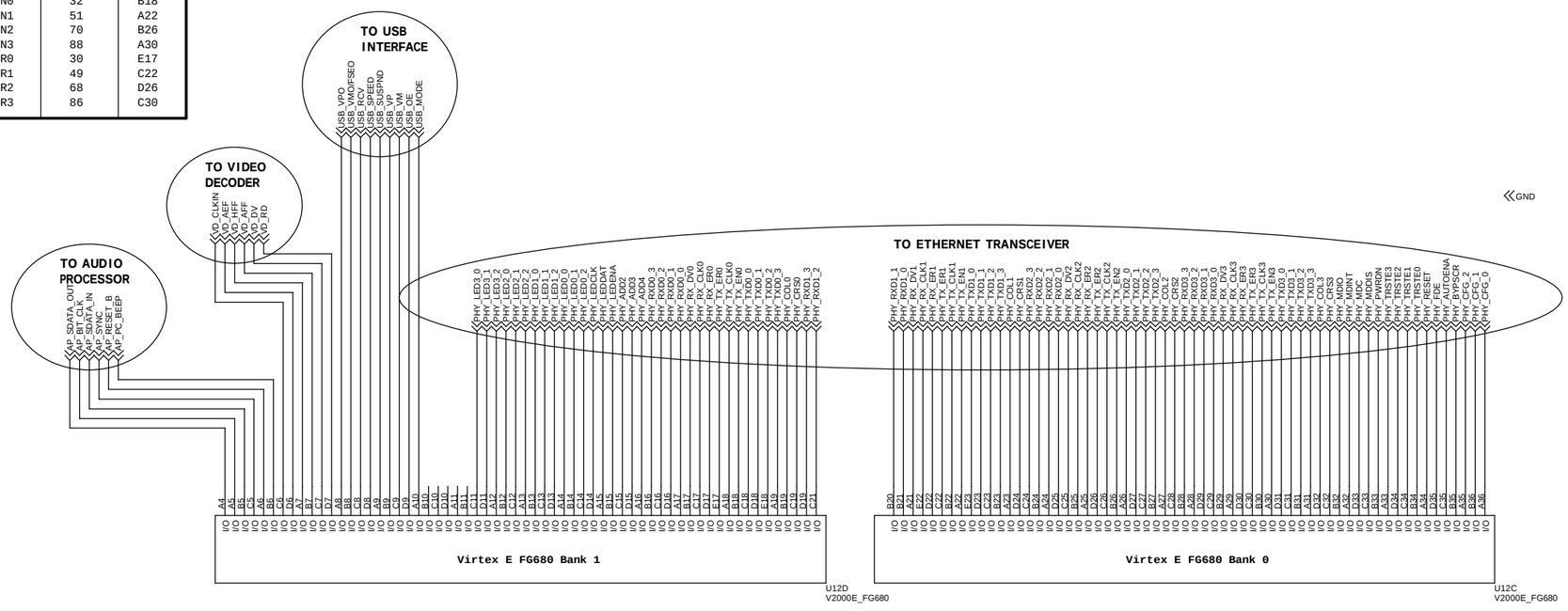
Audio Codec		
Codec Pin Name	Codec Pin Number	FPGA Pin Number
BIT_CLK	6	A5
PC_BEEP	12	B6
RESET_B	11	A6
SDATA_IN	8	B5
SDATA_OUT	5	A4
SYNC	10	C5

USB Interface		
USB Pin Name	USB Pin Number	FPGA Pin Number
MODE	1	A10
OE	2	D9
RCV	3	C8
SPEED	9	D8
SUSPND	6	A9
VM	5	C9
VMO/FSEO	13	B8
VP	4	B9
VPO	12	A8

Video Decoder		
Decoder Pin Name	Decoder Pin Number	FPGA Pin Number
AEF	13	D6
AFF	11	B7
CLKIN	16	C6
DV	78	C7
HFF	12	A7
RD	77	D7

2003 CHANGES:
ADDED VIDEO DECODER CONNECTIONS

ADDED USB INTERFACE CONNECTIONS



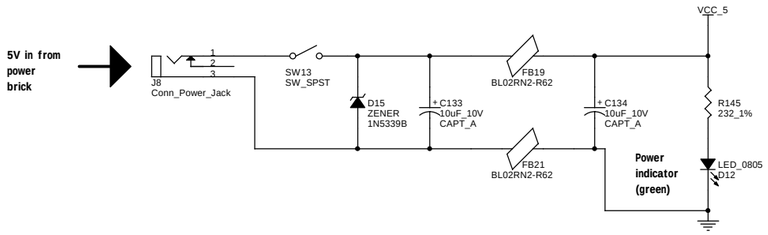
Xilinx, Inc. 2100 Logic Drive San Jose, CA 95124

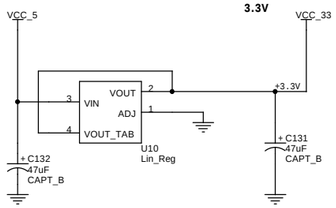
Drawn By: Daniel Postoian, Xilinx APD

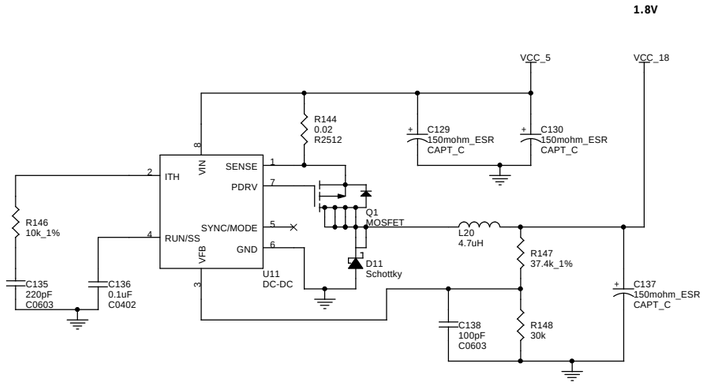
Title: UC Berkeley - FPGA Bank 0 & Bank 1

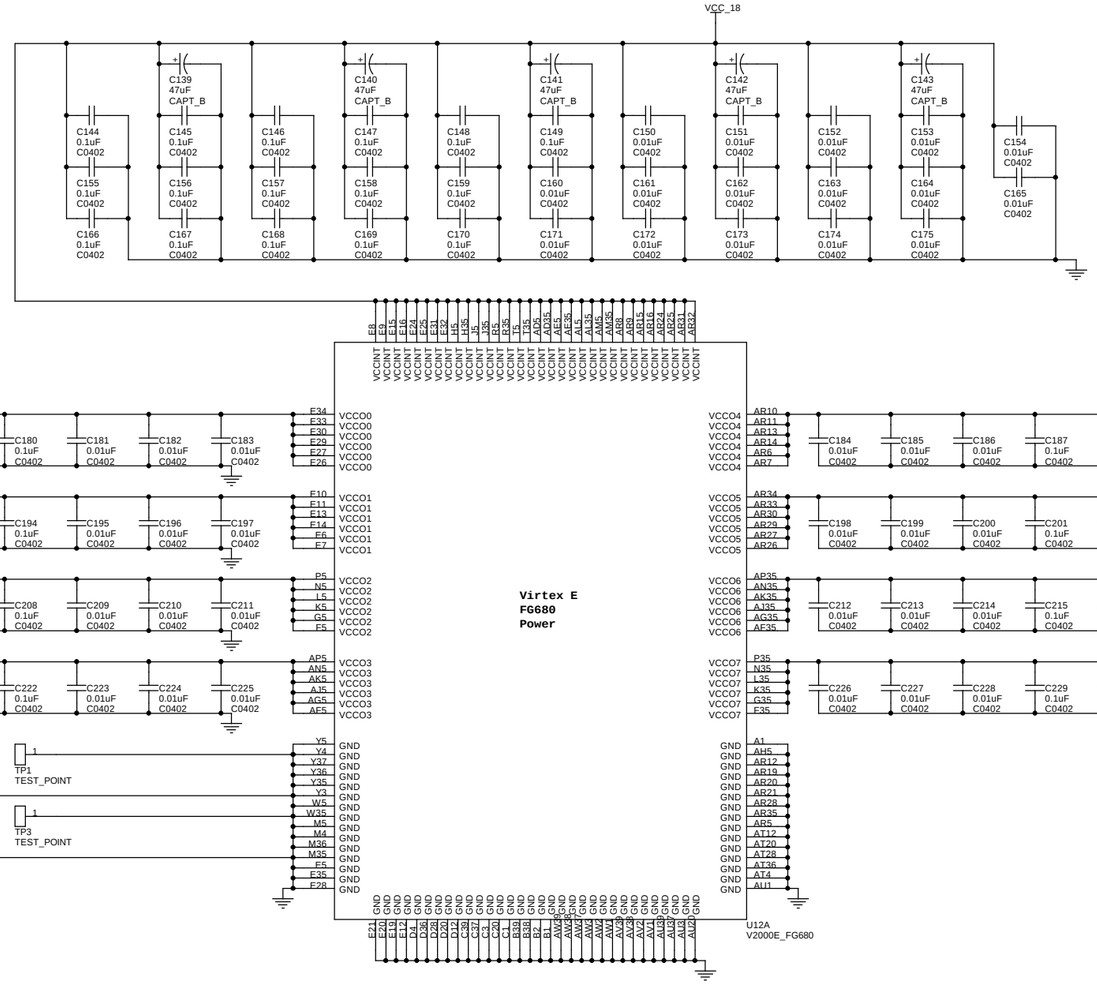
Size: C | Document Number | Rev: C.1

Date: Tuesday, July 22, 2003 | Sheet 7 of 15









Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn By: Daniel Postoian, Xilinx APD	
Title: **UC Berkeley - Power**			
Size: C	Document Number		Rev: **C.1**
Date: Tuesday, July 22, 2003	Sheet 8 of 15		

2003 CHANGES:

MADE ANTI-THEFT CABLE HOLES BIGGER

ADDED POWER AND GND STRIPS TO PROTO AREA

STANDOFF HOLES

X25
Standoff_Hole

X29
Standoff_Hole

X30
Standoff_Hole

X31
Standoff_Hole

ANTI-THEFT CABLE HOLES

X27
Antitheft_Hole

X26
Antitheft_Hole

VCC_33

VCC_5

PROTOTYPE AREA

Header 1 2 3 4 5 6 7 8 9 10 11 12 13 14

X44 X1 X8 X9 X17 X13 X21 X5 X6 X7 X11 X22 X2 X4 X16 X15 X18 X10 X19 X14 X3 X12 X20 X23 X24

VCC_5
VCC_33
GND

Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn By: Daniel Postoian, Xilinx APD	
Title: **UC Berkeley - Prototype Area & Standoffs**			
Size: C	Document Number		Rev: **C.1**
Date: Tuesday, July 22, 2003	Sheet 9 of 15		

NOTES:

ALL PHY_* OFF PAGE CONNECTORS GO TO FPGA BANKS 0 & 1.

VCCH, VCCT, VCCR are all the same 'analog' plane.

GNDH, GNDT, GNDA, GNDR are all the same GND.

Digital GND is regular board GND (GND to all other components).

DIGITAL/ANALOG SUPPLY

DIGITAL/ANALOG GROUND

TRANSMIT CENTERTAP FERRITE

BYPASS CAPS FOR PHY

DIGITAL GND

ANALOG GND

ANALOG SUPPLY

U8 Quad_E-net_Magnetics

U9 Quad_E-net_Xceiver_LXT975A

J6B Dual_High_RJ45_Right

J6A Dual_High_RJ45_Right

J7B Dual_High_RJ45_Left

J7A Dual_High_RJ45_Left

AS CLOSE TO PIN AS POSSIBLE (p42 datasheet)

Xilinx, Inc.	2100 Logic Drive, San Jose, CA 95124	Drawn By:	Daniel Postoian, Xilinx APD
Title: UC Berkeley - Quad Ethernet			
Size: C	Document Number		Rev: C.1
Date: Tuesday, July 22, 2003	Sheet 10 of 15		

2003 CHANGES:

SEPARATED ADDRESS BUS AND CONTROL LINES FOR EACH CHIP, AND ADDED TERMINATION RESISTORS AS APPROPRIATE

ADDED A12 LINE TO ALLOW FOR USE OF LARGER CAPACITY CHIPS

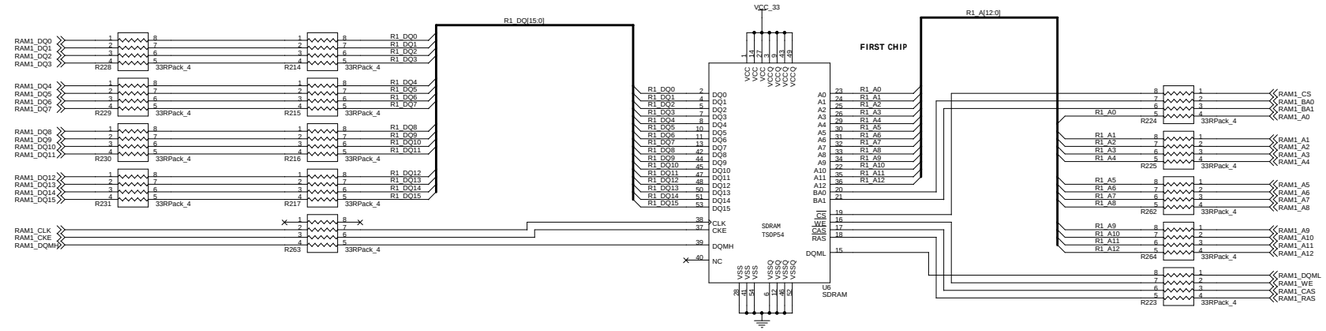
NOTES:

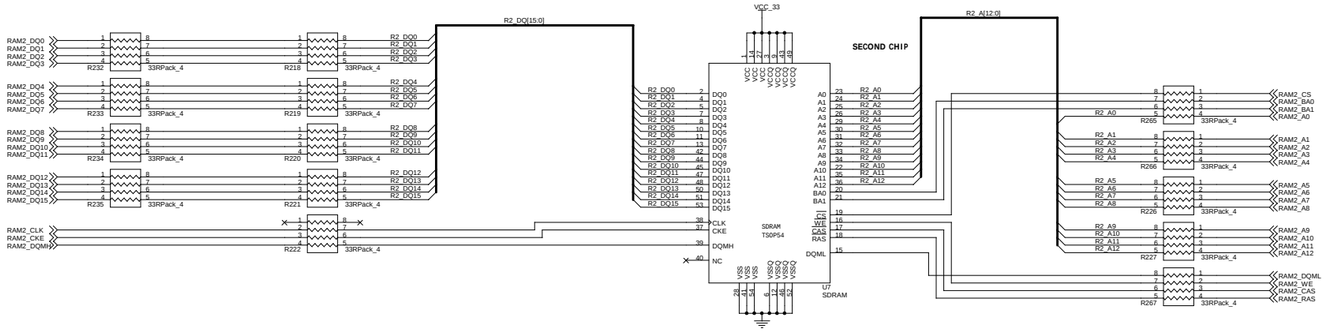
ALL RAM_* OFF PAGE CONNECTORS GO TO FPGA BANK 7.

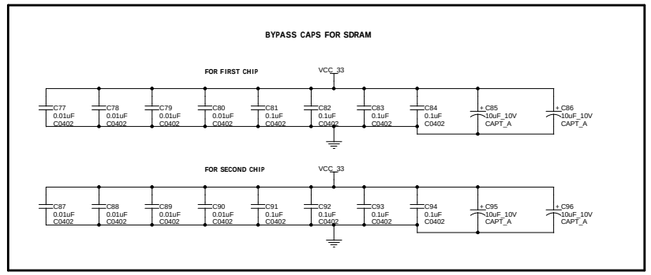
R214, R215, R216, R217 close to U6.

R218, R219, R220, R221 close to U7.

R222 through R235 close to FPGA.



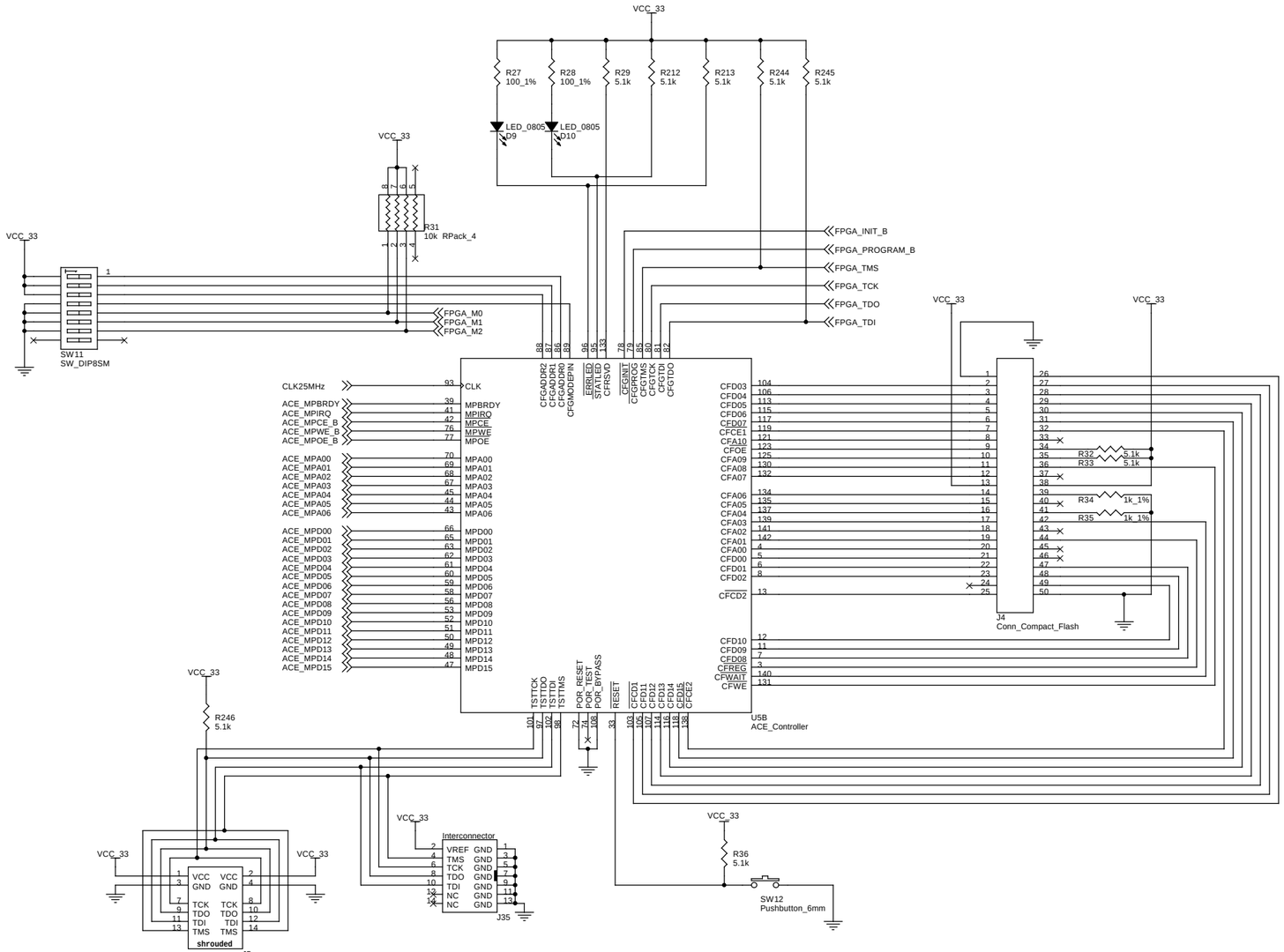


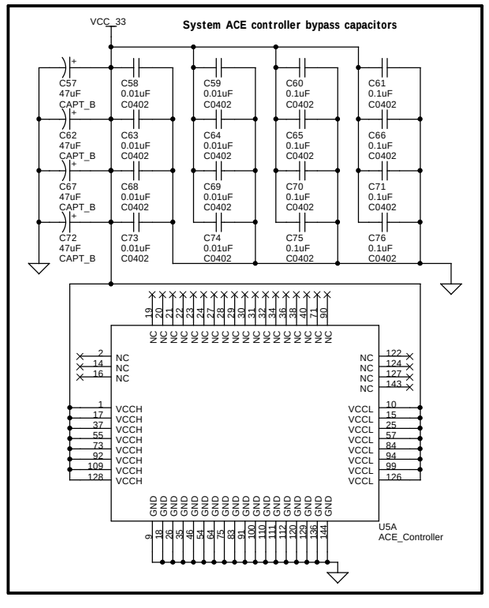


VCC_33
GND

Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn By: Daniel Postolan, Xilinx APD	
Title: UC Berkeley - SDRAM			
Size: D	Document Number		Rev: C.1
Date: Tuesday, July 22, 2003	Sheet 11 of 15		

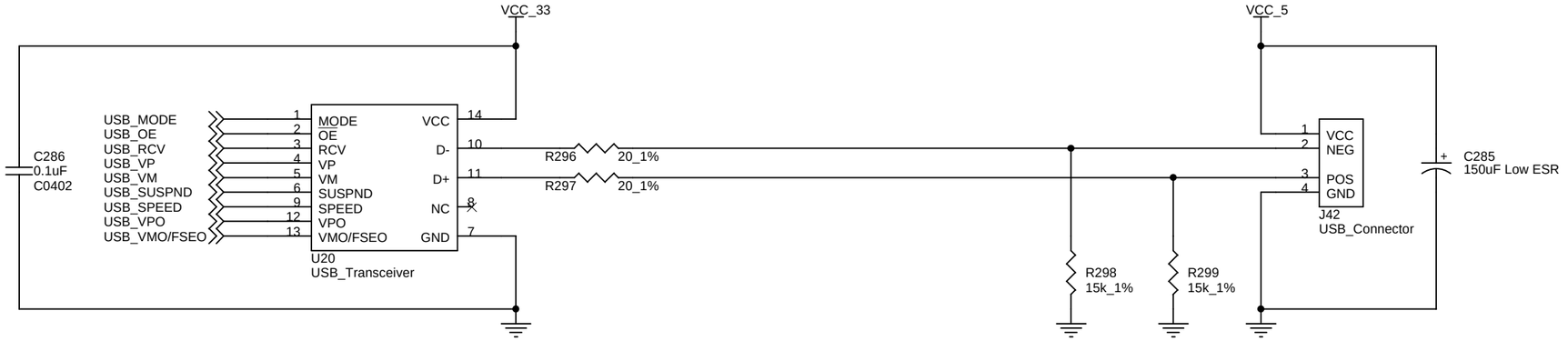
NOTES:
ALL ACE_* PINS GO TO FPGA BANK 2.





Xilinx, Inc.	2100 Logic Drive San Jose, CA 95124	Drawn By: Daniel Postoian, Xilinx APD	
Title: **UC Berkeley - System ACE / CompactFlash**			
Size: C	Document Number		Rev: **C.1**
Date: Tuesday, July 22, 2003	Sheet 12 of 15		

NOTES:
ALL USB_* PINS GO TO FPGA BANK 1.



VCC_5
VCC_33
GND

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Title: **UC Berkeley - USB**			
Size: B	Document Number		Rev: **C.1**
Date: Tuesday, July 22, 2003	Sheet 13 of 15		

2003 CHANGES:

CONNECTED FIFO SIGNALS TO FPGA [RD, DV, AEF, AFF, CLKIN, HFF/QCLK/GL]

REMOVED 0805 RESISTORS R9, R10, R12, R13, R14, R15, R16 & R17. REPLACED WITH (2) R-PACKS.

XTAL SIGNAL NOW COMES FROM DEDICATED FPGA PIN AND NOT A BRANCH OF CRYSTAL

ADDED ACCESS TO S-VIDEO INPUT

NOTES:

ALL VD_* OFF PAGE CONNECTORS GO TO FPGA BANKS 1, 2 & 3.

Composite Video In

Top 3 — J39A Conn_Video

Shield GND set on video encoder page (TV_GND)

CHAN1_COMP_VIDEO_IN — R11 75_1% R1206 — AVSS

C23 0.1uF C0402 — CHAN1_COMP

S-VIDEO PIN 3 — J41 Shield 2 1 4 3 6 5 — S-VIDEO PIN 4

CHAN1_LUMA_IN — R270 75_1% R1206 — AVSS

C277 0.1uF C0402 — CHAN1_Y

CHAN1_CHROMA_IN — R273 75_1% R1206 — AVSS

C278 0.1uF C0402 — CHAN1_C

42	AIN1	CHAN1_COMP
41	AIN_GND1	
44	AIN2	
43	AIN_GND2	
46	AIN3	
45	AIN_GND3	
58	AIN4	
57	AIN_GND4	
60	AIN5	CHAN1_Y
59	AIN_GND5	
62	AIN6	CHAN1_C
61	AIN_GND6	
51	REFOUT	
52	CML	
48	CAPY1	
49	CAPY2	
54	CAPC1	
55	CAPC2	
30	DVDD	
10	DVDD	
72	DVDD	
4	DVDDIO	
15	DVDDIO	
50	AVDD	
38	AVDD	
39	AVSS	
40	AVSS	
47	AVSS	
53	AVSS	
56	AVSS	
63	AVSS	
31	DVSS	
9	DVSS	
71	DVSS	
3	DVSSIO	
14	DVSSIO	

C24 10uF C1206, C25 0.1uF C0402, C26 0.1uF C0402 — AVSS

C27 0.1uF C0402, C28 10uF C1206, C29 0.1uF C0402 — AVSS

C30 0.1uF C0402 — AVSS

C35 0.1uF C0402, C36 10uF C1206, C37 0.1uF C0402, C38 0.1uF C0402 — AVSS

VCC_33 — C31 0.01uF C0402, C32 0.01uF C0402, C33 0.1uF C0402, C34 0.1uF C0402 — GND

VCC_5 — FB7 BLM31P601SG, FB8 BLM31P601SG — C39 33uF_10V CAPT_C, C40 10uF_10V CAPT_A, C41 0.01uF C0402, C42 0.1uF C0402 — GND / PVSS

PVDD

VCC_5 — FB9 BLM31P601SG, FB10 BLM31P601SG — C45 33uF_10V CAPT_C, C46 10uF_10V CAPT_A, C47 0.01uF C0402, C48 0.1uF C0402 — GND / AVSS

AVDD

VCC_33 — FB11 BLM31P601SG — C49 33uF_10V CAPT_C, C50 10uF_10V CAPT_A, C51 0.01uF C0402, C52 0.01uF C0402, C53 0.01uF C0402, C54 0.1uF C0402, C55 0.1uF C0402, C56 0.1uF C0402 — GND

DVDD

U4 Video_Decoder

P19	73	VD_P19
P18	74	VD_P18
P17	75	VD_P17
P16	76	VD_P16
P15	5	VD_P15
P14	6	VD_P14
P13	7	VD_P13
P12	8	VD_P12
P11	17	VD_P11
P10	18	VD_P10
P9	19	
P8	20	
P7	21	
P6	22	
P5	23	
P4	24	
P3	32	
P2	33	
P1	34	
P0	35	
XTAL1	28	
XTAL	29	VD_XTAL
SCLOCK	68	VD_SCLOCK
SDATA	67	VD_SDATA
RD	77	VD_RD
DV	78	VD_DV
OE	79	
VREF	69	
HREF	70	
LLCREF	25	
LLC2	26	VD_LLC2
LLC1/PCLK	27	VD_LLC1/PCLK
AEF	13	VD_AEF
HFF/QCLK/GL	12	VD_HFF
AFF	11	VD_AFF
CLKIN	16	VD_CLKIN
FIELD	80	
HS	2	
VS	1	
ISO	65	VD_ISO
RESET	64	VD_RESET_B
PWRDN	36	
ALSB	66	
ELPF	37	

R268 20RPack_4 — VD_P19, VD_P18, VD_P17, VD_P16

R269 20RPack_4 — VD_P15, VD_P14, VD_P13, VD_P12

R18 20_1%, R19 20_1% — VD_P11, VD_P10

VCC_33 — R20 3.32k_1%, R21 3.32k_1%

Decoded Video Data to FPGA

R260 20_1% — VD_XTAL — XTAL resistor should be at FPGA

R22 100_1% — VD_SCLOCK

R23 100_1% — VD_SDATA

R271 20_1% — VD_RD

R272 20_1% — VD_DV

R24 20_1% — VD_LLC2

R25 20_1% — VD_LLC1/PCLK

R274 20_1% — VD_AEF

R275 20_1% — VD_HFF

R276 20_1% — VD_AFF

R277 20_1% — VD_CLKIN — CLKIN resistor should be at FPGA

VCC_33 — GND

R26 5.62k_1%, C43 68pF C0603, C44 2.2nF_5% C0805 — PVDD

VCC_5
VCC_33
GND

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Title: **UC Berkeley - Video Decoder**

Size C | Document Number | Rev C.1

Date: Tuesday, July 22, 2003 | Sheet 14 of 15

NOTES:
ALL VE_* OFF PAGE CONNECTORS GO TO FPGA BANK 3.

2003 CHANGES:
ALTERED VE_CLKIN CONNECTION - NOW COMES STRAIGHT FROM FPGA INSTEAD OF BRANCHING FROM OSC.

ADDED AMPLIFIERS FOR COMPONENT VIDEO AND ROUTED THE OUTPUTS TO VIDEO HEADER REPLACING THE DAC OUTPUTS

Component Video Out Header
Do Not Stuff

Composite Video Out

S-Video Out

Processed Video Data from FPGA

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Sheet	15 of 15