2003 CHANGES:
MOVED Y5 FROM VIDEO ENCODER PAGE & CHANGED THE MANNER OF ITS CONNECTION SUCH THAT IT GOES SOLELY TO THE FPGA. THE OTHER PINS PREVIOUSLY DRIVEN BY Y5 ARE NOW TO BE DRIVEN BY FPGA I/O PINS.
2003 CHANGES:
- Made Anti-Theft Cable Holes BIGGER
- Added Power and GND Strips to Proto Area

UC Berkeley - Prototype Area & Standoffs
Date: Tuesday, July 22, 2003
2100 Logic Drive
San Jose, CA 95124

Drawn By: Daniel Postoian, Xilinx APD
Xilinx, Inc.
2003 CHANGES:
- CAPACITY CHIPS SEPARATED ADDRESS BUS AND CONTROL LINES FOR EACH
- RAM2 utility chip close to FPGA
- RAM1 utility chip close to U7
- Jumper used to disable one of the cards

UC Berkeley - SDRAM

Xilinx, Inc.
San Jose, CA 95124
2100 Logic Drive

Drawn By:
System ACE controller bypass capacitors

NOTES:
ALL ACE_* PINS GO TO FPGA BANK 2.
NOTES:
ALL USB_* PINS GO TO FPGA BANK 1.

UC Berkeley - USB

Xilinx, Inc.

NOTES:
ALL USB_* PINS GO TO FPGA BANK 1.
ADDED ACCESS TO S-VIDEO INPUT
CONNECTED FIFO SIGNALS TO FPGA [RD, DV, AND NOT A BRANCH OF CRYSTAL
XTAL SIGNAL NOW COMES FROM DEDICATED FPGA PIN
AND NOT A MANUFACTURED CRYSTAL
REMOVED 0805 RESISTORS R9, R10, R12, R13, R14,
REPLACED WITH (2) R-PACKS.

R15, R16 & R17. REPLACED WITH (2) R-PACKS.

CLKIN resistor should be at FPGA
XTAL resistor should be at FPGA

NOTES:

Date: Sheet
Size Document Number Rev
Title

BANKS 1, 2 & 3.

Decoded Video Data to FPGA

Daniel Postoian, Xilinx APD
Rick Ballantyne, Xilinx Labs
Drawn by:

Xilinx, Inc.
San Jose, CA 95124
2100 Logic Drive

14 15

UC Berkeley - Video Decoder

Xilinx, Inc.

15

C.1
2003 CHANGES:
- Signal path correction - has been altered from FPGA in lieu of branching from DAC.

Additional amplifiers for component video and routed from FPGA instead of branching from DAC.

ALTERED VE_CLKIN CONNECTION - Now comes straight from FPGA, all VE_* off page connectors go to FPGA bank 3.

NOTE: All Xilinx outputs go to FPGA bank 3.