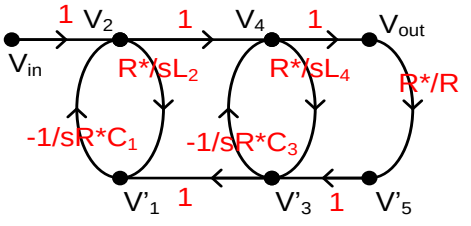
EE247
Lecture 14

- Administrative issues
  - Midterm exam postponed to **Thurs. Oct. 28th**
    - o You can *only* bring one 8x11 paper with your own written notes (please do not photocopy)
    - o No books, class or any other kind of handouts/notes, calculators, computers, PDA, cell phones....
    - o Midterm includes material covered to end of lecture 14

HW2
1st Problem

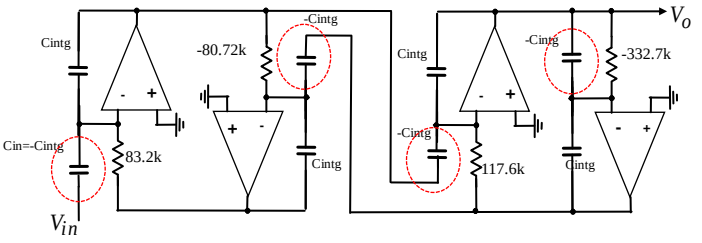
- 4th order highpass filter SFG



- Almost all have used one or two extra amplifiers for summing e.g. at node V4

HW2
1st Problem

- 4th order highpass filter implementation without use of extra summing amplifiers



- The four circled capacitors are used for summing of signals to eliminat need for extra amplifiers
  → save power dissipation and Si area , no additional noise

EE247
Lecture 14

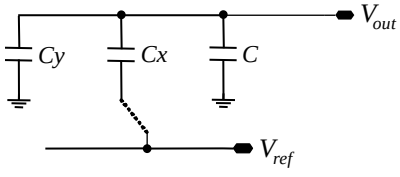
- D/A converters
  - D/A converters: Various Architectures (continued)
    - Charge scaling DACs
    - R-2R type DACs
    - Current based DACs
  - Static performance of D/As
    - Component matching
    - Systematic & random errors
  - Practical aspects of current-switched DACs
  - Segmented current-switched DACs
  - DAC dynamic non-idealities
  - DAC design considerations

Summary of Last Lecture

- Data Converters
  - Data converter testing (continued)
    - Dynamic tests
      - Spectral testing
      - Relationship between: DNL & SNR, INL & SFDR
    - Effective number of bits (ENOB)
  - D/A converters: Various Architectures
    - Resistor string DACs
    - Serial charge redistribution DACs

Parallel Charge Scaling DAC

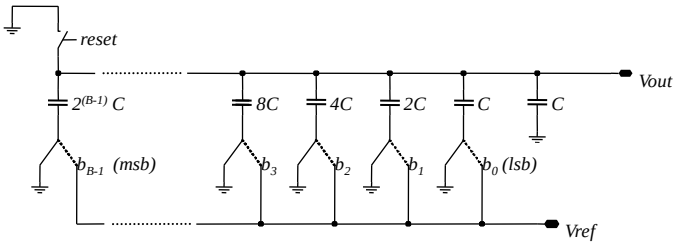
- DAC operation based on capacitive voltage division



$$V_{out} = \frac{Cx}{Cx+Cy+C} V_{ref}$$

→ Make *Cx* & *Cy* function of incoming DAC digital word

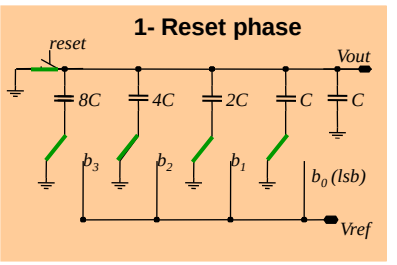
Parallel Charge Scaling DAC

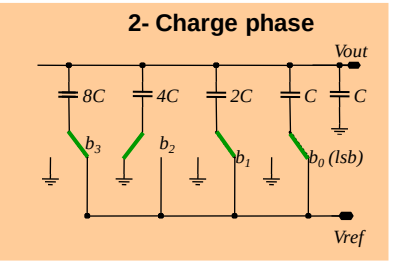


- E.g. "Binary weighted"
- B+1 capacitors & B switches (Cs built of unit elements → 2^B units of C)

$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C} V_{ref}$$

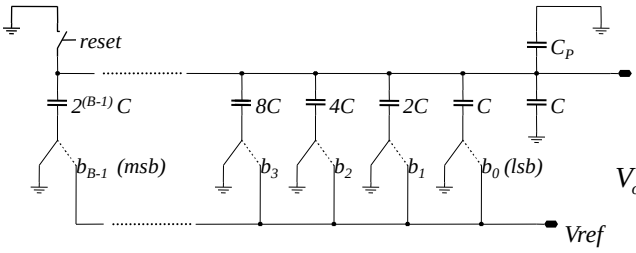
Charge Scaling DAC
Example: 4Bit DAC- Input Code 1011





$$V_{out} = \frac{2^0 C + 2^1 C + 2^3 C}{2^4 C} V_{ref} = \frac{11}{16} V_{ref}$$

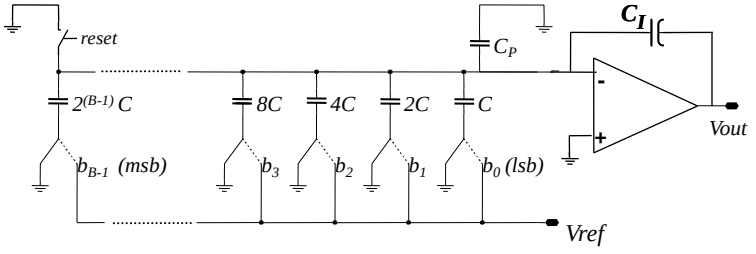
Charge Scaling DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C + C_P} V_{ref}$$

- Sensitive to parasitic capacitor @ output
  - If C_p constant → gain error
  - If C_p voltage dependant → DAC nonlinearity
- Large area of caps for high DAC resolution (10bit DAC ratio 1:512)

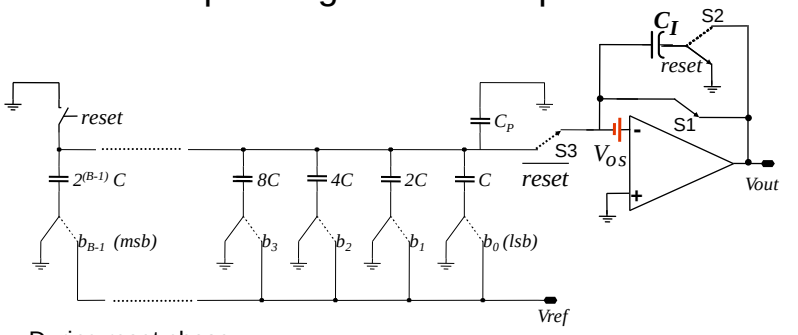
Parasitic Insensitive Charge Scaling DAC



$$V_{out} = -\frac{\sum_{i=0}^{B-1} b_i 2^i C}{C_I} V_{ref}, \quad C_I = 2^B C \rightarrow V_{out} = -\frac{\sum_{i=0}^{B-1} b_i 2^i}{2^B} V_{ref}$$

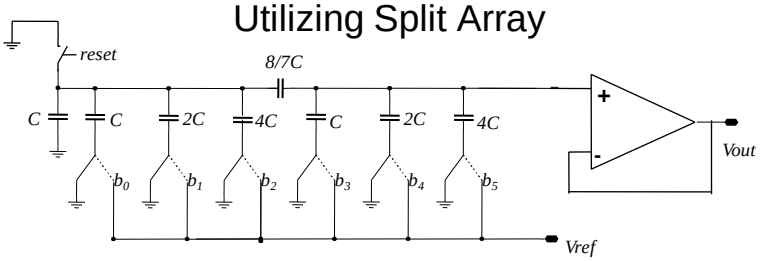
- Opamp helps eliminate the parasitic capacitor effect by producing virtual ground at the sensitive node since C_P has zero volts at start & end
  - Issue: opamp offset & speed- also double capacitor area

Charge Scaling DAC
Incorporating Offset Compensation



- During reset phase:
  - Opamp disconnected from capacitor array via switch S3
  - Opamp connected in unity-gain configuration (S1)
  - C_I Bottom plate connected to ground (S2)
  - $V_{out} \sim -V_{os} \rightarrow V_{CI} = -V_{os}$
- This effectively compensates for offset during normal phase

Charge Scaling DAC
Utilizing Split Array



$$C_{series} = \frac{\sum all\ LSB\ array\ C}{\sum all\ MSB\ array\ C} C$$

- Split array→ reduce the total area of the capacitors required for high resolution DACs
  - E.g. 10bit regular binary array requires 1024 unit Cs while split array (5&5) needs 64+~1 unit Cs
  - Issue: Sensitive to series capacitance parasitic capacitor

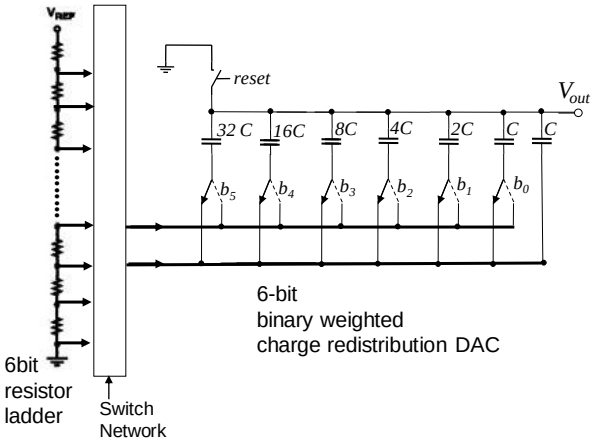
Charge Scaling DAC

- Advantages:
  - Low power dissipation → capacitor array does not dissipate DC power
  - Output is sample and held → no need for additional S/H
  - INL function of capacitor ratio
  - Possible to trim or calibrate for improved INL
  - Offset cancellation almost for free
- Disadvantages:
  - Process needs to include good capacitive material → not compatible with standard digital process
  - Requires large capacitor ratios
  - If binary-weighted Cs used then not inherently monotonic (more later)

Segmented DAC

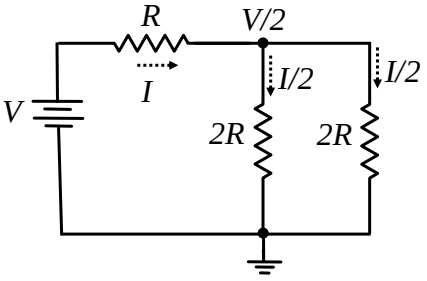
Resistor Ladder (MSB) & Binary Weighted Charge Scaling (LSB)

- Example: 12bit DAC
  - 6-bit MSB DAC→ R- string
  - 6-bit LSB DAC → binary weighted charge scaling
- Component count much lower compared to full R-string
  - Full R string→ 4096 resistors
  - Segmented → 64 R + 7 Cs (64 unit caps)



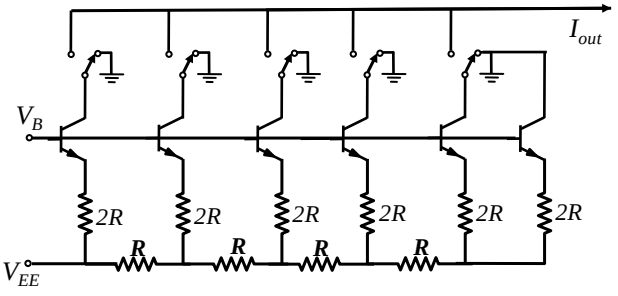
Current Based DACs
R-2R Ladder Type

- R-2R DAC basics:
  - Simple R network divides both voltage & current by 2



Increase # of bits by replicating circuit

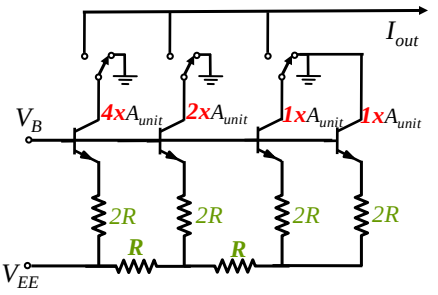
R-2R Ladder DAC



Emitter-follower added to convert to high output impedance current sources

R-2R Ladder DAC
How Does it Work?

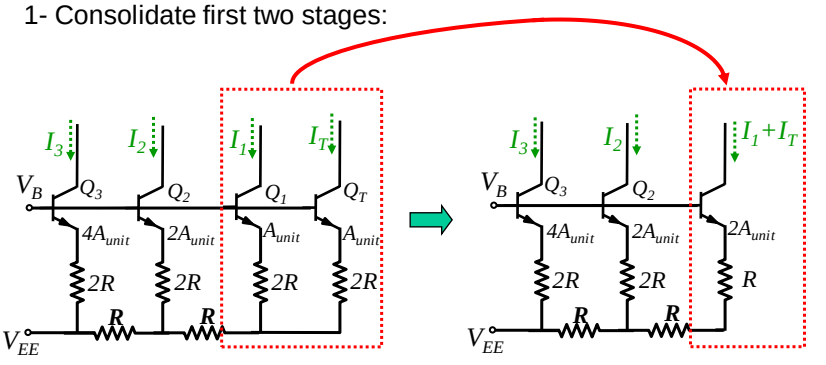
Consider a simple 3bit R-2R DAC:



R-2R Ladder DAC
How Does it Work?

Simple 3bit DAC:

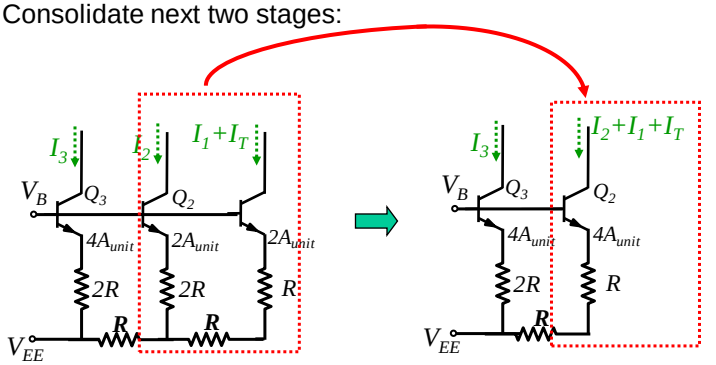
1- Consolidate first two stages:



R-2R Ladder DAC
How Does it Work?

Simple 3bit DAC-

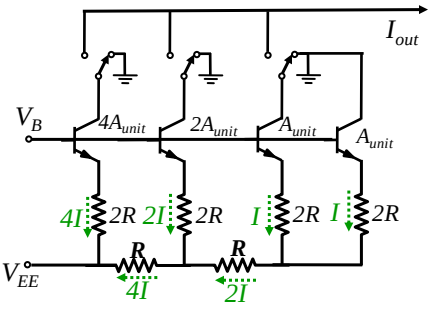
2- Consolidate next two stages:



$$I_3 = I_2 + I_1 + I_T \rightarrow I_3 = \frac{I_{Total}}{2}, I_2 = \frac{I_{Total}}{4}, I_1 = \frac{I_{Total}}{8}$$

R-2R Ladder DAC
How Does it Work?

Consider a simple 3bit R-2R DAC:

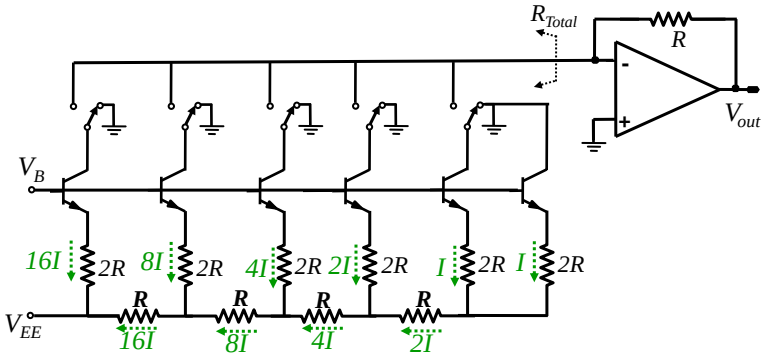


In most cases need to convert output current to voltage

Note that finite output resistance of the current sources causes gain error only

Ref: B. Razavi, "*Data Conversion System Design*", IEEE Press, 1995, page 84-87

R-2R Ladder DAC



Trans-resistance amplifier added to:

- Convert current to voltage
- Generate virtual ground @ current summing node so that output impedance of current sources do not cause error
- Issue: error due to opamp offset

R-2R Ladder DAC
Opamp Offset Issue

$$V_{os}^{out} = V_{os}^{in}\left(1+\frac{R}{R_{Total}}\right)$$

If $R_{Total} = large$,

$\rightarrow V_{os}^{out} \approx V_{os}^{in}$

If $R_{Total} = not\ large$

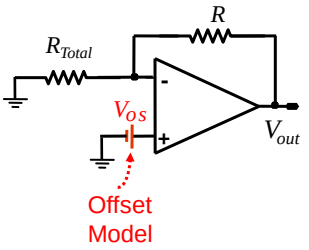
$$\rightarrow V_{os}^{out} = V_{os}^{in}\left(1+\frac{R}{R_{Total}}\right)$$

Problem:

Since R_{Total} *is code dependant*

$\rightarrow V_{os}^{out}$ *would be code dependant*

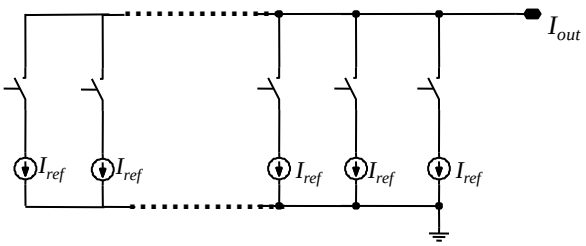
$\rightarrow$ *Gives rise to INL & DNL*



R-2R Ladder Summary

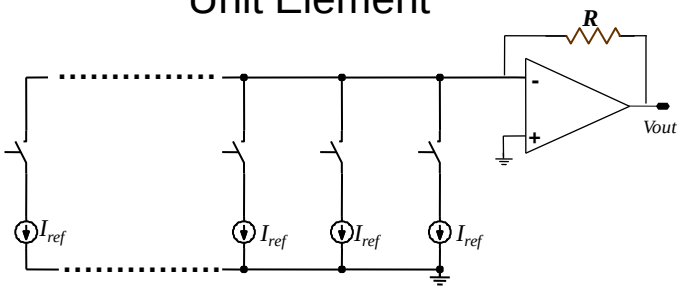
- Advantages:
  - Resistor ratios only x2
  - Does not require precision capacitors
  - Implemented both in BJT & MOS
- Disadvantages:
  - Total device emitter area → $A_E^{unit} x\ 2^B$
    → Not practical for high resolution DACs
  - INL/DNL error due to amplifier offset

Current based DAC Unit Element Current Source DAC



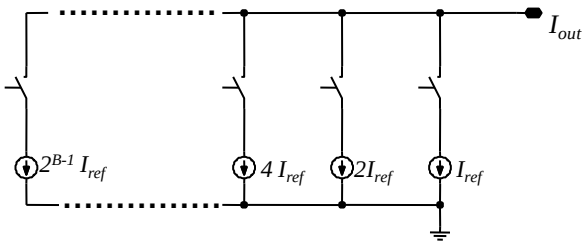
- "Unit elements" or thermometer
- 2^B-1 current sources & switches
- Suited for both MOS and BJT technologies
- Monotonicity does not depend on element matching and is guaranteed
- Output resistance of current source → gain error
  - Cascode type current sources higher output resistance → less gain error

Current Source DAC
Unit Element



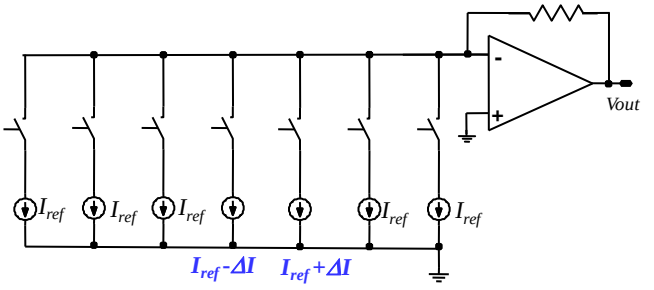
- Output resistance of current source → gain error problem
  →Use transresistance amplifier
  - Current source output held @ virtual ground
  - Error due to current source output resistance eliminated
  - New issues: offset & speed reduction due to amplifier bandwidth limitations

Current Source DAC
Binary Weighted



- "Binary weighted"
- B current sources & switches (2^B-1 unit current sources but less # of switches)
- Monotonicity depends on element matching →not guaranteed

Current Source DAC
DNL/INL Due to Element Mismatch



- Simplified example:
  - 3-bit DAC
  - Assume only two of the current sources mismatched (# 4 & #5)

Current Source DAC
DNL/INL Due to Element Mismatch

$$DNL[m] = \frac{segment[m] - V[LSB]}{V[LSB]}$$

$$DNL[4] = \frac{segment[4] - V[LSB]}{V[LSB]}$$

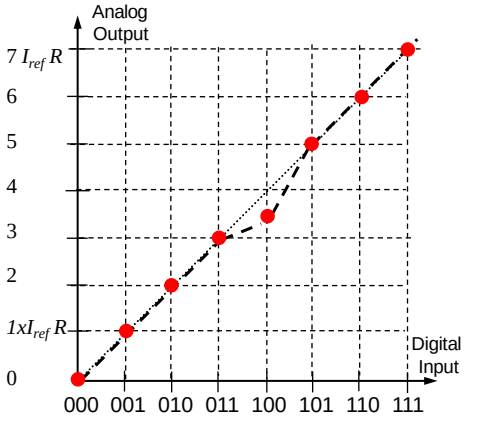
$$= \frac{(I - \Delta I)R - IR}{IR}$$

$$\boxed{DNL[4] = -\Delta I / I\ [LSB]}$$

$$DNL[5] = \frac{(I + \Delta I)R - IR}{IR}$$

$$\boxed{DNL[5] = \Delta I / I [LSB]}$$

$$\boxed{\rightarrow INL_{max} = -\Delta I / I\ [LSB]}$$



Static DAC Errors -INL / DNL

Static DAC errors mainly due to component mismatch

- Systematic errors
  - Contact resistance
  - Edge effects in capacitor arrays
  - Process gradients
  - Finite current source output resistance
- Random variations
  - Lithography etc…
  - Often Gaussian distribution (central limit theorem)

*Ref: C. Conroy et al, "Statistical Design Techniques for D/A Converters," JSSC Aug. 1989, pp. 1118-28.

Component Mismatch Probability Distribution Function

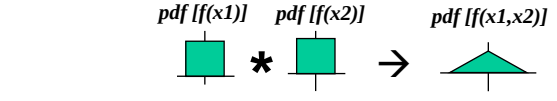
- **Component parameters → Random variables**

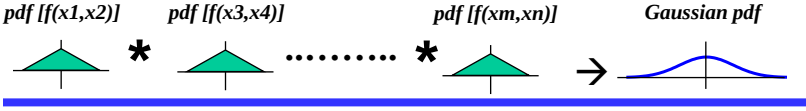
- **Each component is the product of many fabrication steps**
- **Most fabrication steps includes random variations**

→Overall component variations product of several random variables

→Assuming each of these variables have a uniform pdf distribution:

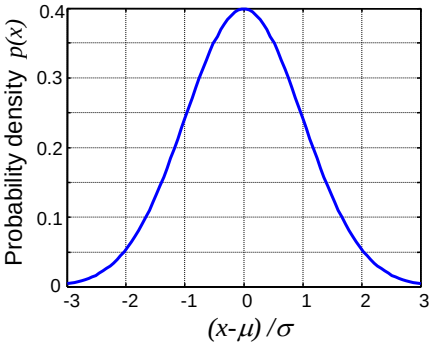
→Joint pdf of a random variable affected by two uniformly distributed variables → convolution of the two uniform pdfs…….





Gaussian Distribution

$$p(x)=\frac{1}{\sqrt{2\pi}\sigma}e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$



where:
μ *is the expected value and*
standard deviation : $\sigma=\sqrt{E(X^2)-\mu^2}$
$\sigma^2 \rightarrow$ *variance*

Yield

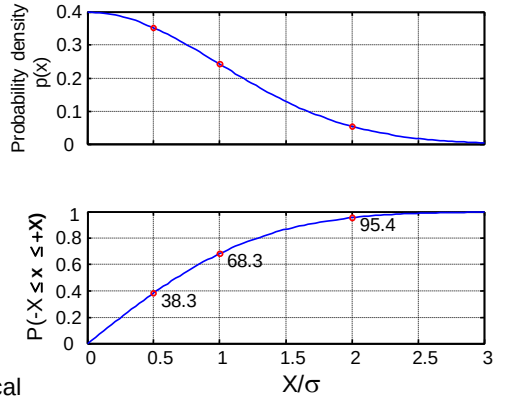
In most cases we are interested in finding the percentage of components (e.g. R) falling within certain bounds around a mean value μ

$$P(-X \le x \le +X)=$$

$$=\frac{1}{\sqrt{2\pi}}\int_{-X}^{+X} e^{-\frac{x^2}{2}}dx$$

$$=erf\left(\frac{X}{\sqrt{2}}\right)$$

Integral has no analytical solution → found by numerical methods



Yield

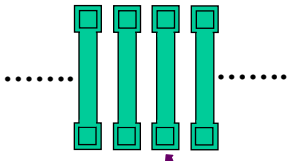
X/σ	P(-X ≤ x ≤ X) [%]	X/σ	P(-X ≤ x ≤ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

Example

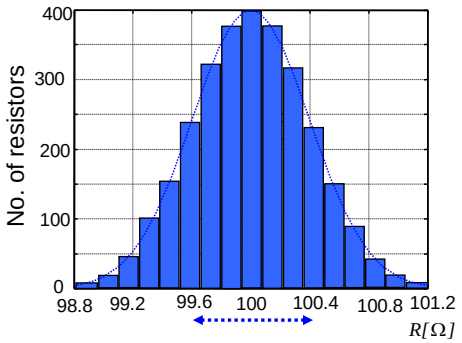
- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with σ = 2mV and μ = 0.
- Find the fraction of opamps with $|V_{os}| <$ 6mV:
  - $X/\sigma = 3$ → 99.73 % yield
- Fraction of opamps with $|V_{os}| <$ 400μV:
  - $X/\sigma = 0.2$ → 15.85 % yield

Component Mismatch

Example: Resistors layouted out side-by-side



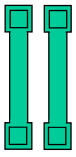
After fabrication large # of devices measured & graphed → typically if sample size large shape is Gaussian



E.g. Let us assume in this example 1000 Rs measured
& 68.5% fall within +-0.4OHM or +-0.4% of average
→ 1σ for resistors→ 0.4%

Component Mismatch

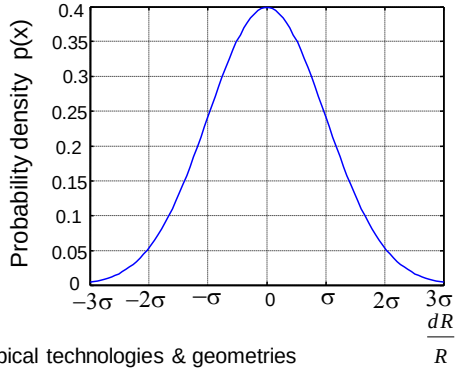
Example: Two resistors layouted out side-by-side



$$R = \frac{R_1 + R_2}{2}$$

$$dR = R_1 - R_2$$

$$\sigma^2_{\frac{dR}{R}} \propto \frac{1}{Area}$$



For typical technologies & geometries
1σ for resistors → *0.02 to 5%*

In the case of resistors σ is a function of area

DNL Unit Element DAC

E.g. Resistor string DAC:
Assumption: No systematic error- only random error

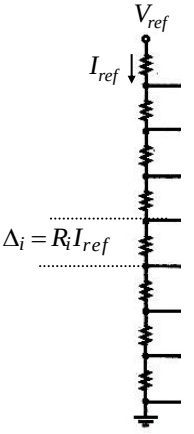
$$\Delta = R_{median}\, I_{ref} \quad where \quad R_{median} = \frac{\sum_{o}^{2^B-1} R_i}{2^B}$$

$$\Delta_i = R_i I_{ref}$$

$$DNL_i = \frac{\Delta_i - \Delta_{median}}{\Delta_{median}}$$

$$= \frac{R_i - R_{median}}{R_{median}} = \frac{dR}{R_{median}} \approx \frac{dR}{R_i}$$

$$\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}$$



To first order → DNL of unit element DAC is independent of resolution!
Note: Similar results for other unit-element based DACs

DNL Unit Element DAC

E.g. Resistor string DAC:

$$\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}$$

Example:

If $\sigma_{dR/R}$ = 0.4%, what DNL spec goes into the unit-element DAC datasheet so that 99.9% of all converters meet the spec?

Yield

X/σ	P(-X ≤ x ≤ X) [%]	X/σ	P(-X ≤ x ≤ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

DNL Unit Element DAC

E.g. Resistor string DAC:

$$\sigma_{DNL} = \sigma_{\frac{dR_i}{R_i}}$$

Example:

If $\sigma_{dR/R}$ = 0.4%, what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

Answer:

From table or Matlab: for 99.9%

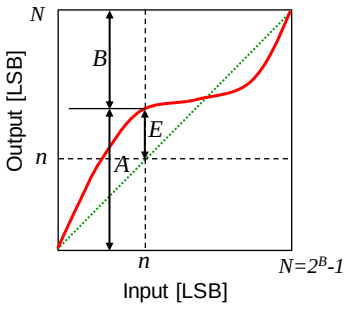
→ X/σ = 3.3

$\sigma_{DNL} = \sigma_{dR/R}$ = 0.4%

3.3 σ_{DNL} = 3.3x0.4%=1.3%

→DNL= +/- 0.013 LSB

DAC INL Analysis



	Ideal	Variance
$A=n+E$	n	$n.\sigma_\varepsilon^2$
$B=N-n-E$	$N-n$	$(N-n).\sigma_\varepsilon^2$

$E = A-n \quad r = n/N \quad N=A+B$

$= A-r(A+B)$

$= (1-r).A - r.B$

→ *Variance of E:*

$\sigma_E^2 = (1-r)^2 .\sigma_A^2 + r^2 .\sigma_B^2$

$= N.r.(1-r).\sigma_\varepsilon^2 = n.(1-n/N).\sigma_\varepsilon^2$

DAC INL

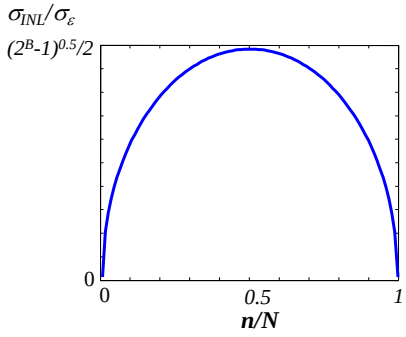
$$\sigma_E^2 = n\left(1-\frac{n}{N}\right)\times\sigma_\varepsilon^2$$

$$To\ find\ max.\ variance: \quad \frac{d\sigma_E^2}{dn}=0$$

$$\rightarrow n = N/2 \rightarrow \sigma_E^2 = \frac{N}{4}\times\sigma_\varepsilon^2$$

- Error is maximum at mid-scale ($N/2$):

$$\sigma_{INL}^{max} = \frac{1}{2}\sqrt{2^B-1}\,\sigma_\varepsilon \quad with \quad N=2^B-1$$



- INL depends on both DAC resolution & element matching σ_ε
- While $\sigma_{DNL} = \sigma_\varepsilon$ is to first order independent of DAC resolution and is only a function of element matching

Ref: Kuboki et al, TCAS, 6/1982

Untrimmed DAC INL

Example:

Assume the following requirement for a DAC:

$$\sigma_{INL} \cong \frac{1}{2}\sqrt{2^B - 1}\ \sigma_\varepsilon$$

$\sigma_{INL} = 0.1\ LSB$

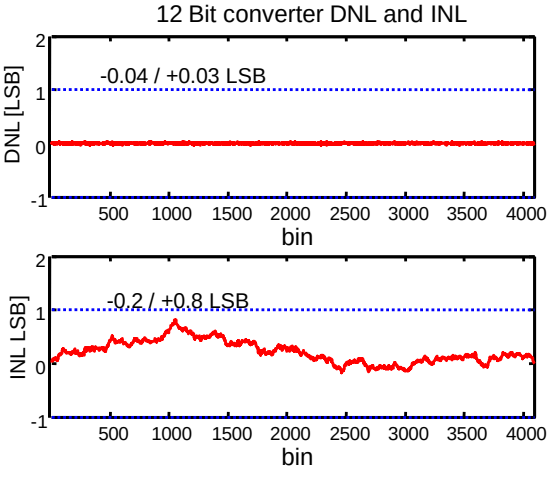
Find maximum resolution for:

$$B \cong 2 + 2\log_2\left[\frac{\sigma_{INL}}{\sigma_\varepsilon}\right]$$

$$\sigma_\varepsilon = 1\% \rightarrow B_{max} = 8.6bits$$
$$\sigma_\varepsilon = 0.5\% \rightarrow B_{max} = 10.6bits$$
$$\sigma_\varepsilon = 0.2\% \rightarrow B_{max} = 13.3bits$$
$$\sigma_\varepsilon = 0.1\% \rightarrow B_{max} = 15.3bits$$

Note: In most cases, a number of systematic errors prevents achievement of above results

Simulation Example



σ_ε = 1%
B = 12
Random # generator used in MatLab

Computed INL:
σ_{INL}^{max} = 0.32 LSB (midscale)

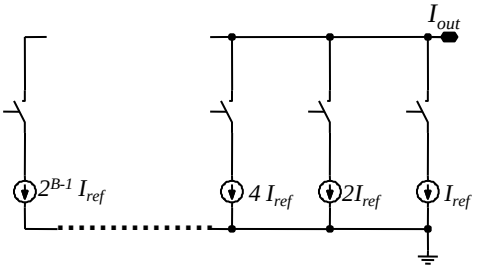
Why is the results not as expected per our derivation?

INL & DNL for Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
  - Example:

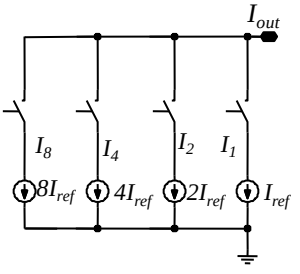
    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dI/I)}^2$

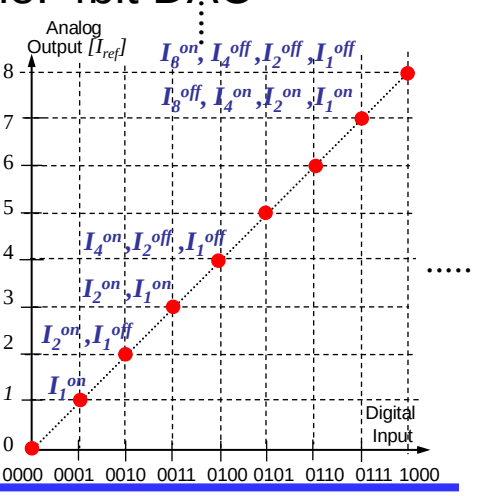
    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dI/I)}^2$



- Consider MSB transition:
  0111 … → 1000 …

DAC DNL
Example: 4bit DAC



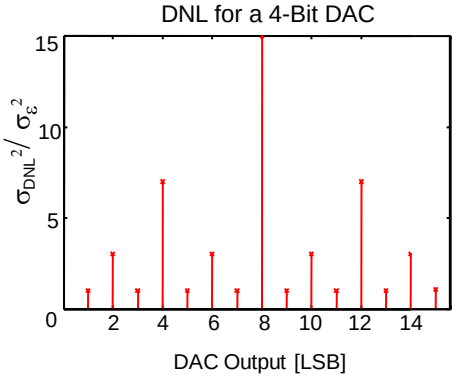


- DNL depends on transition
  - Example:

    0 to 1 → $\sigma_{DNL}^2 = \sigma_{(dIref/Iref)}^2$

    1 to 2 → $\sigma_{DNL}^2 = 3\sigma_{(dIref/Iref)}^2$

Binary Weighted DAC DNL



- Worst-case transition occurs at mid-scale:

$$\sigma_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)\sigma_\varepsilon^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)\sigma_\varepsilon^2}_{1000\ldots}$$

$$\cong 2^B\sigma_\varepsilon^2$$

$$\sigma_{DNL_{max}} = 2^{B/2}\sigma_\varepsilon$$

$$\sigma_{INL_{max}} \cong \frac{1}{2}\sqrt{2^B-1}\,\sigma_\varepsilon \cong \frac{1}{2}\sigma_{DNL_{max}}$$

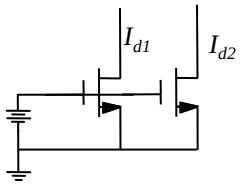
- Example:
  B = 12, σ_ε = 1%
  → σ_{DNL} = 0.64 LSB
  → σ_{INL} = 0.32 LSB

MOS Current Source Variations Due to Device Matching Effects

$$I_d = \frac{I_{d1}+I_{d2}}{2}$$

$$\frac{dI_d}{I_d} = \frac{I_{d1}-I_{d2}}{I_d}$$

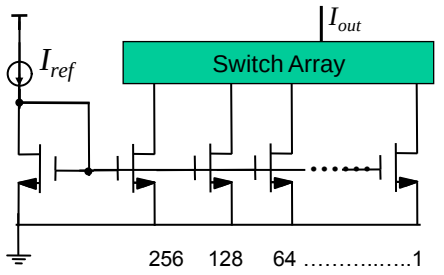
$$\frac{dI_d}{I_d} = \frac{d{}^{W}\!/_{L}}{{}^{W}\!/_{L}} + \frac{2\times dV_{th}}{V_{GS}-V_{th}}$$



- Current matching depends on:
  - Device W/L ratio matching
    → Larger device area less mismatch effect
  - Current mismatch due to threshold voltage variations:
    → Larger gate-overdrive less threshold voltage mismatch effect

Current-Switched DACs in CMOS

$$\frac{dI_d}{I_d} = \frac{d\,W/L}{W/L} + \frac{2dV_{th}}{V_{GS}-V_{th}}$$



Example: 8bit Binary Weighted

- Advantages:
  - Can be very fast
  - Reasonable area for resolution < 9-10bits
- Disadvantages:
  - Accuracy depends on device W/L & V_{th} matching

Unit Element versus Binary Weighted DAC

Unit Element DAC	Binary Weighted DAC
$\sigma_{DNL} = \sigma_\varepsilon$	$\sigma_{DNL} \cong 2^{B/2}\sigma_\varepsilon = 2\sigma_{INL}$
$\sigma_{INL} \cong 2^{B/2-1}\sigma_\varepsilon$	$\sigma_{INL} \cong 2^{B/2-1}\sigma_\varepsilon$

Number of switched elements:

$S = 2^B$	$S = B$

Key point: Significant difference in performance and complexity!

Unit Element versus Binary Weighted DAC
Example: B=10

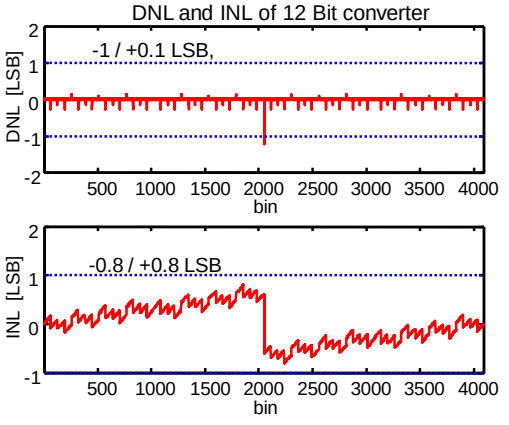
Unit Element DAC	Binary Weighted DAC
$\sigma_{DNL} = \sigma_\varepsilon$	$\sigma_{DNL} \cong 2^{B/2}\sigma_\varepsilon = 32\sigma_\varepsilon$
$\sigma_{INL} \cong 2^{B/2-1}\sigma_\varepsilon = 16\sigma_\varepsilon$	$\sigma_{INL} \cong 2^{B/2-1}\sigma_\varepsilon = 16\sigma_\varepsilon$

Number of switched elements:

$S = 2^B = 1024$	$S = B = 10$

Significant difference in performance and complexity!

"Another" Random Run …

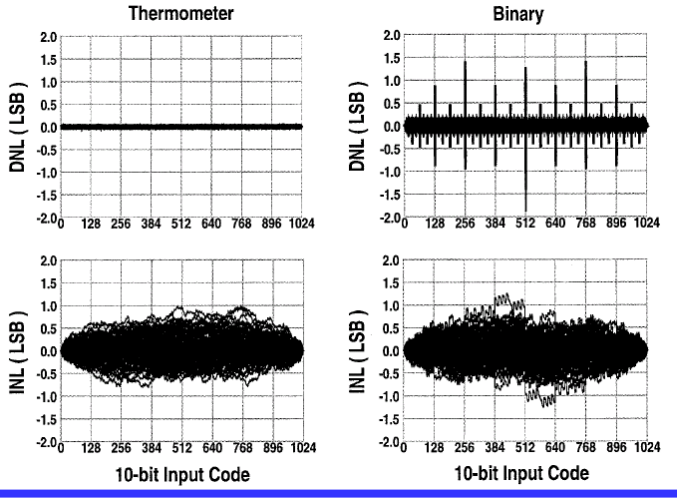


Now (by chance) worst DNL is mid-scale.

Close to statistical result!

10Bit DAC DNL/INL Comparison
Plots: 100 Matlab Simulation Runs Overlaid

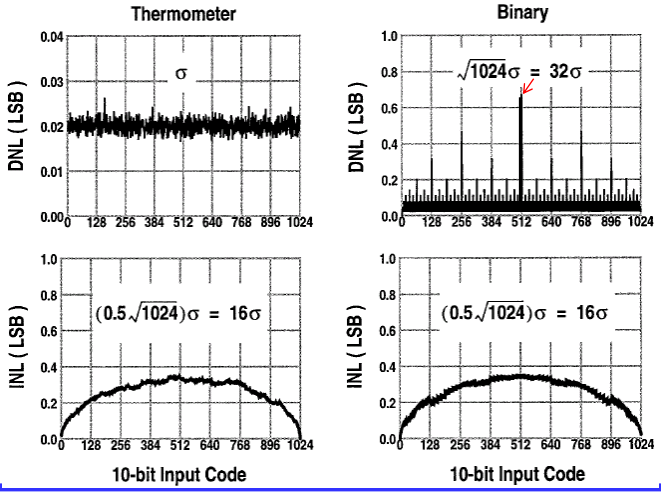
Ref: C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948 - 1958, December 1998.



Note: σ_ε=2%

10Bit DAC DNL/INL Comparison
Plots: RMS for 100 Simulation Runs

Ref: C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948 - 1958, December 1998.



Note: σ_ε=2%

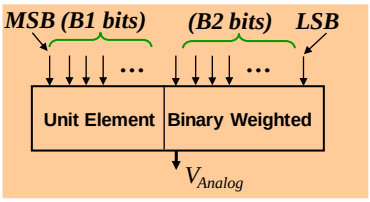
DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results assume uncorrelated random element variations
- Systematic errors and correlations are usually also important and may affect final DAC performance

Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. IEEE Transactions on Circuits and Systems, vol.CAS-29, (no.6), June 1982. p.383-9.

Segmented DAC
Combination of Unit-Element & Binary-Weighted

- Objective:
  Compromise between unit-element and binary-weighted DAC



$B_{Total} = B_1 + B_2$

- Approach:
  B_1 MSB bits → unit elements
  B_2 LSB bits → binary weighted
- INL: unaffected same as either architecture
- DNL: Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with (B_2+1) # of bits
- Number of switched elements: $(2^{B1}-1) + B_2$

Comparison

Example:

$B = 12,\ B_1 = 5,\ B_2 = 7$

$\underbrace{B_1 = 6}_{\text{MSB}},\ \underbrace{B_2 = 6}_{\text{LSB}}$

$$\sigma_{DNL} \cong 2^{(B_2+1)/2}\sigma_\varepsilon = 2\sigma_{INL}$$

$$\sigma_{INL} \cong 2^{B/2-1}\sigma_\varepsilon$$

$$S = 2^{B1} - 1 + B_2$$

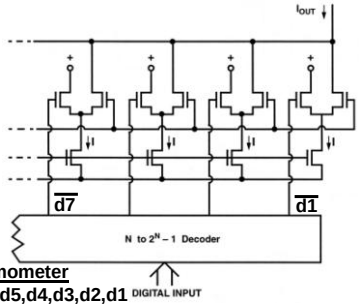
Assuming: $\sigma_\varepsilon = 1\%$

DAC Architecture (B1+B2)	$\sigma_{INL[LSB]}$	$\sigma_{DNL[LSB]}$	# of switched elements
Unit element (12+0)	*0.32*	*0.01*	*4095*
Segmented (6+6)	*0.32*	*0.113*	*63+6=69*
Segmented (5+7)	*0.32*	*0.16*	*31+7=38*
Binary weighted (0+12)	*0.32*	*0.64*	*12*

Practical Aspects
Current-Switched DACs

- Unit element DACs ensure monotonicity by turning on equal-weighted current sources in succession
- Typically current switching performed by differential pairs
- For each diff pair, only one of the devices are on→ switch device mismatch not an issue
- Issue: While binary weighted DAC can use the incoming binary digital word directly, unit element requires a decoder

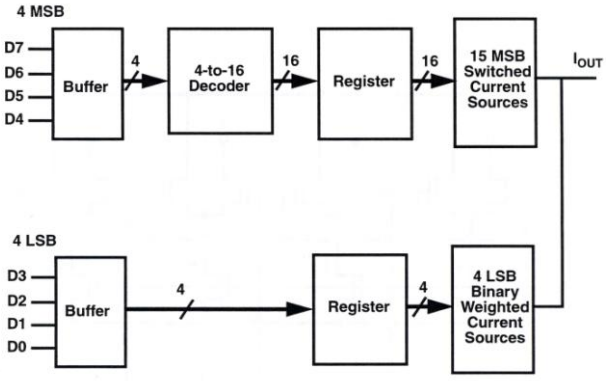
→ N to (2^N-1) decoder



Binary b2,b1,b0	Thermometer d7,d6,d5,d4,d3,d2,d1
000	0000000
001	0000001
010	0000011
011	0000111
100	0001111
101	0011111
110	0111111
111	1111111

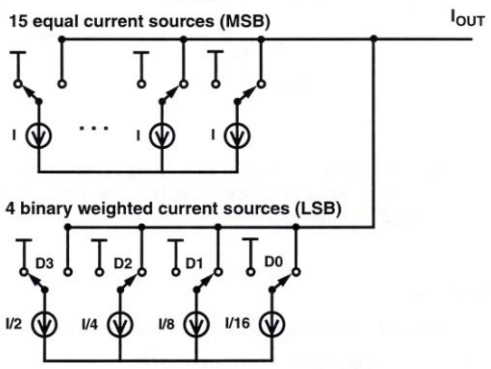
Segmented Current-Switched DAC Example: 8bit→4MSB+4LSB

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register



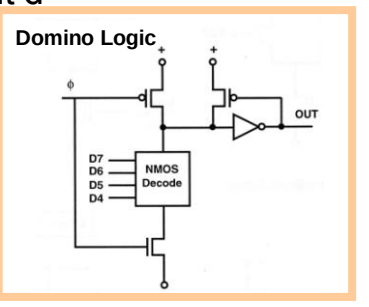
Segmented Current-Switched DAC Cont'd

- 4-bit MSB Unit element DAC + 4-bit binary weighted DAC
- Note: 4-bit MSB DAC requires extra 4-to-16 bit decoder
- Digital code for both DACs stored in a register

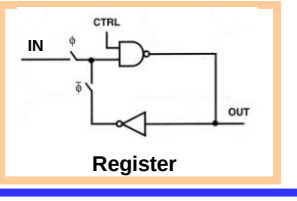


Segmented Current-Switched DAC Cont'd

- MSB Decoder
  - →Domino logic
  - →Example: D4,5,6,7=1 OUT=1

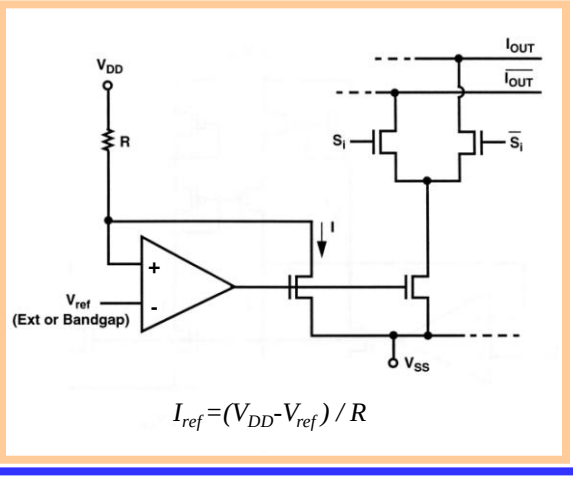


- Register
  - → Latched NAND gate:
  - → CTRL=1 OUT=INB



Segmented Current-Switched DAC Reference Current Considerations

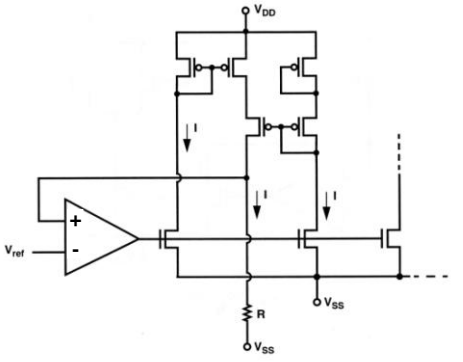
- I_{ref} is referenced to V_{DD}
  - → Problem: Reference current varies with supply voltage



$$I_{ref}=(V_{DD}-V_{ref})/R$$

Segmented Current-Switched DAC Reference Current Considerations

- I_{ref} is referenced to V_{ss}→GND



$$I_{ref} = (V_{ref} - V_{ss}) / R$$

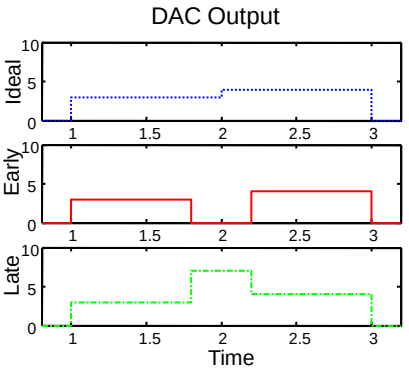
$V_{ss} \rightarrow 0$

DAC Dynamic Non-Idealities

- Finite settling time
  - Linear settling issues: (e.g. RC time constants)
  - Slew limited settling
- Spurious signal coupling
  - Coupling of clock/control signals to the output via switches
- Timing error related glitches
  - Control signal timing skew

Dynamic DAC Error: Timing Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where the control signals for LSB & MSB
  - LSB/MSBs on time
  - LSB early, MSB late
  - LSB late, MSB early



Glitch Energy

- Glitch energy (worst case) proportional to: $dt \times 2^{B-1}$
- dt → error in timing & 2^{B-1} associated with half of the switches changing state
- LSB energy proportional to: $T=1/f_s$
- Need $dt \times 2^{B-1} << T$ or $dt << 2^{-B+1} T$
- Examples:

f_s [MHz]	B	dt [ps]
1	12	<< 488
20	16	<< 1.5
1000	12	<< 0.5

→ **Timing accuracy for data converters much more critical compared to digital circuitry**

DAC Dynamic Errors

- To suppress effect of non-idealities:
  - Retiming of current source control signals
    - Each current source has its own clocked latch incorporated in the current cell
    - Minimization of latch clock skew by careful layout ensuring simultaneous change of bits
  - To minimize control and clock feed through to the output via G-D & G-S of the switches
    - Use of low-swing digital circuitry

DAC Implementation Examples

- Untrimmed segmented
  - T. Miki et al, "An 80-MHz 8-bit CMOS D/A Converter," JSSC December 1986, pp. 983
  - A. Van den Bosch et al, "A 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," JSSC March 2001, pp. 315
- Current copiers:
  - D. W. J. Groeneveld et al, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," JSSC December 1989, pp. 1517
- Dynamic element matching:
  - R. J. van de Plassche, "Dynamic Element Matching for High-Accuracy Monolithic D/A Converters," JSSC December 1976, pp. 795

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-21, NO. 6, DECEMBER 1986

An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI,
YOICHI AKASAKA, AND YASUTAKA HORIBA

8x8 array

2μ tech., 5Vsupply
6+2 segmented

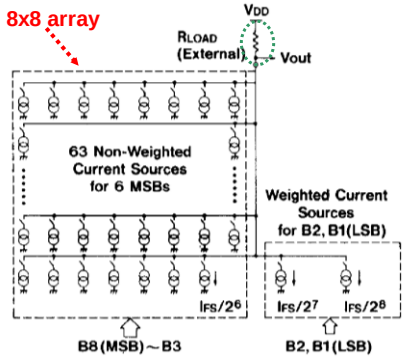


Fig. 1. Basic architecture of the DAC.

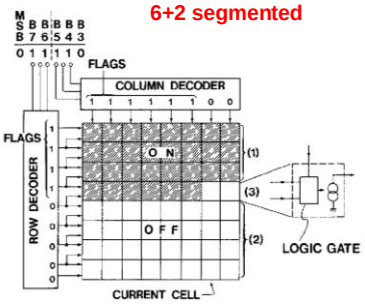
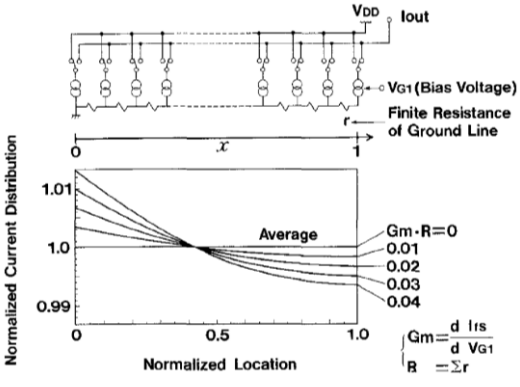


Fig. 2. Two-step decoding.

Two sources of systematic error:
- **Finite current source output resistance**
- **Voltage drop due to finite ground bus resistance**



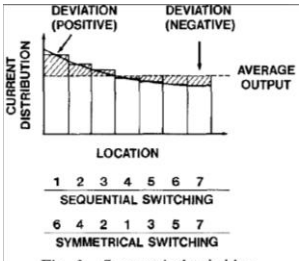
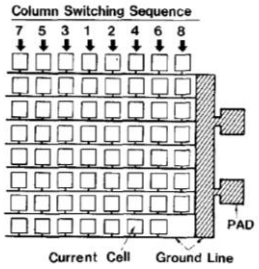


Fig. 9. Symmetrical switching.



Current-Switched DACs in CMOS

Assumptions:
RxI small compared to transistor gate-overdrive
To simplify analysis: Initially, all device currents assumed to be equal to *I*

$$V_{GS_{M2}} = V_{GS_{M1}} - 4RI$$

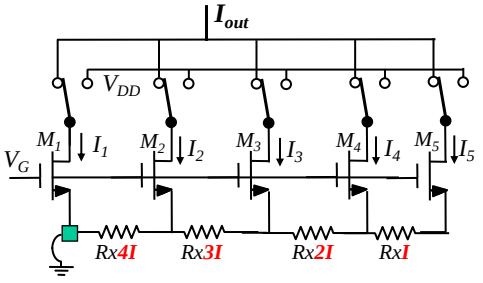
$$V_{GS_{M3}} = V_{GS_{M1}} - 7RI$$

$$V_{GS_{M4}} = V_{GS_{M1}} - 9RI$$

$$V_{GS_{M5}} = V_{GS_{M1}} - 10RI$$

$$I_2 = k\left(V_{GS_{M2}} - V_{th}\right)^2$$

$$I_2 = I_1\left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$



Example: 5 unit element current sources

Current-Switched DACs in CMOS

$$I_2 = k\left(V_{GS_{M2}} - V_{th}\right)^2 = I_1\left(1 - \frac{4RI}{V_{GS_{M1}} - V_{th}}\right)^2$$

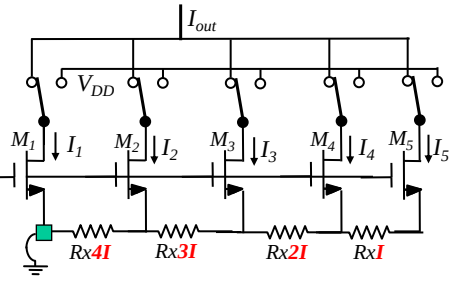
$$g_{m_{M1}} = \frac{2I_1}{V_{GS_{M1}} - V_{th}}$$

$$\rightarrow I_2 = I_1\left(1 - \frac{4Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 4Rg_{m_{M1}}\right)$$

$$\rightarrow I_3 = I_1\left(1 - \frac{7Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 7Rg_{m_{M1}}\right)$$

$$\rightarrow I_4 = I_1\left(1 - \frac{9Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 9Rg_{m_{M1}}\right)$$

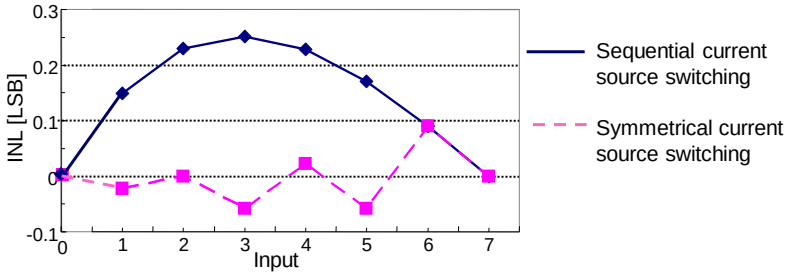
$$\rightarrow I_5 = I_1\left(1 - \frac{10Rg_{m_{M1}}}{2}\right)^2 \approx I_1\left(1 - 10Rg_{m_{M1}}\right)$$



Example: 5 unit element current sources

→ Desirable to have g_m small

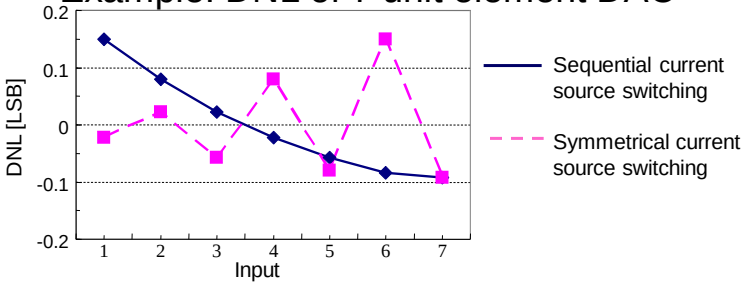
Current-Switched DACs in CMOS
Example: INL of 3-Bit unit element DAC



Example: 7 unit element current source DAC- assume $g_m R = 1/100$

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → $INL = +0.25LSB$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)
  → $INL = +0.09, -0.058LSB$ → INL reduced by a factor of 2.6

Current-Switched DACs in CMOS
Example: DNL of 7 unit element DAC



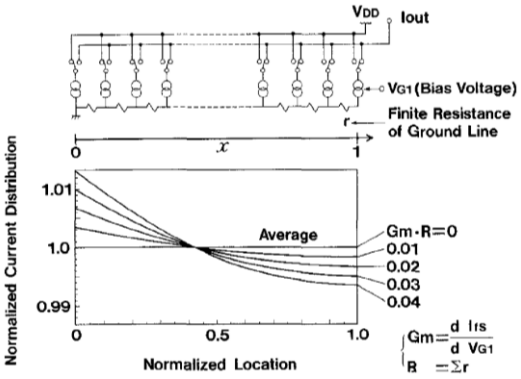
Example: 7 unit element current source DAC- assume $g_m R = 1/100$

- If switching of current sources arranged sequentially (1-2-3-4-5-6-7)
  → $DNL_{max} = +0.15LSB$
- If switching of current sources symmetrical (4-3-5-2-6-1-7)

  → $DNL_{max} = +0.15LSB$ → DNL_{max} unchanged

Two sources of systematic error:

- **Finite current source output resistance**
- **Voltage drop due to finite ground bus resistance**



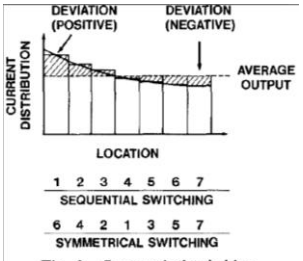


Fig. 9. Symmetrical switching.