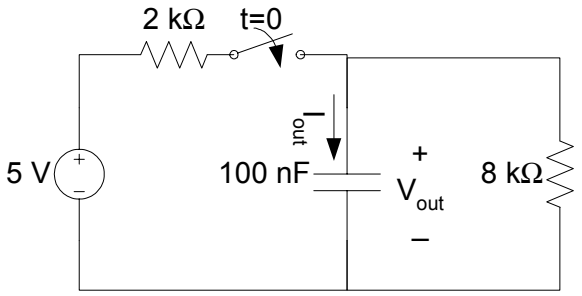
EE 42

Homework #4 Solutions

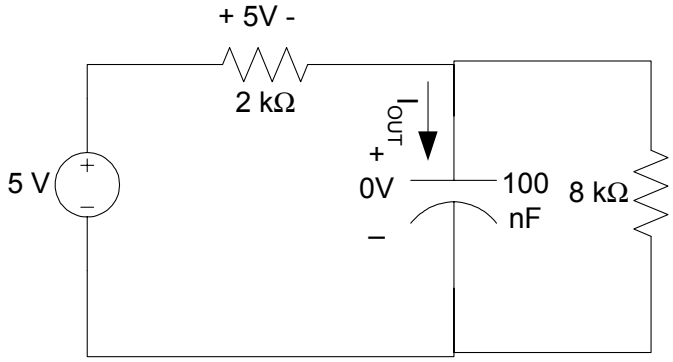
Problem 1:



$V_{OUT}(0) = 0$ V

since for t < 0, the capacitor was not attached to a voltage source.

At t = 0, the switch closes.



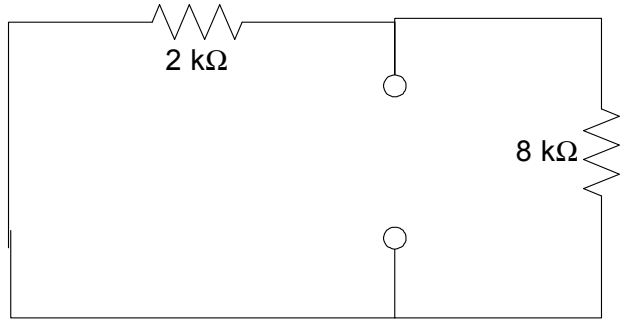
Since we know that the capacitor has 0 V, by KVL, the 2 kΩ resistor must have 5 V as shown.

By KCL,

$5\text{ V} / 2\text{ k}\Omega = I_{OUT} + 0\text{ V} / 8\text{ k}\Omega$

$I_{OUT}(0) = 2.5$ mA

To find the time constant for the circuit, turn off the voltage source and find R_{TH} with respect to capacitor terminals.

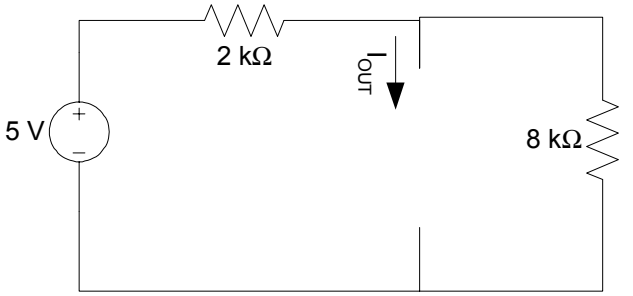


The resistors are in parallel (NOT in series, imagine an ohmmeter attached to the terminals…).

$R_{TH} = (1 / 2\text{ k}\Omega + 1 / 8\text{ k}\Omega)^{-1} = 1.6\text{ k}\Omega$

RC = (1.6 kW)(100 nF) = 160 μs

As t goes to infinity, the capacitor opens:

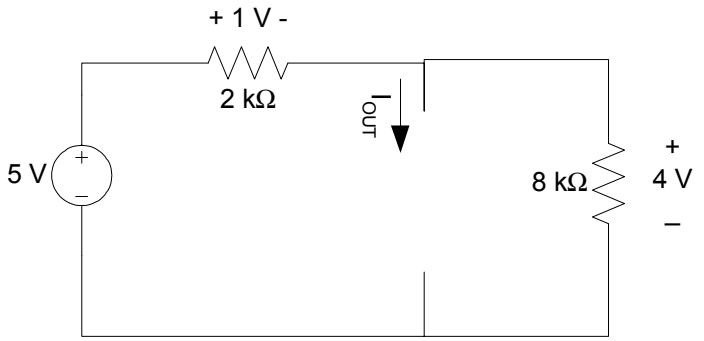


The final value of I_{OUT} is 0 A.

$I_{OUT}(t) = 2.5\ e^{-t/160\ \mu s}$ mA

Maximum value: 2.5 mA (at t = 0)

To find the power absorbed by the resistors, we need to find their individual voltages or currents. Finding $V_{OUT}(t)$ will help. We already know $V_{OUT}(0) = 0$ V and RC = 160 μs. The final value of V_{OUT} can be determined by the circuit as t goes to infinity.



Since there is no current through the open-circuit capacitor, the resistors are effectively in series. By voltage division, the 8 kΩ resistor has 4 V as shown. Thus, the final value of V_{OUT} is 4 V.

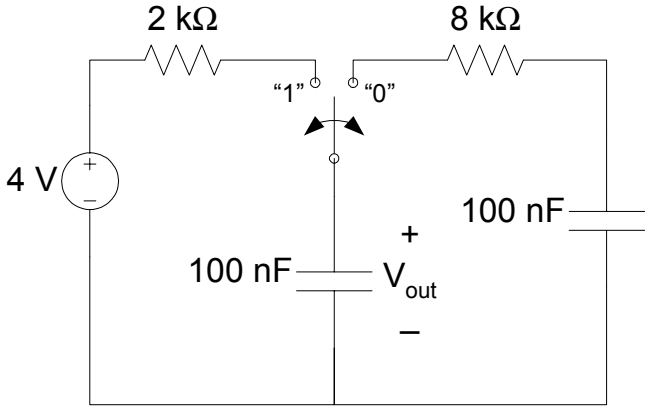
$V_{OUT}(t) = 4 - 4\, e^{-t/160\ \mu s}$ V

$P_{2k\Omega} = VI = V^2 / R = (5 - (4 - 4\, e^{-t/160\ \mu s}))^2 / 2000$ W Integral from t = 0 to infinity is infinity!

$P_{8k\Omega} = VI = V^2 / R = (4 - 4\, e^{-t/160\ \mu s})^2 / 8000$ W Integral from t = 0 to infinity is infinity!

So the total energy absorbed is infinite. (Prof. Ross confused the direction of the switch and ended up asking a silly question!)

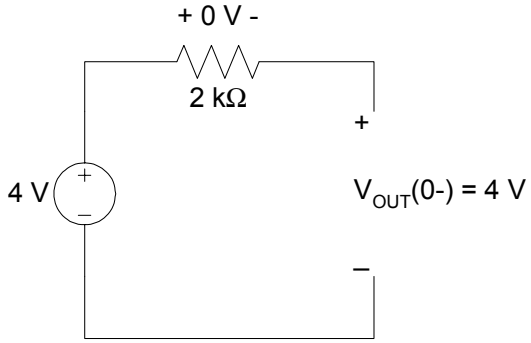
Problem 2:

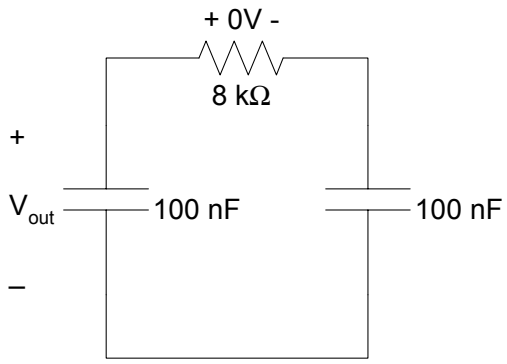


a) When the circuit is in position "0", the 4 V source and 2 kΩ resistor are disconnected. The two 100 nF capacitors combine in series to make $(1/(100 \times 10^{-9}) + 1/(100 \times 10^{-9}))^{-1}$ which is 50 nF. The only resistance is 8 kΩ.
$t_P = (\ln 2)(RC) = (\ln 2)(8\ k\Omega)(50\ nF)$
$= \mathbf{277\ \mu s}$

b) When the circuit is in position "1", the 8 kW resistor and 100 nF capacitor on the right are disconnected. The only capacitor is the 100 nF capacitor on the left, and the 2 kW resistor is the only resistance.
$t_P = (\ln 2)(RC) = (\ln 2)(2\ k\Omega)(100\ nF) = \mathbf{139\ \mu s}$

c) If the circuit has been in position "1" for a long time, the capacitor will be acting like an open circuit (until the first switch occurs at t = 0). Since zero current flows through an open circuit, the resistor carries 0 voltage and the capacitor gets all 4 V. So $V_{out}(0-) = V_{out}(0+) = 4$ V.





At t = 0, the circuit switches for the first time. The circuit will stay this way until t = 1 ms. We know the initial condition, and need the final value and RC.

Repeating the RC calculation from part a,
RC = (8 kΩ)(50 nF) = **400 µs**.

The final value is the value of V_{out} that would occur if we left the circuit this way indefinitely. Eventually, the capacitors will act like open circuits. This means that the resistor will have zero voltage (zero current flow). So to make KVL work, the capacitors must have equal voltage. The left capacitor starts out with 4 V x 100 nF worth of charge, and the right capacitor starts out discharged. The left capacitor must give half of its charge to the right capacitor to make the voltages equal. So the final value of V_{out} is half of the initial value: **2 V**.

So for t = 0 to t = 1 ms, $V_{out}(t)$ is:

$$V_{out}(t) = 2\text{ V} + 2\,e^{-t/400\ \mu s}\text{ V}$$

At t = 1 ms, the circuit switches back. We can find the voltage on the capacitor just after switching by finding the voltage just before switching since capacitor voltage is continuous:

$$V_{out}(1\text{ ms}) = 2\text{ V} + 2\,e^{-1\text{ ms}/400\ \mu s}\text{ V} = 2.16\text{ V}$$

From our part b calculation, for this circuit, RC = (2 kΩ)(100 nF) = **200 µs**.

When the circuit has been this way for a long time, the capacitor turns back into an open circuit, giving us again the circuit on the previous page. The final value of V_{out} is **4 V.**

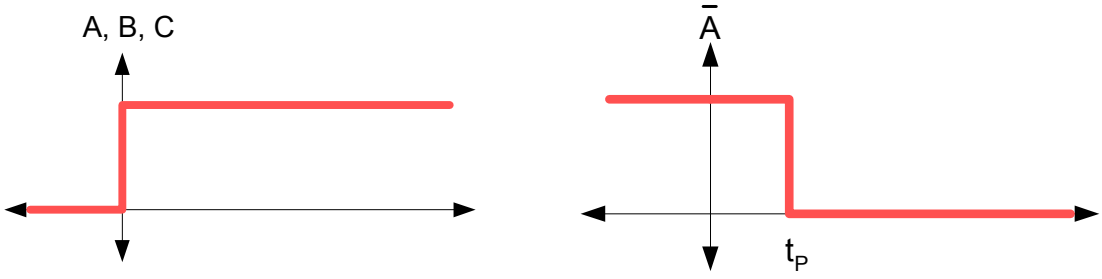
So for t = 1 ms and above,

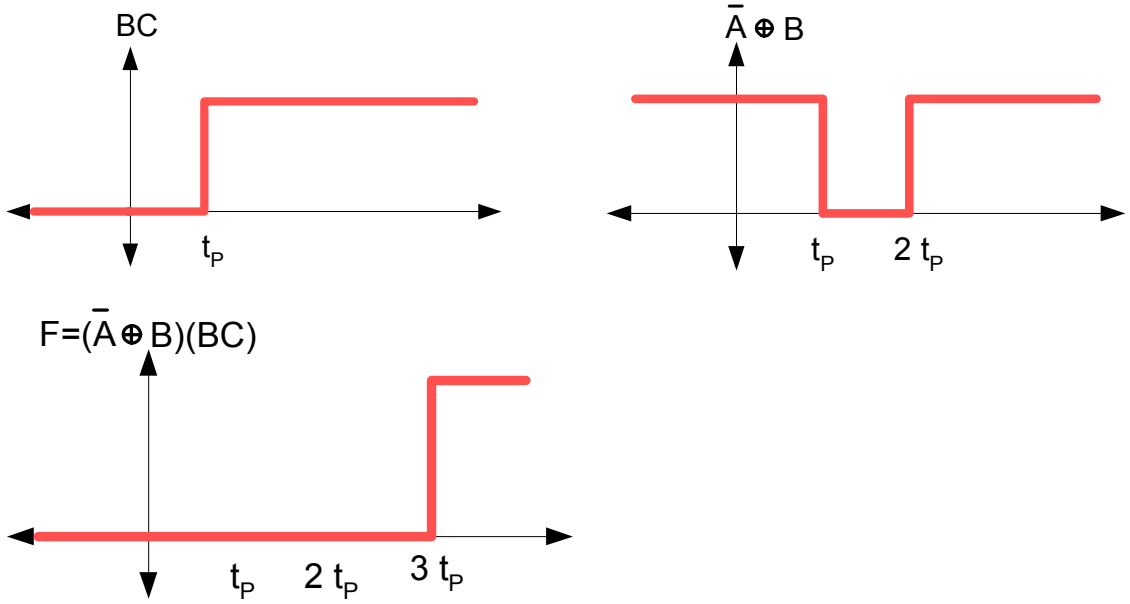
$$V_{out}(t) = 4\text{ V} + (2.16 - 4)\,e^{-(t-1\text{ms})/200\ \mu s}\text{ V} = 4\text{ V} - 1.84\,e^{-(t-1\text{ms})/200\ \mu s}\text{ V}$$

We may write the equations together as:

$$V_{out}(t) = \begin{cases} 2\text{ V} + 2\,e^{-t/400\ \mu s}\text{ V} & \text{for } 0 \le t < 1\text{ ms} \\ 4\text{ V} - 1.84\,e^{-(t-1\text{ms})/200\ \mu s}\text{ V} & \text{for } t \ge 1\text{ ms} \end{cases}$$

Problem 3:





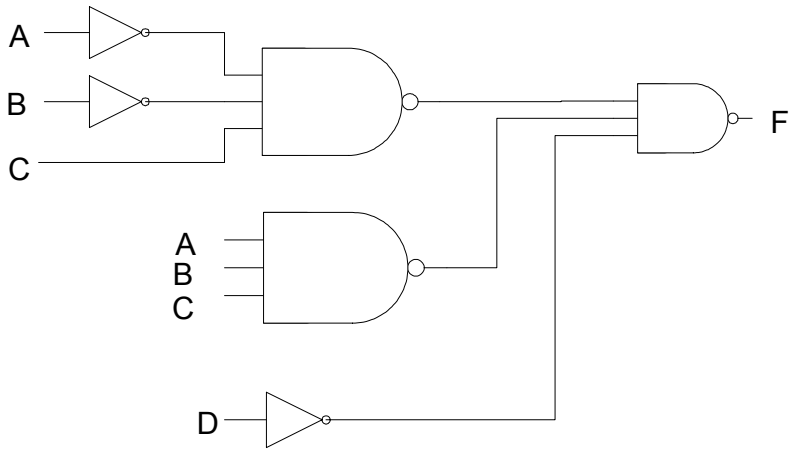
Problem 4:

AB \ CD	00	01	11	10
00	0	1	1	1
01	0	1	1	0
11	0	1	1	1
10	0	1	1	0

A good first step in any simplification is to use a Karnaugh map to provide a simpler sum of products implementation.

$F = D + \bar{A}\cdot\bar{B}\cdot C + A\cdot B\cdot C$

a) Lowest cost means fewest number of chips used. A good strategy is to minimize the number of different types of chips used by doing at least a partial NAND-NAND implementation of the sum-of-products we found. Many possible answers—here is one.



This requires two chips ($0.30):

3 3-input NAND chip
6 inverter chip

We don't have to use all the gates on the chip.

The inverter is needed at the D input to properly convert from AND-OR to NAND-NAND.

b) There is really no systematic way to reduce the propagation delay of a circuit. One could try to simplify the circuit using Boolean logic. In this case, I can't find a way to reduce the delay to less than 60 ns (3 gates), so the circuit from part a would be an acceptable answer.

c) There is really no systematic way to find the circuit with the minimum number of gates. The Karnaugh map gives us the simplest sum-of-products implementation, but maybe other types of implementations would be simpler. We need to look at the function and see if we can simplify it.

$$F = D + \overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot C = D + \left(\overline{A} \cdot \overline{B} + A \cdot B\right)C = D + \overline{(A \oplus B)} \cdot C$$

The sum-of-products implementation was hiding an XNOR gate, which does the work of several AND/OR/NOT gates in this example. This gives us a circuit with only 3 gates.