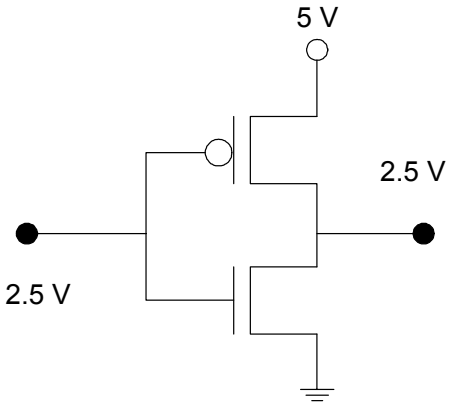
EE 42

Homework #6

Due Friday, May 7 at 4pm in drop box

Problem 1:

Imagine that you are fabricating a CMOS inverter from scratch. You want your inverter to have a midpoint of 2.5 V when the supply voltage is 5 V. This means when the input is 2.5 V, the output should be 2.5 V, as shown.



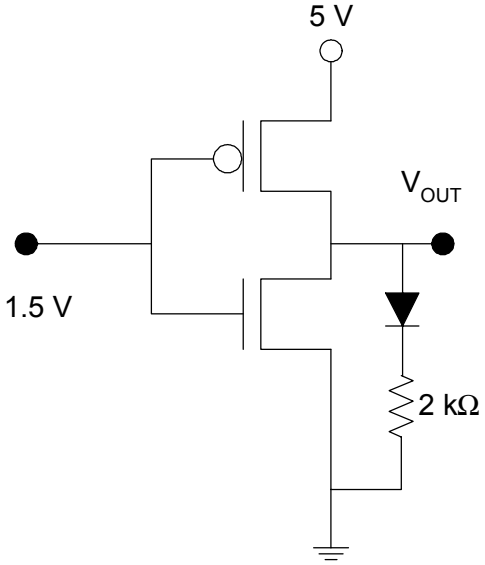
Your fabrication process determines that:
C_{OX} = 5 fF/μm^2 for both PMOS and NMOS
μ_n = 500 cm^2/(Vs)
μ_p = 400 cm^2/(Vs)
$V_{TH(n)}$ = 1 V
$V_{TH(p)}$ = -1 V
λ_n = 0.1 V^{-1}
λ_p = -0.1 V^{-1}

You have already decided on the lengths of the transistors; $L_n = L_p$ = 1.5 μm.

With W_n = 10 μm, what is the value of W_p (the width of the PMOS) needed for this midpoint?

Problem 2:

Find V_{OUT} for the circuit shown at right.



Assume the large-signal model for the diode,
With V_F = 2 V.

$W/L\mu_nC_{ox} = W/L\mu_pC_{ox}$ = 1 mA/V^2
$V_{TH(n)}$ = 1 V
$V_{TH(p)}$ = -1 V
$\lambda_n = \lambda_p$ = 0 V^{-1}

Problem 3:

Consider a CMOS NAND gate.
Suppose we attach *n* CMOS logic gate inputs to the output of this NAND gate (fanout of *n*).

What is the maximum value of *n* allowed if the worst-case propagation delay t_p through the NAND is not to exceed 100 ns?

Note: The propagation delay varies with different input combinations. You need to find the worst-case combination.

R_n = 1 kΩ R_p = 3 kΩ C_G = 10 pF

Problem 4:

Let's explore how transistor design, through the choice of the transistor dimensions W and L, as well as the choice of power supply voltage V_{DD}, contributes to gate delay.

R_n and R_p, the pull-down/pull-up transistor resistances, are calculated in the following way:

R = average value of (V_{DS} / I_D) over the time period 0 to t_p (during pull-up for PMOS or pull-down for NMOS)

In other words, average V_{DS} / I_D from the start of the pull, when $V_{DS} = \pm V_{DD}$, to the halfway point of the pull, when $V_{DS} = \pm V_{DD}/2$. During this time, V_{DS} is bigger in magnitude than $V_{DD}/2$, so you can assume saturation mode (Why? Review our inverter analysis of Lecture 20 where we talked about the possible modes during transitions.) You can also neglect the effect of λ.

C_G is calculated in the following way, via the parallel-plate capacitor formula:

$C_G = (W)(L)(C_{ox}) = (W)(L)(\varepsilon_0 k_{ox})/(t_{ox})$

where ε_0 is a physical constant, and k_{ox} and t_{ox} are fixed by the fabrication process.

In view of these facts, fill in the following table, and provide justification for your answers:

Fill in "increases" or "decreases" in each blank below.			
As W increases,	R _____	C_G _____	t_p _____
As L increases,	R _____	C_G _____	t_p _____
As V_{DD} increases,	R _____	C_G _____	t_p _____

Problem 5:

Suppose you have a DRAM cell, with capacitance C_{cell} = 25 fF.

In order to read a logic 1 (3 V) from this cell, the bit line must be able to achieve a voltage of at least 0.1 V so the sense amplifier can detect it.

How big can the bit line capacitance C_{line} be?

If $C_{line} = (W)(L)(C_{ox}) = (1\ \mu m)(L)(150\ \mu F/m^2)$ where L is the length of the bit line in meters, how long can the bit line be?