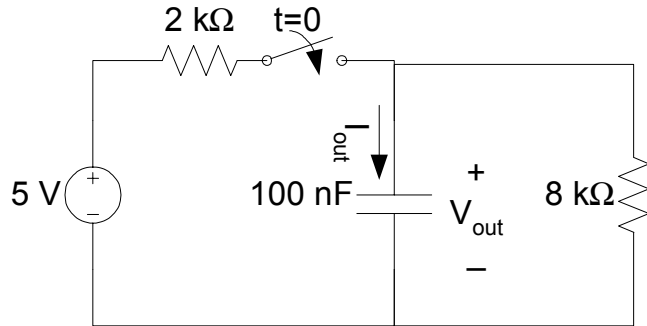# EE 42

Homework #4

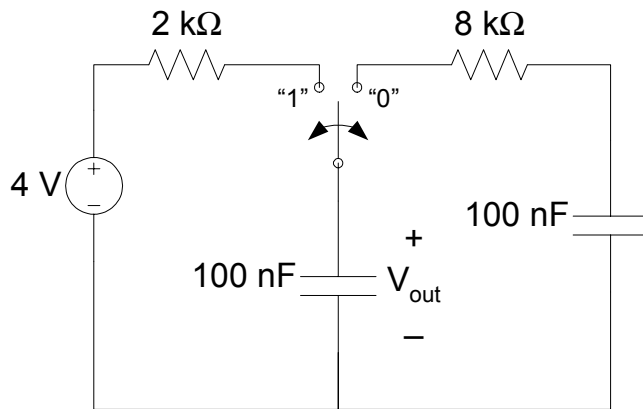Due Friday, March 19 at noon in drop box

Problem 1:

Assume that the circuit has been "unswitched" for a long time, and then switches as shown at t=0.

a) What is the maximum value of $I_{out}(t)$? When does it occur?
b) How much energy is absorbed by the resistors from t = 0 to infinity?

Problem 2:

Assume that the circuit has been in position "1" for a long time, and then switches to position "0" at t = 0, then back to position "1" at 1 ms.

a) What is t_P (the propagation delay) when the circuit is in position "0"?
b) What is t_P (the propagation delay) when the circuit is in position "1"?
c) Write an expression for $V_{out}(t)$ covering all values of t ≥0.

Problem 3:
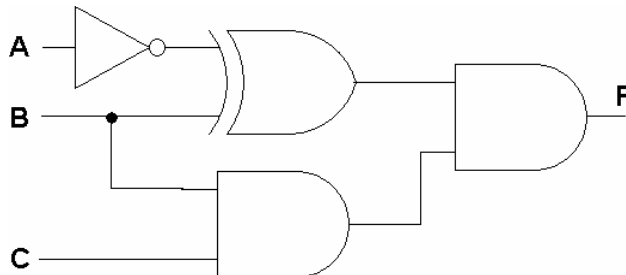
Assume that inputs A, B, and C have been at logic zero for a long time, and then instantaneously change to logic 1 at time t=0.

Assume also that each logic gate has propagation delay t_P.

Draw a timing diagram indicating the logic transitions of the output F.

Problem 4:

Inputs				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Consider the Boolean function defined by the truth table at left.

Available to you are chips with the following contents:

- a chip with 6 NOT gates
- a chip with 4 2-input AND gates
- a chip with 4 2-input NAND gates
- a chip with 4 2-input OR gates
- a chip with 4 2-input NOR gates
- a chip with 4 2-input XOR gates
- a chip with 4 2-input XNOR gates
- a chip with 3 3-input AND gates
- a chip with 3 3-input NAND gates
- a chip with 3 3-input OR gates
- a chip with 3 3-input NOR gates
- a chip with 2 4-input NAND gates
- a chip with 2 4-input NOR gates
- a chip with 1 8-input NAND gate

Each chip costs $0.15, and each logic gate has a propagation delay of 20 ns.

Using these chips,

a) Design a circuit that implements the Boolean function at the lowest cost.

b) Design a circuit that implements the Boolean function with the lowest propagation delay from input to output.

c) Design a circuit that implements the Boolean function using the fewest total number of logic gates.

(In real life, the chip prices and propagation delays differ for the different types of gates. But, I was surprised to see that the price and delay for something simple like an inverter were actually pretty close to that for more complicated gates like XOR, making this simple example somewhat realistic. I was looking at Texas Instruments' High-Speed CMOS technology family for this example.)