EE 42

Homework #3

Due Friday, March 5, 2004 at 12:00 PM in drop box

Problem 1:

Most of the time, the range of voltages that a digital circuit considers to be "logic 1" is larger than the range it considers to be "logic 0".

For example, a circuit may be able to interpret an input that is anywhere between 3 V and 5 V as logic 1, but it may only recognize voltages between 0 V and 1V (or less) as logic 0.

So the threshold voltage is usually not right in the middle of the range. This means it may take longer for the comparator to switch for input is transitioning from logic 1 to logic 0 than it does for the opposite transition. This means it takes longer (and takes more power) to perform computations with certain numbers. Let's explore this asymmetry.

Consider a comparator with:

A = 1000
$R_i = \infty\ \Omega$
$R_O = 0\ \Omega$
Logic 1 = 5 V
Logic 0 = 0 V
Threshold voltage = 1.5 V

Let $V_{IN,UP}(t) = 5 - 5e^{-2000\,t}$ V where t is in seconds.

Let $V_{IN,DN}(t) = 5\,e^{-2000\,t}$ V where t is in seconds.

Find t_{UP}, the time when the comparator output first hits 5 V for input $V_{IN,UP}$, and t_{DN}, the time when the comparator output first hits 0 V for input $V_{IN,DN}$.

Problem 2:

Digital circuits use the most power when the input voltage is between logic 0 and logic 1. Reducing the amount of time that signals spend between logic 0 and logic 1 reduces energy consumption. A comparator can accomplish this.

The power absorbed by a certain digital circuit, P=VI, works out to the following as a function of the input voltage V_{IN}:

$$P = 4 - (V_{IN} - 2)^2 \quad W$$

a) Suppose we apply a "corrupted" signal $V_{IN,BAD}(t) = 4\,e^{-t}$ V (where t is in seconds) directly to the input of the digital circuit, without first "cleaning it up" with a

comparator. Find the total energy absorbed by the digital circuit for t>0 (all the way to infinity).

b) Now suppose we "clean up" the input signal before applying it to the digital circuit, using a comparator with

A = 1000
$R_i = \infty\ \Omega$
$R_O = 0\ \Omega$
Logic 1 = 4 V
Logic 0 = 0 V
Threshold voltage = 1 V

We put $V_{IN,BAD}(t)$ into the comparator, and the comparator output will be fed to the digital circuit instead. Call the comparator output $V_{IN,GOOD}(t)$.

Find the total energy absorbed by the digital circuit for t>0 (all the way to infinity) when the input is $V_{IN,GOOD}(t)$.

Problem 3:

Design a 4-bit D/A converter.

The circuit should take four voltage inputs, V_0 V_1 V_2 and V_3, with V_0 representing the least significant bit (1's place), and V_3 representing the most significant bit (8's place). The inputs can either be 0 V (logic 0) or 4 V (logic 1).

The output should be an integer voltage with value equal to the number represented at the input.

Specify what the rails should be to ensure proper operation of the circuit.

Problem 4:

Design a 2-bit A/D converter, **without using digital logic gates**.

The circuit takes an input voltage V_{IN} which is greater than or equal to 0 V and strictly less than 4 V.

There should be 2 output voltages, V_0 and V_1. This is what the output should be:

$0 \le V_{IN} \le 1$	V_1 = 0 V, V_0 = 0 V
$1 < V_{IN} \le 2$	V_1 = 0 V, V_0 = 4 V
$2 < V_{IN} \le 3$	V_1 = 4 V, V_0 = 0 V
$3 < V_{IN}$	V_1 = 4 V, V_0 = 4 V

Assume you are working with op-amps that have very high gain, so you don't have to worry about the small range of inputs that land you in the linear region.

Hint: It is easy to get the output V_1, you are deciding whether the input is above 2 V. Think about how you would determine if a number is even or odd. It also might be helpful to think about how you convert from decimal to binary by hand.