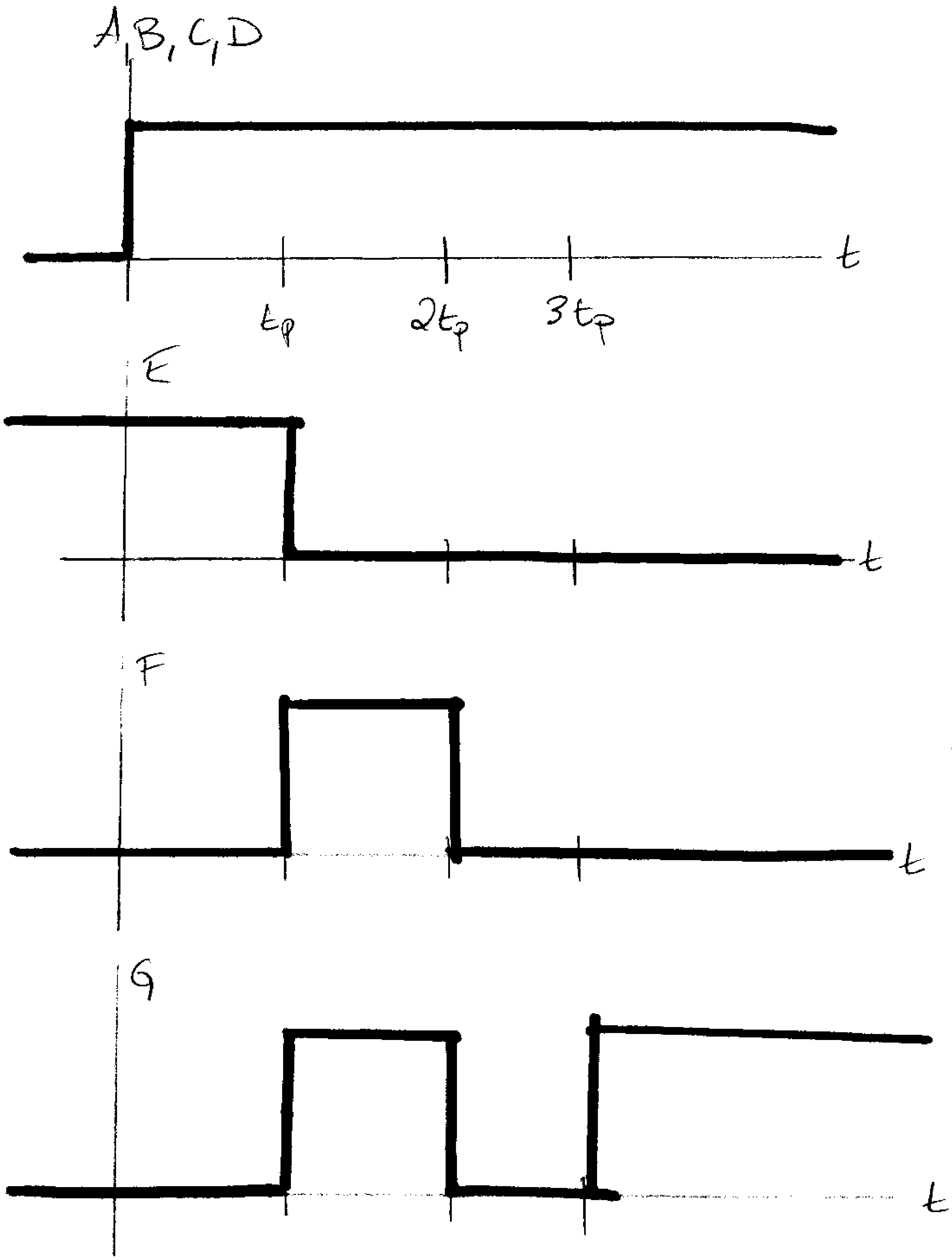
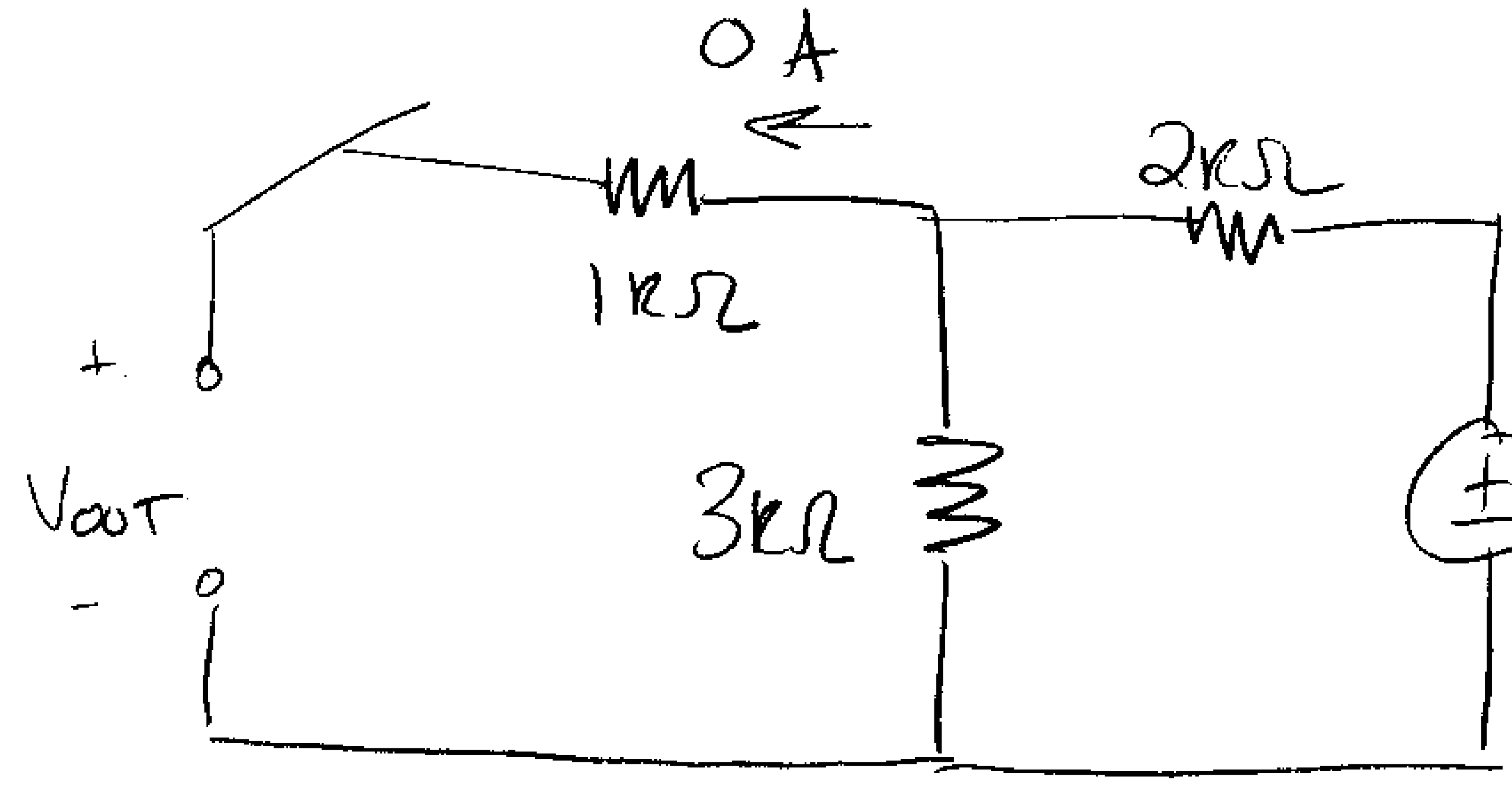
Practice Exam Solutions

Problem 1:

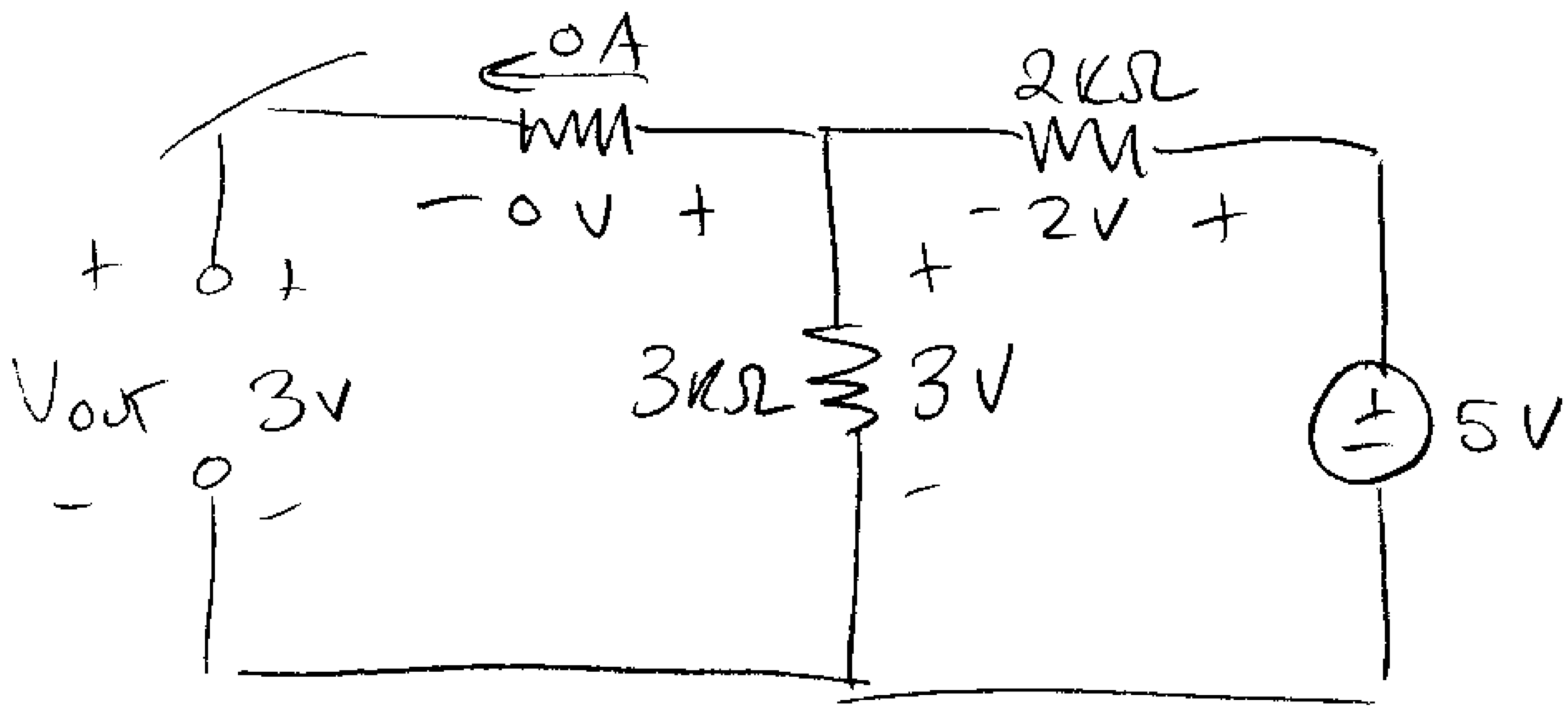


Problem 2: Need to find $V_{OUT}(0)$.

$t<0$: After a long time, capacitor is open circuit

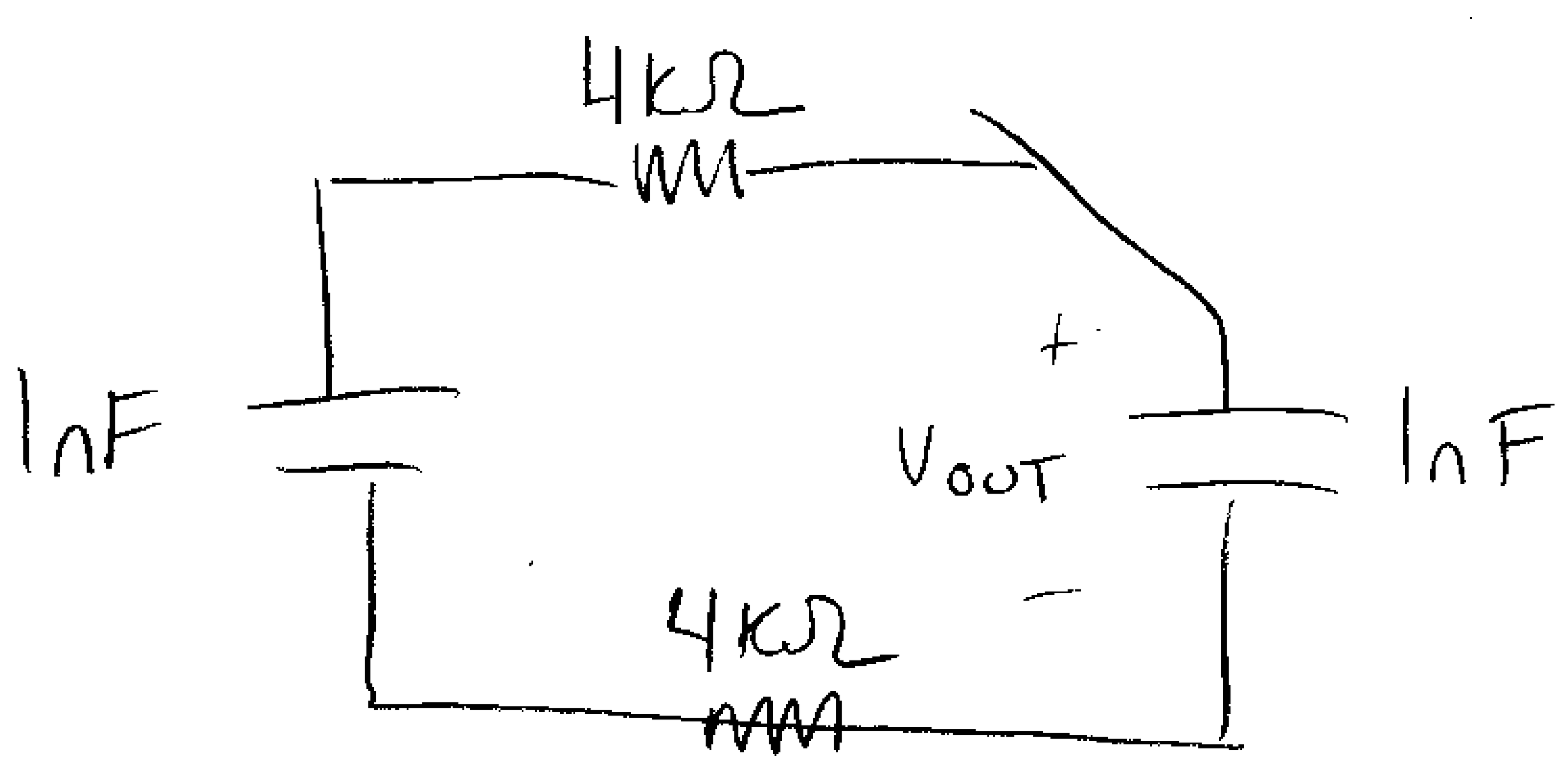


Since 0 A thru 1kΩ resistor (open circuit), voltage division of 5V over 2K + 3K resistors (they have same current):



By KVL, $V_{OUT}(0) = 3V$.

$t \geq 0$ until $t = 8\mu s$:



Everything in series.

Total resistance: $8k\Omega$.

Total capacitance: $500pF$.

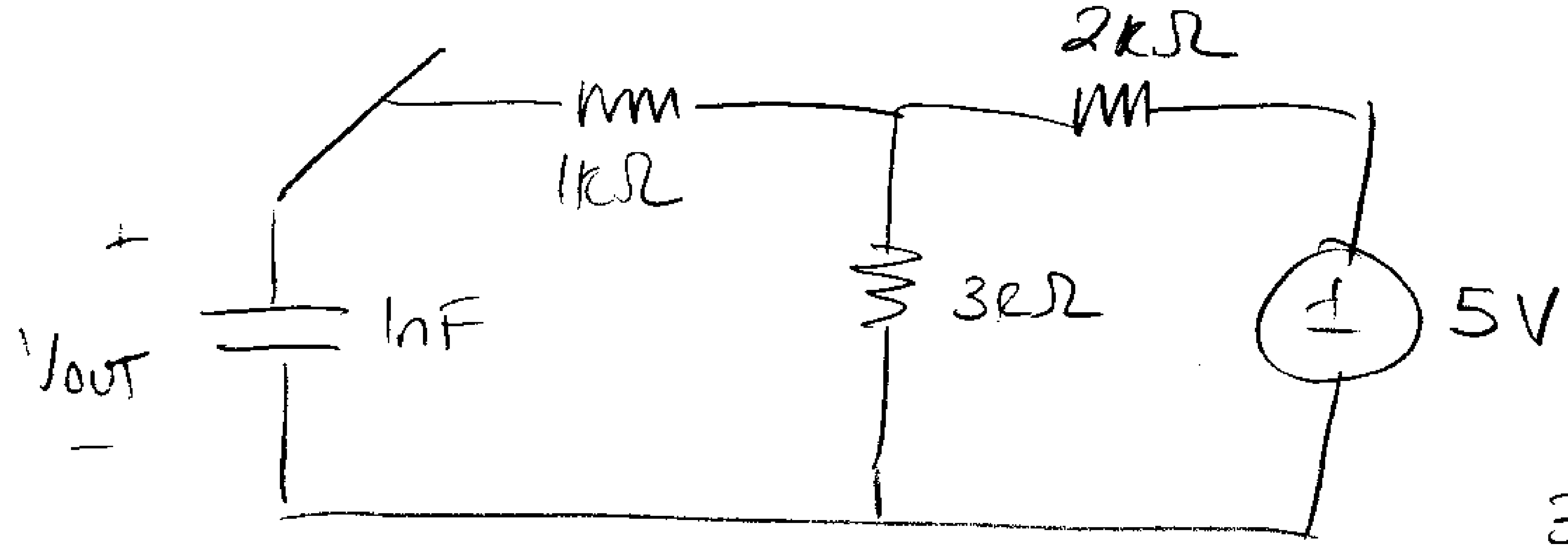
$RC = 4\mu s$.

$V_{OUT}(0) = 3V$

$V_{OUT,f} = 1.5V$ (must give 1/2 its charge to other capacitor)

$V_{out}(t) = 1.5 + (3-1.5)e^{-t/4\mu s}$

$t \geq 8\mu s$:



$C = 1nF$

R_{eq}: kill source to see that $3k\Omega$ + $2k\Omega$ in parallel, Combo is $\left(\frac{1}{3k} + \frac{1}{2k}\right)^{-1} = 1.2k$

This in series with 1k gives $R_{eq} = 2.2 k\Omega$

$$V_{OUT}(8\mu s) = 1.5 + (3 - 1.5)e^{-8\mu s / 4\mu s}$$

$$= 1.70 \text{ V}$$

$V_{OUT_f} = 3V$ by same analysis as $V_{OUT}(0)$

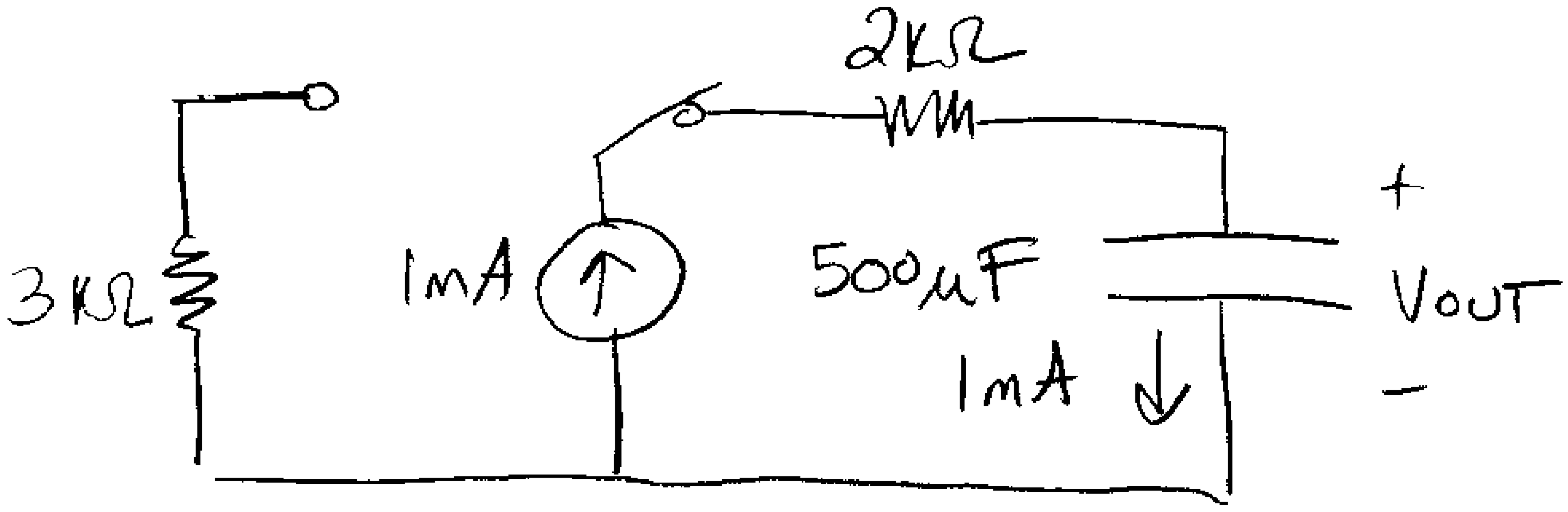
$$V_{out}(t) = 3V + (1.7 - 3)e^{\frac{-(t - 8\mu s)}{2.2\mu s}}$$

Overall,

$$V_{out}(t) = \begin{cases} 1.5 + 1.5e^{-t/4\mu s} \text{ V} & 0 \leq t \leq 8\mu s \\ 3 - 1.3e^{\frac{-(t-8\mu s)}{2.2\mu s}} & 8\mu s \leq t \end{cases}$$

Problem 3:

For $t \geq 0$, until $t = 3s$,



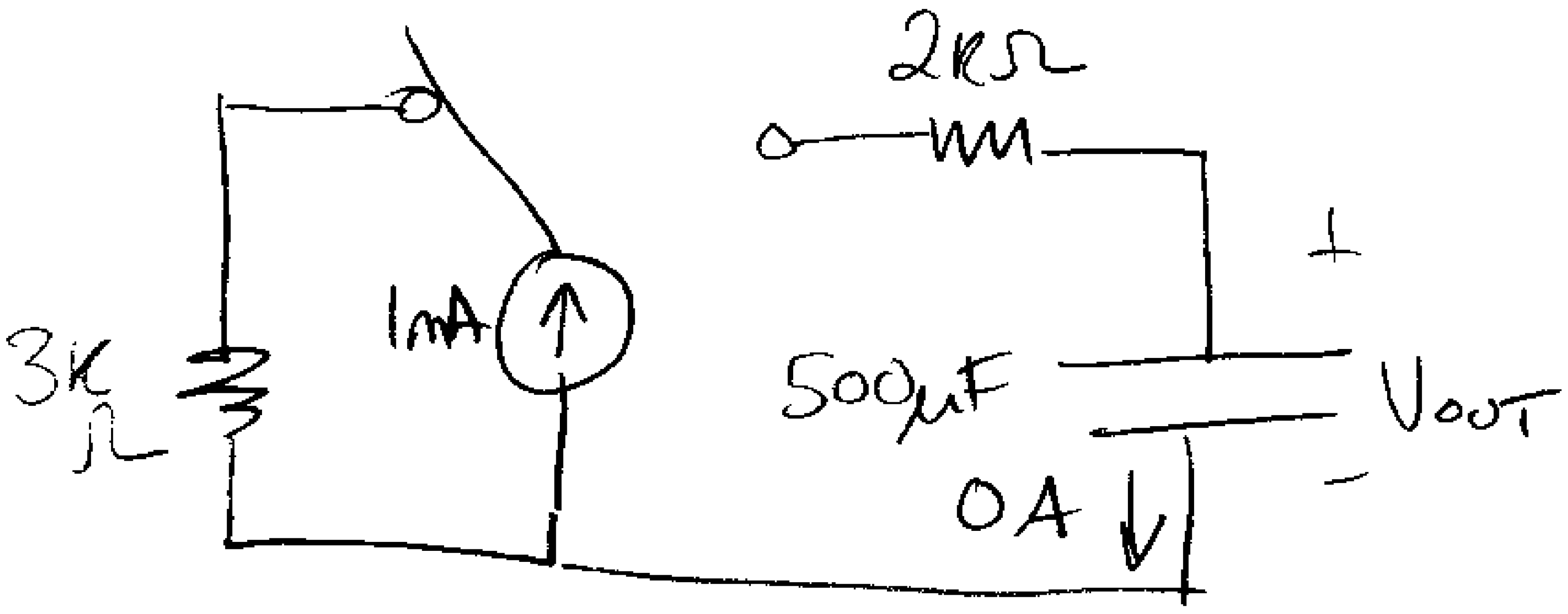
$$I = C\frac{dv}{dt}$$

$$1mA = 500\mu F \frac{dV_{OUT}}{dt}$$

$$V_{OUT}(t) = \int_0^t \frac{1mA}{500\mu F} dt' + V_{OUT}(0)$$

$$= \frac{1mA}{500\mu F} t + 1V = 2t + 1 \text{ V}$$

For $t \geq 3s$,



$$V_{out}(t) = \int_{3s}^{t} 0 \, dt' + V_{out}(3s)$$

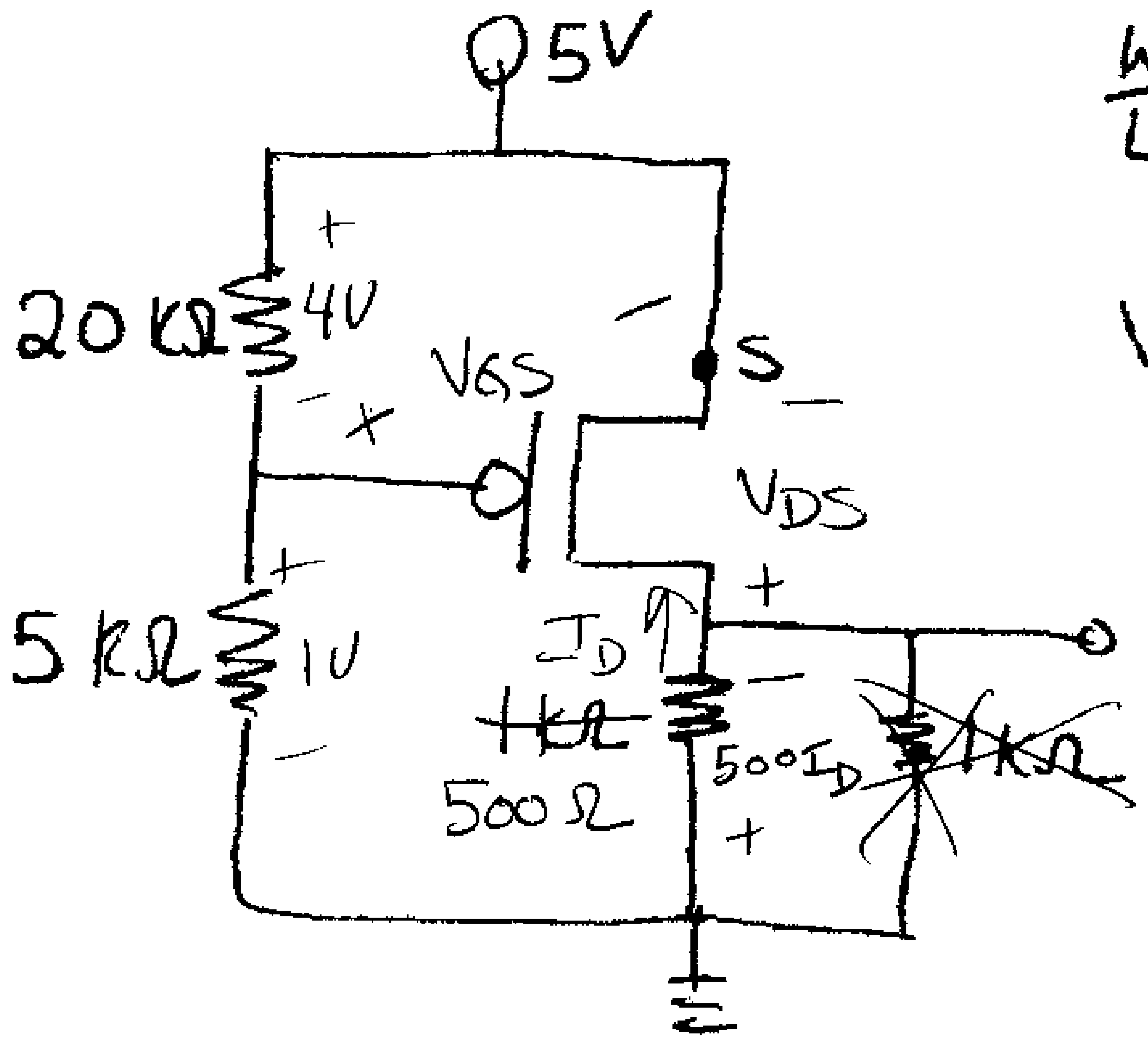
(open circuit, 0A)

$$= V_{out}(3s)$$

$$= 7 \text{ V}$$

$$V_{OUT}(t) = \begin{cases} 2t + 1 \text{V} & 0 \leq t \leq 3 \text{ s} \\ 7 \text{ V} & 3s \leq t \end{cases}$$

Problem 4:



$\frac{W}{L} \mu_p C_{ox} = 2\ mA/V^2$

$\lambda p = 0$

$V_{TH(p)} = -1V$

Find V_{OUT}.

By voltage division (since no current into gate) 20kΩ resistor has 4V as shown.

By KVL, $V_{GS} = -4V$ $V_{GS} < V_{TH} \Rightarrow$ not cutoff

Guess saturation (although the bigger V_{GS} is, the more likely we are in triode mode!)

$I_D = -2mA/V^2 \cdot 1/2 \cdot (-4V - -1V)^2 = -9mA$

Can combine parallel 1K resistors to one 500Ω resistor.

KVL: $500\Omega \cdot I_D + V_{DS} + 5V = 0$. $V_{DS} = -0.5V$

$V_{DS} \not< V_{GS} - V_{TH}$ So must be triode mode...

Problem 4 Cont.

$$I_D = -2mA/V^2 \left(-4V - -1V - \frac{V_{DS}}{2}\right) V_{DS}$$

From KVL, $I_D = -\dfrac{5 + V_{DS}}{500}$

Substitute & solve...

$V_{DS} = \{-6.45, -1.55\}$

-6.45 V impossible since then $V_{DS} \not> V_{GS} - V_{TH}$

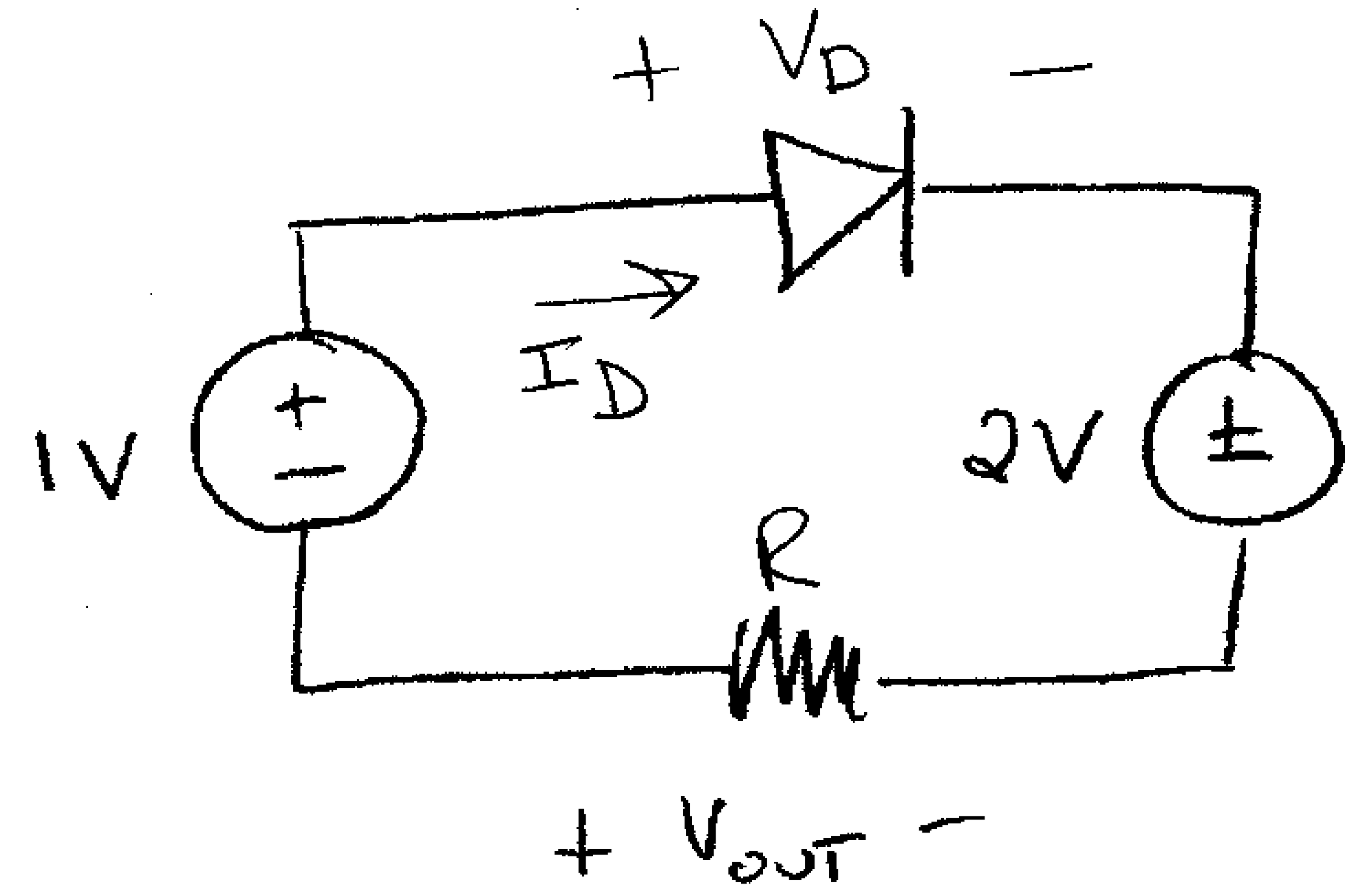
(and also, associated I_D would be positive ⇒ can't for PMOS)

So $V_{DS} = -1.55$, satisfies $V_{DS} > V_{GS} - V_{TH}$.

$V_{OUT} = -500 I_D$ (see diagram)

$$V_{OUT} = -500\left(-\frac{5 + V_{DS}}{500}\right) = \underline{3.45V}$$

Problem 5:



$V_F = 0.7V$

Use large-signal model for diode.

By KVL,

$$-1V + V_D + 2V - V_{OUT} = 0$$

By Ohm's law,

$$V_{OUT} = -R I_D$$

$$V_D = -R I_D - 1V$$

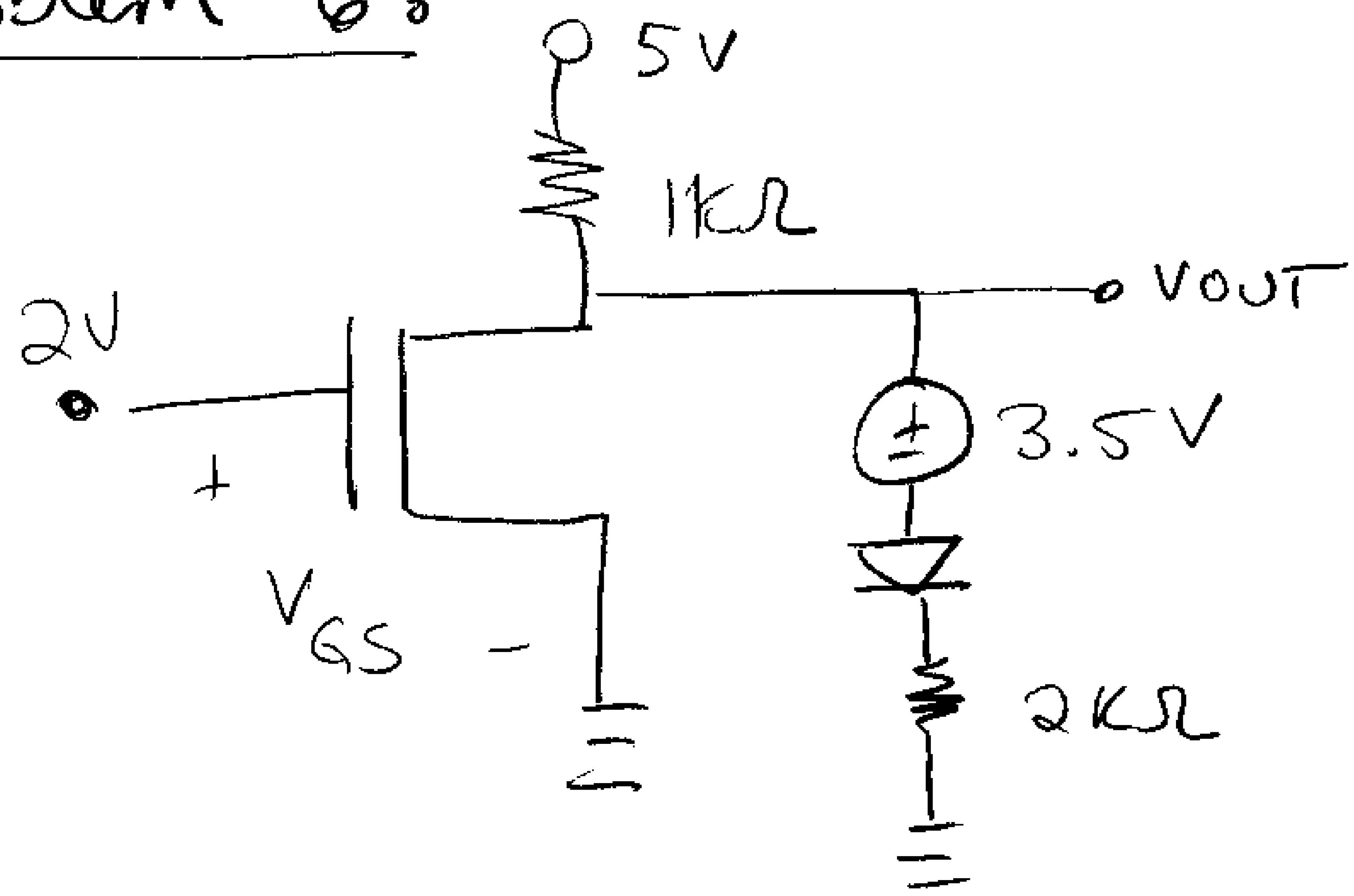
If forward bias, $V_D = 0.7V$ and $I_D > 0$.
If reverse bias, $V_D < 0.7V$ and $I_D = 0$.
One of these works in above equation.

If forward bias,
$0.7 = -R I_D - 1V$ Since $R > 0$ & $I_D > 0$, impossible.

If reverse bias,
$V_D = -1V$ possible under reverse bias.

$$V_{OUT} = -R I_D = -R \cdot 0A = 0V$$

Problem 6:



$V_{GS} = 2V$ $\quad V_{GS} > V_{TH} \Rightarrow$ not cutoff

Guess saturation.

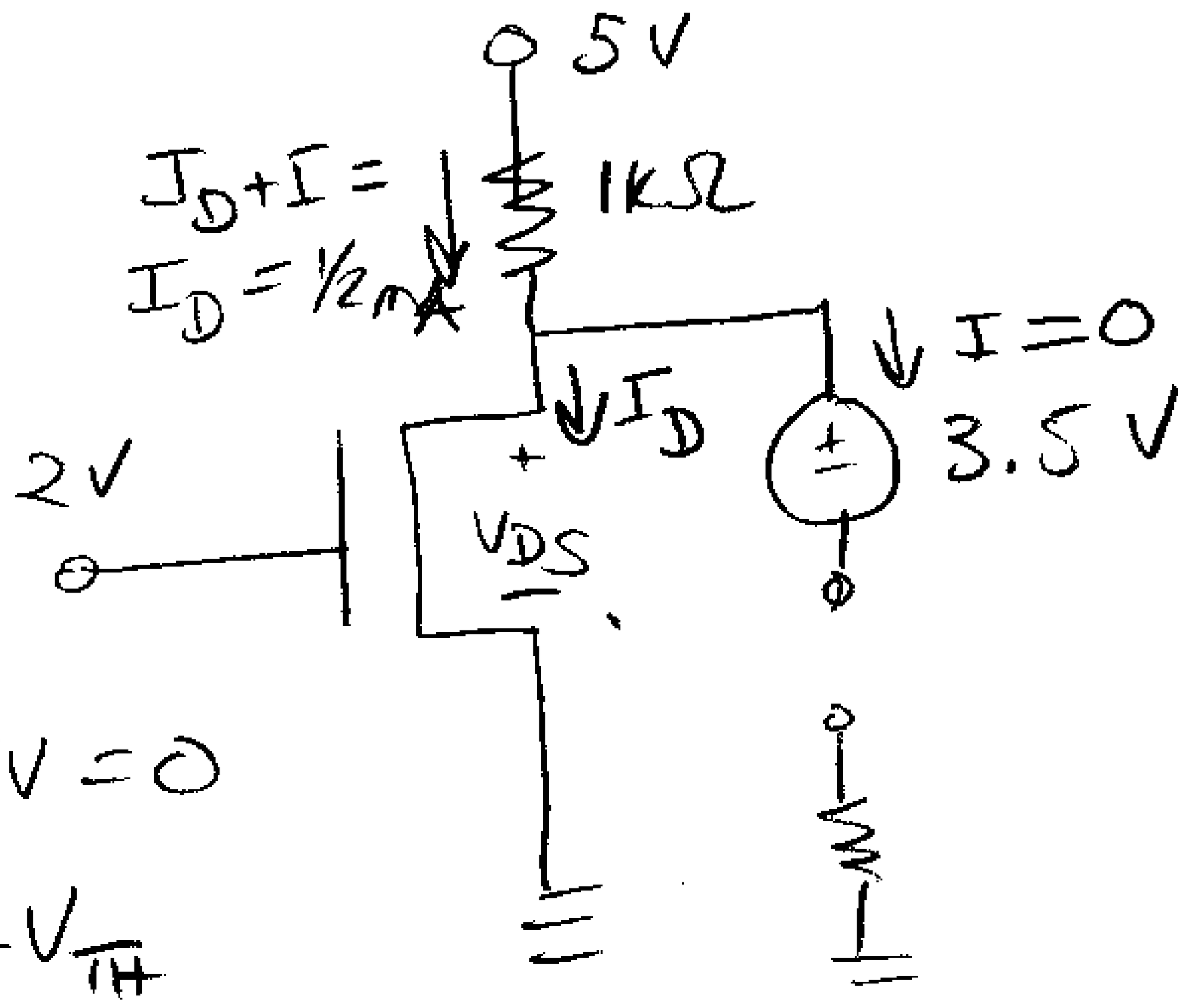
$I_D = 1mA/V^2 \cdot \frac{1}{2}(2V - 1V)^2 = \frac{1}{2} mA$ (not a joke)

Diode forward or reverse biased?

If forward, then V_{OUT} would be at least 5.5V.
This would make current flow up the 1K resistor.
Since current can't flow up the diode,
current would have to flow up transistor,
making I_D negative. Not possible for NMOS.

Guess reverse bias.

Now no current thru diode branch. By KCL, I_D flows thru 1K resistor.



KUL: $-V_{DS} - 1K\Omega \cdot \frac{1}{2}mA + 5V = 0$

$V_{DS} = 4.5V \quad V_{DS} > V_{GS} - V_{TH}$

Saturation is correct mode. $V_{OUT} = V_{DS} = 4.5V$