Name Solutions

EE 40

Final Exam

May 23, 2003

PLEASE WRITE YOUR NAME ON EACH ATTACHED PAGE

PLEASE SHOW YOUR WORK TO RECEIVE PARTIAL CREDIT

PLEASE DO NOT LEAVE DURING LAST 30 MINUTES OF EXAM PERIOD

Problem 1: 10 Points Possible ________

Problem 2: 10 Points Possible ________

Problem 3: 10 Points Possible ________

Problem 4: 15 Points Possible ________

Problem 5: 15 Points Possible ________

Problem 6: 45 Points Possible ________

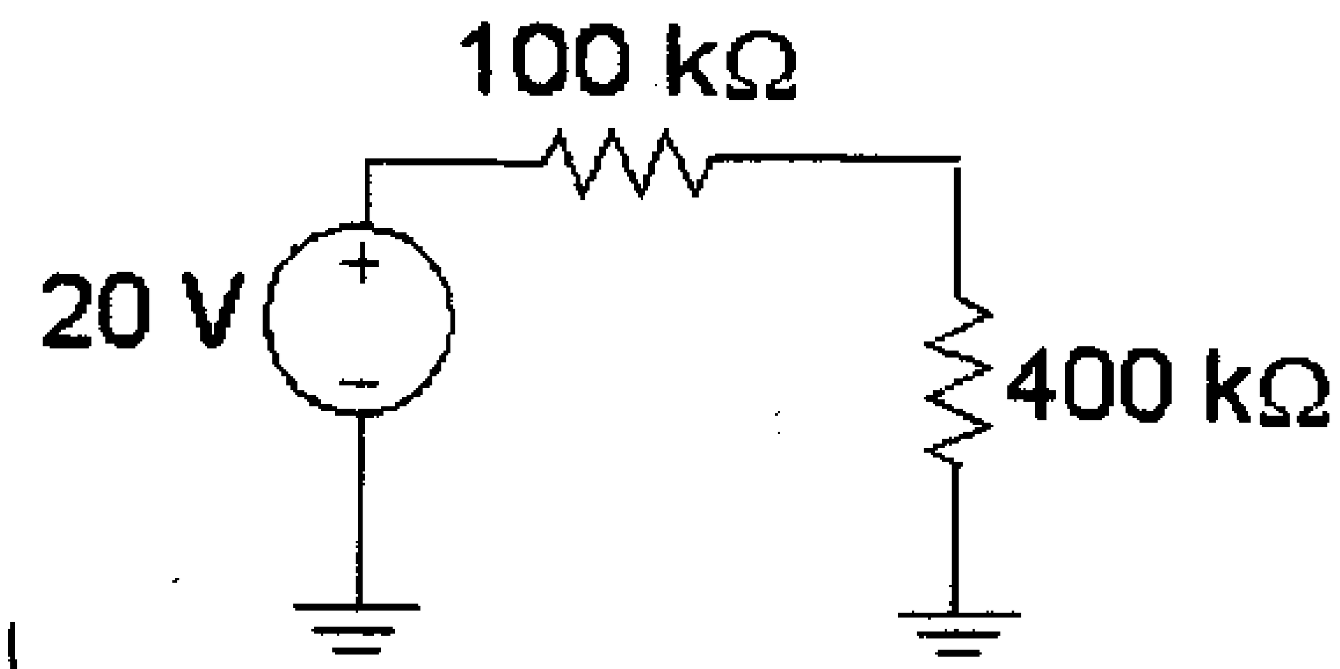
________ Choice 1 ________ Choice 2 ________ Choice 3 ________ Choice 4 ________ Choice 5

TOTAL: 105 Points Possible ________ (Yes, you can score over 100%)

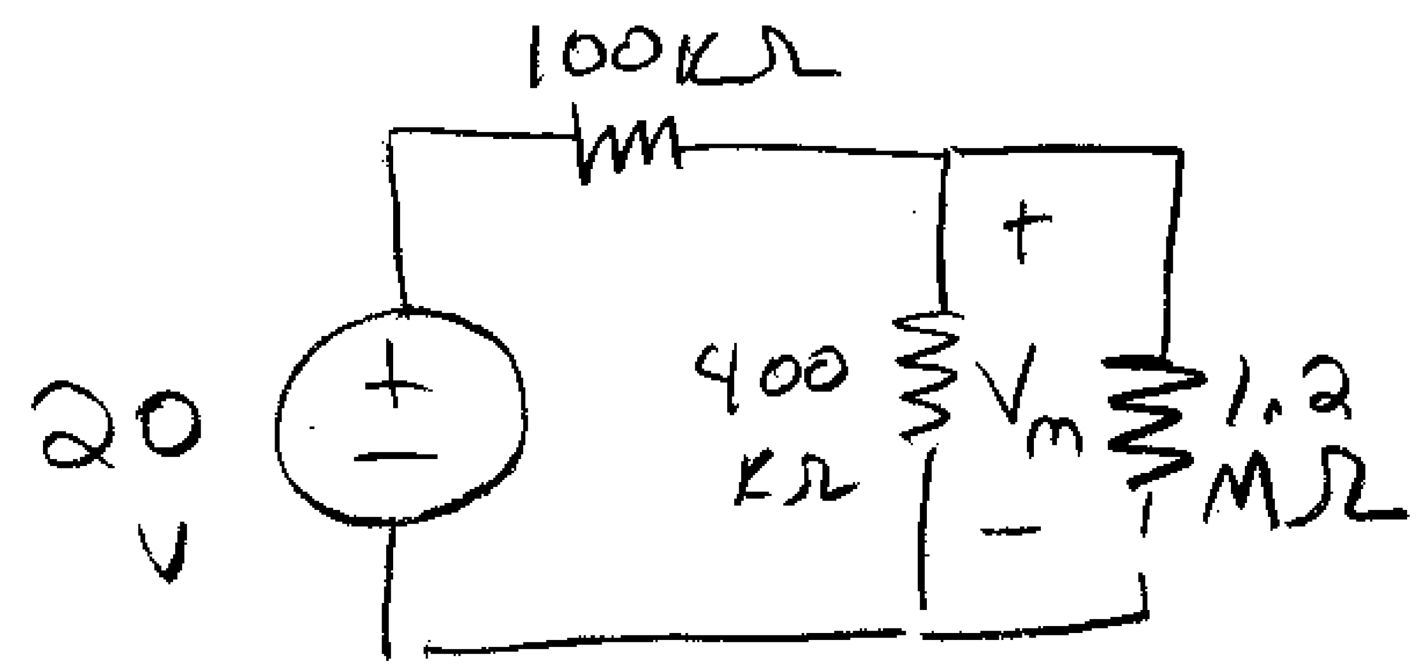
Name ____________________________________

Problem 1: 10 Points Possible

a) Suppose I measure the voltage over the 400 kΩ resistor using a voltmeter with an internal resistance of 1.2 MΩ. What is the voltage reading on the voltmeter?



Voltmeter placed in parallel with measured element:



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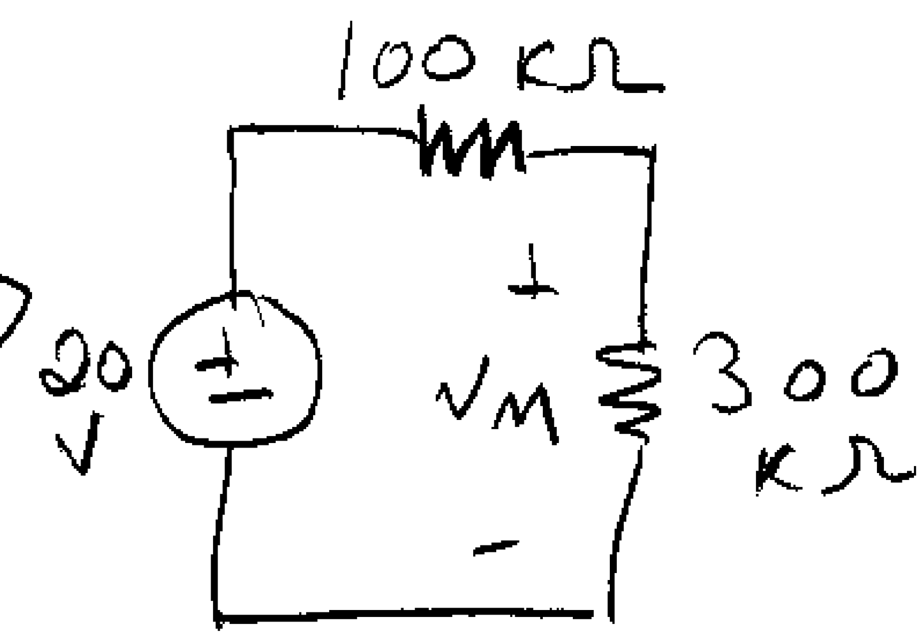


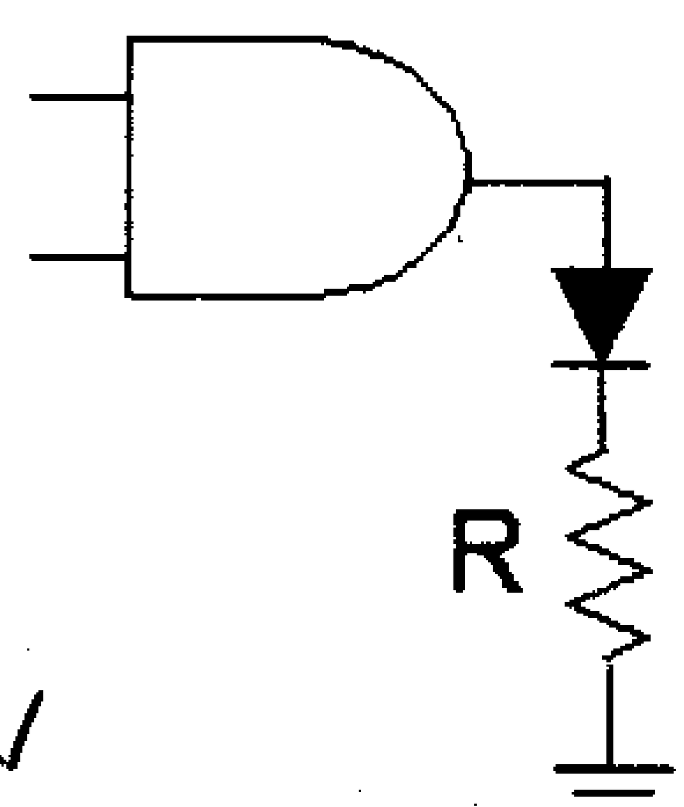
Voltage division:

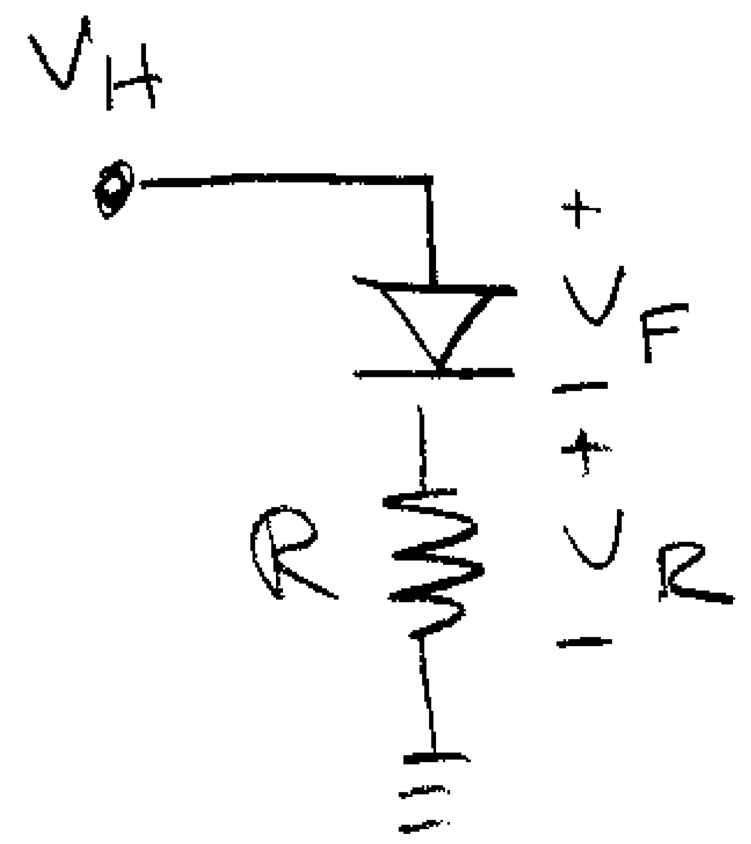
$V_M = 20\,V \cdot \frac{300k\Omega}{300k\Omega + 100k\Omega}$

$V_M = 15\,V$

b) I have attached a diode to the output of a logic gate, so it will light up when the output is high. Assume the large signal model for the diode, with V_F = 1 V.

Find the range of values for R that will satisfy the following condition: The diode must have between 20 mA and 50 mA of current when the logic output is between 4 V and 5 V.





V_H ranges from 4 to 5 V

V_F is always 1 V

V_R ranges from 3 to 4 V

Current through V_R will range from $\frac{3V}{R}$ to $\frac{4V}{R}$

$\frac{3V}{R} \geq 20\,mA \Rightarrow R \leq 150\,\Omega$

$\frac{4V}{R} \leq 50\,mA \Rightarrow R \geq 80\,\Omega$

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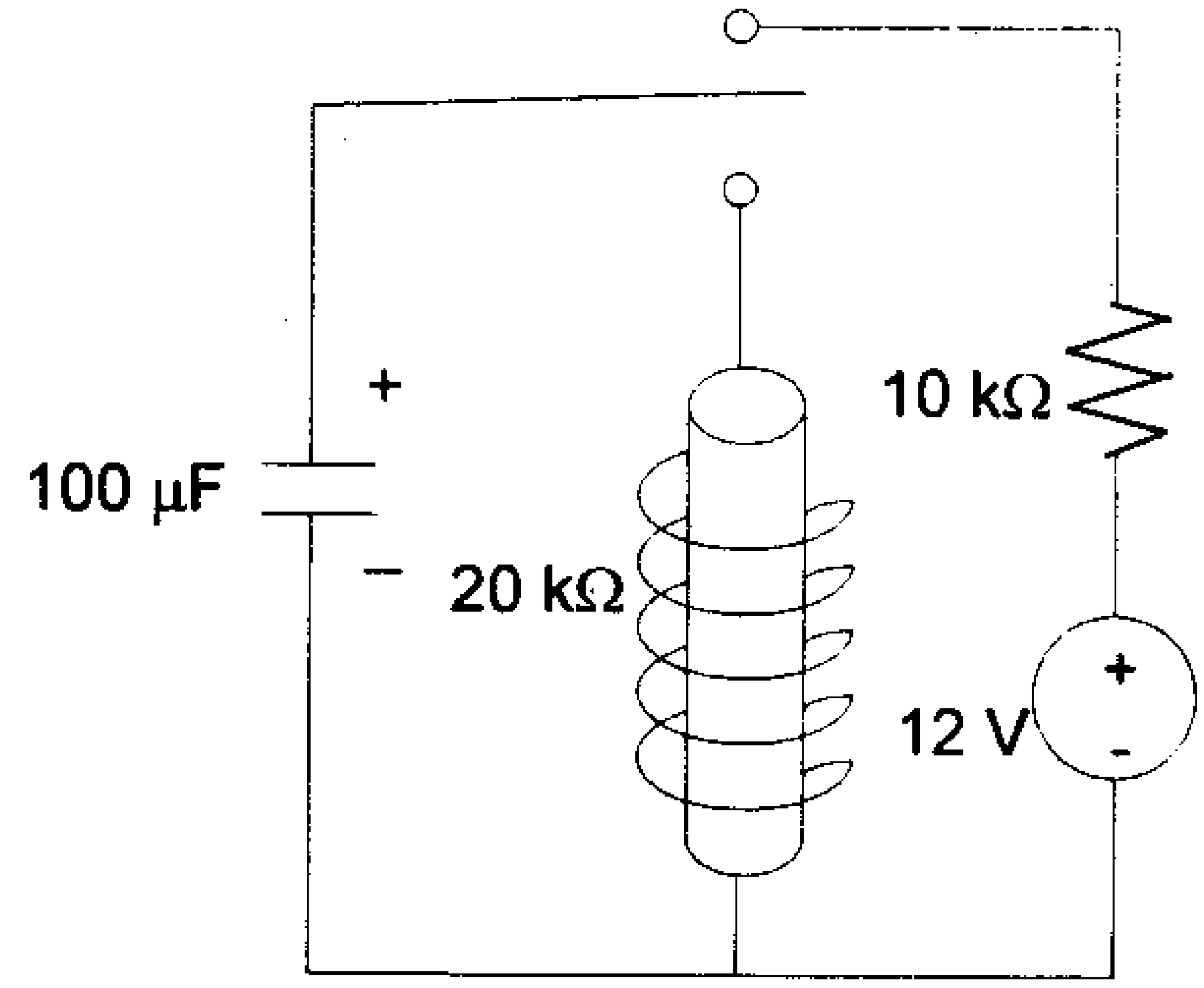
Problem 2: 10 Points Possible

Consider the relay circuit.

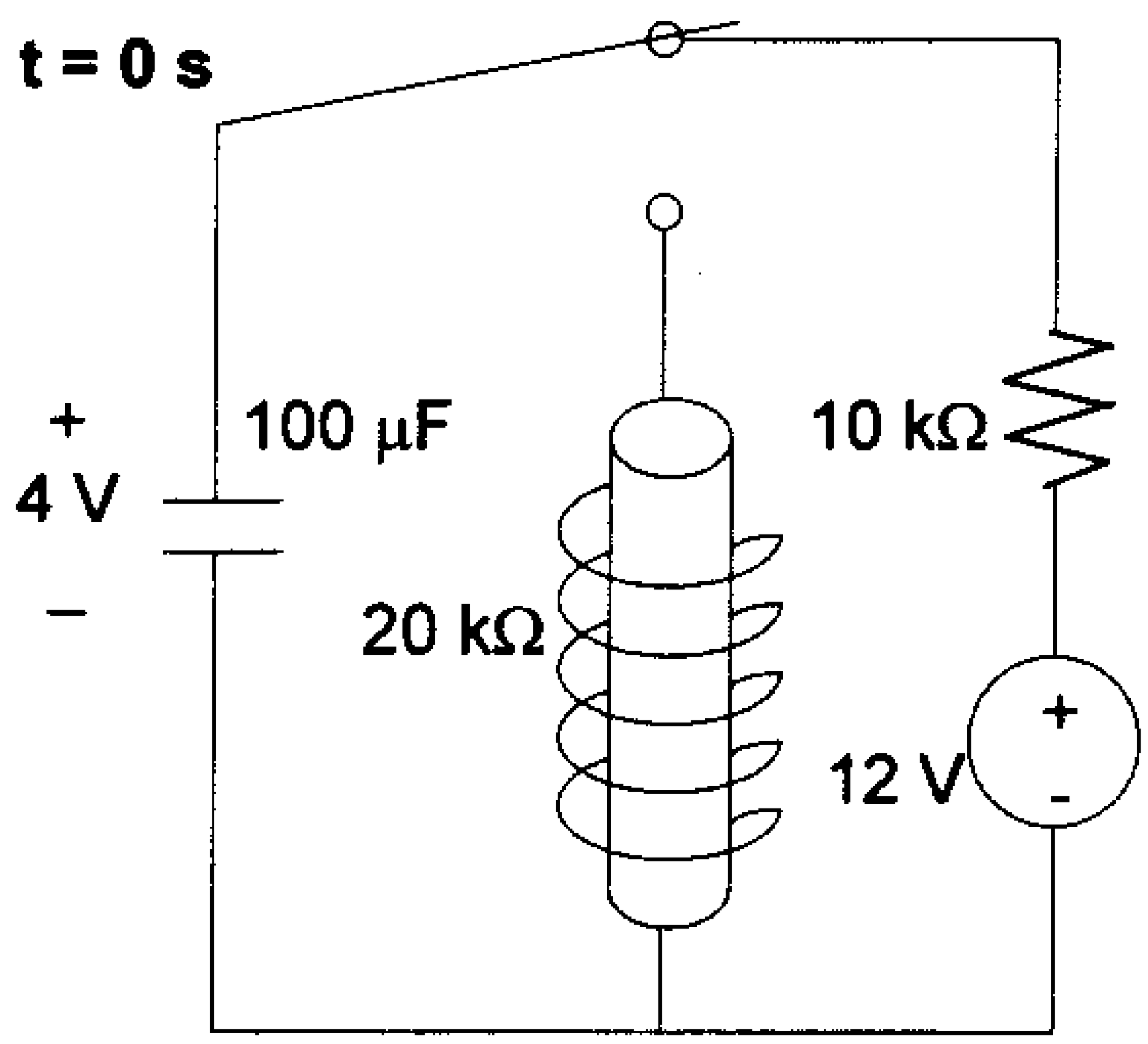
The 100 μF capacitor is connected to the 12 V source and 10 kΩ resistor when the switch is up, and connected to the 20 kΩ resistor representing the electromagnet coil when the switch is down.

The electromagnet keeps the switch in the "down" position until the coil voltage drops to 4 V; at that point, the magnet releases the switch and it springs back up.



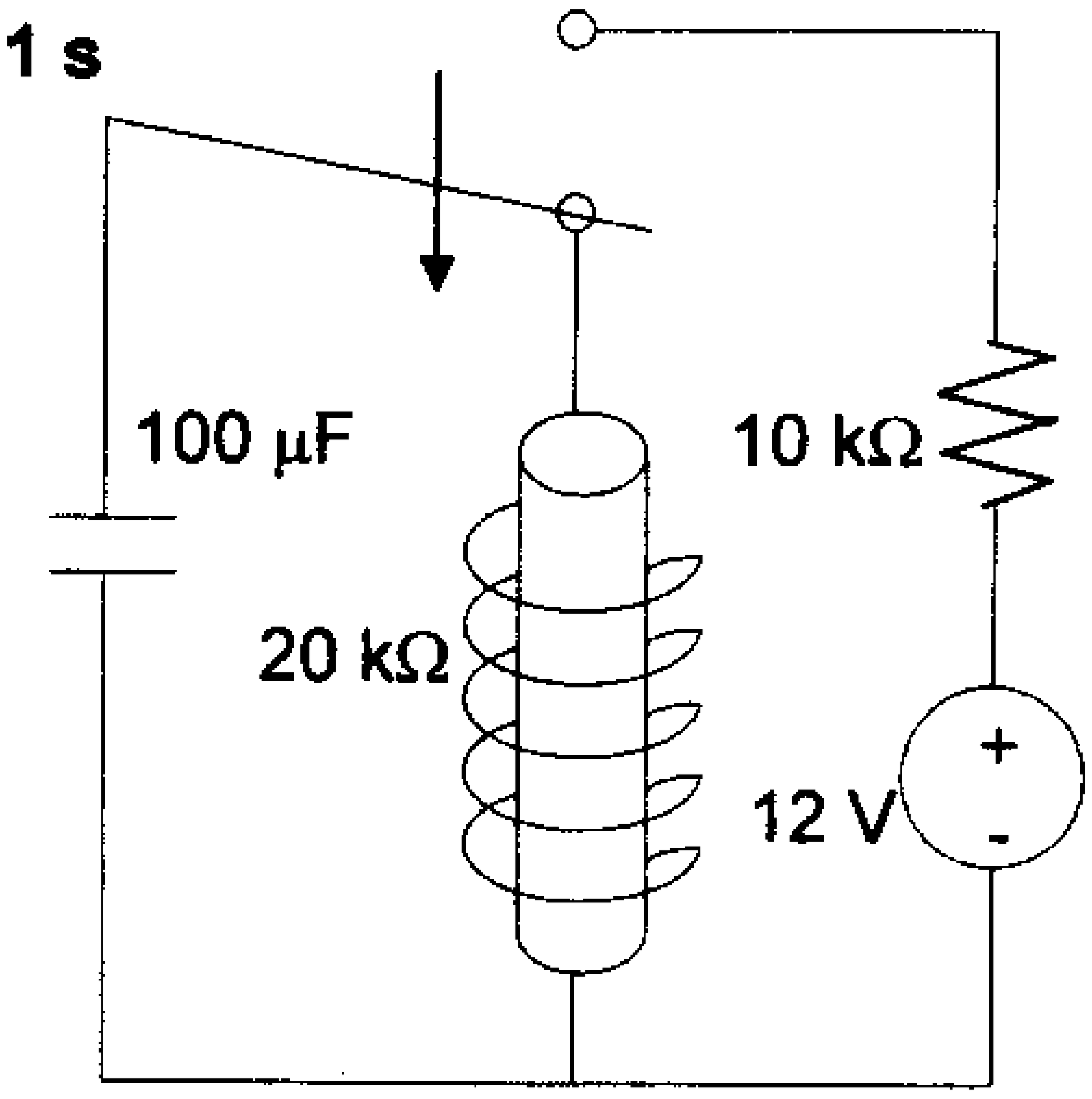
Suppose that at t = 0, the capacitor has voltage 4 V with polarity shown, and the switch is up.

t = 0 s



At t = 1 second, I flip the switch down (and let go).

t = 1 s



How long will the switch stay down?

Capacitor starts discharging at t = 1 s

What is initial capacitor voltage at t = 1 s?

Capacitor was charging for t = 0 to t = 1

$V_c(t) = 4V e^{-t/\tau} + 12V(1 - e^{-t/\tau})$ $\tau = 100\mu F \cdot 10k\Omega = 1s$

$V_c(1s) = 4V \underbrace{e^{-1s/1s}}_{0.37} + 12V \underbrace{(1 - e^{-1s/1s})}_{0.63} = 9.04V$

How long does discharging from 9.04V to 4V take?

$4V = 9.04V e^{-t/\tau}$ $\tau = 100\mu F \cdot 20k\Omega = 2s$

$t = -2s \cdot \ln \frac{4V}{9.04V} =$ **1.63 s**

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Problem 3: 10 Points Possible

Determine whether the circuit below performs a logical operation.

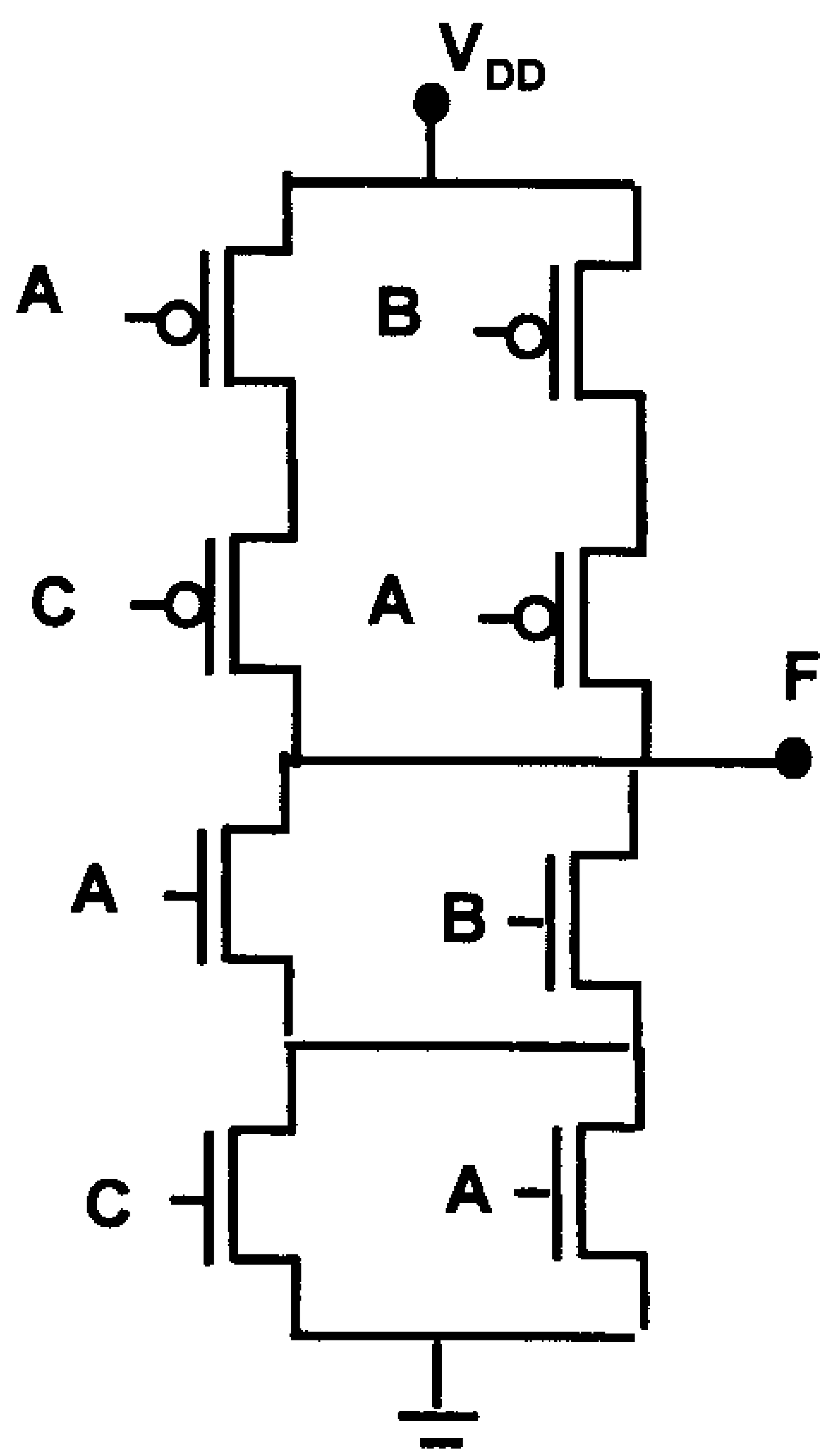
If the circuit **does** perform a logical operation,

a) give the Boolean function it computes, and
b) design a circuit that computes the same function using fewer transistors.

If the circuit **does not** perform a logical operation,

a) give a set of inputs that results in an invalid output, and
b) rearrange the inputs so that the circuit does perform some logical operation.

For your convenience, 8 copies of this circuit are given on the next page. Assume that all PMOS transistors have source terminal on top, and all NMOS transistors have source terminal on the bottom.



To connect F to V_{DD}: $F = \bar{A}\bar{C} + \bar{A}\bar{B}$

To connect F to ground: $\bar{F} = (A+B)(C+A)$

Use De Morgan: $F = \overline{(A+B)(C+A)} = (\overline{A+B}) + (\overline{C+A})$

$= \bar{A}\bar{B} + \bar{C}\bar{A}$ Agrees with PMOS half!

Logical operation performed: $F = \bar{A}\bar{C} + \bar{A}\bar{B}$

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Problem 3 Workspace

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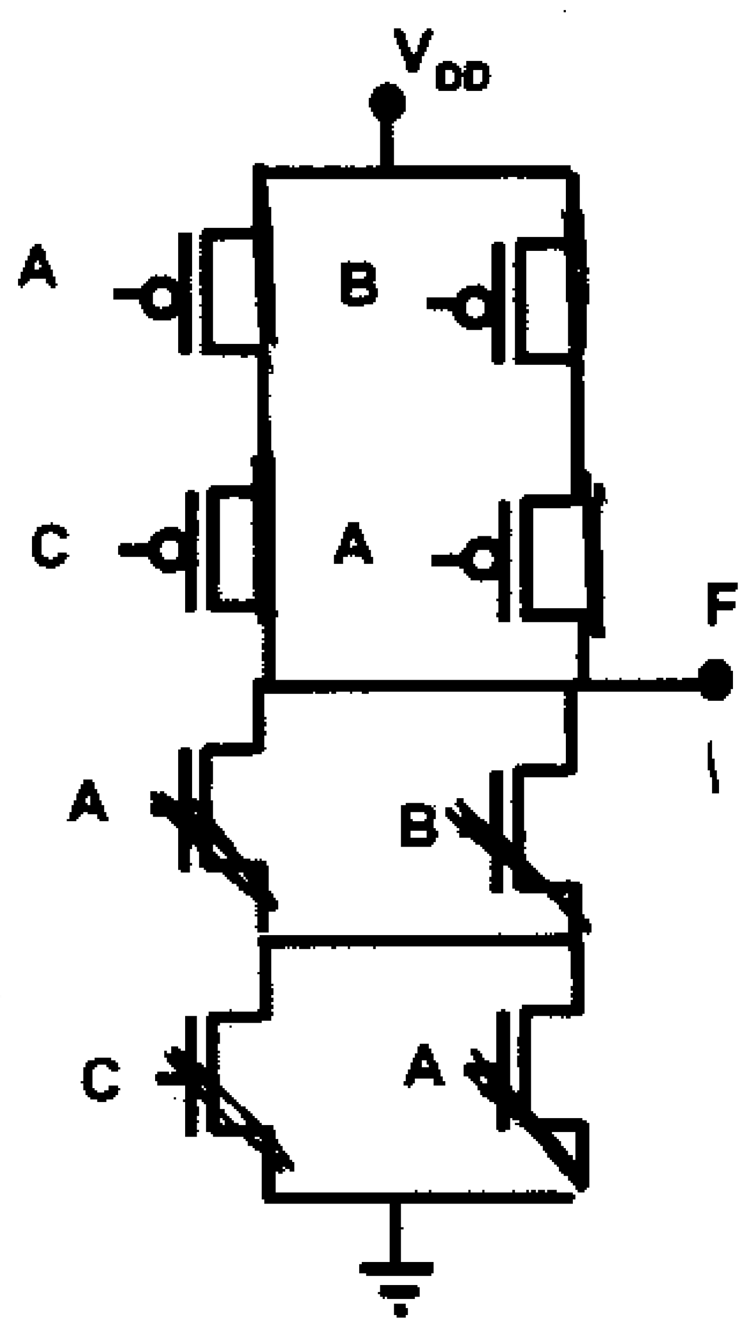

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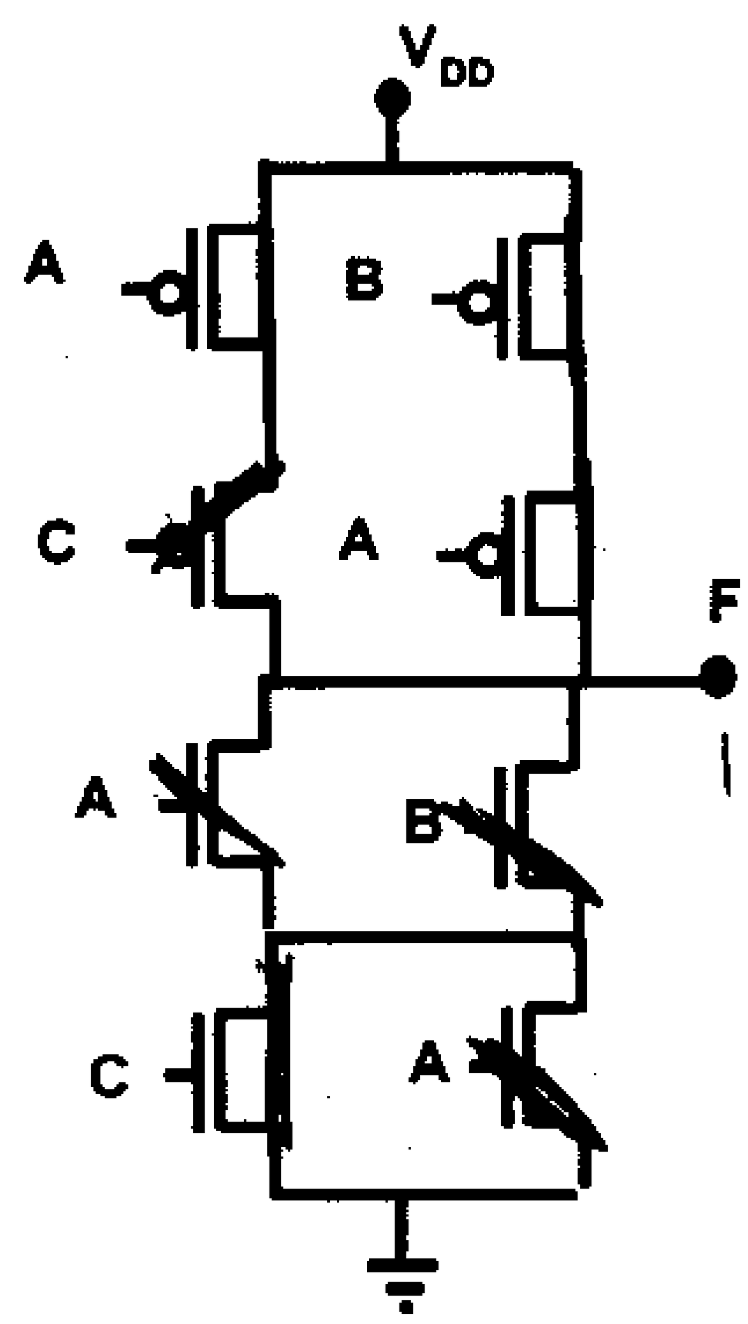

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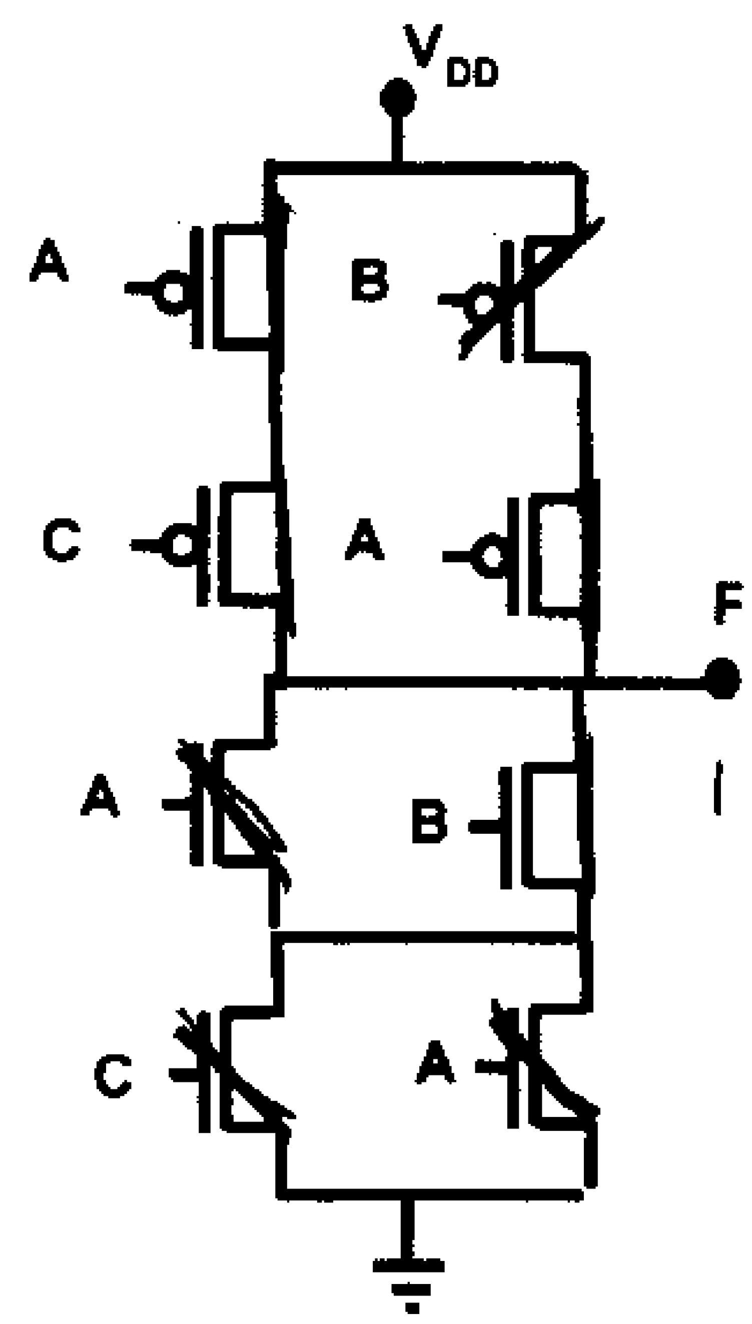

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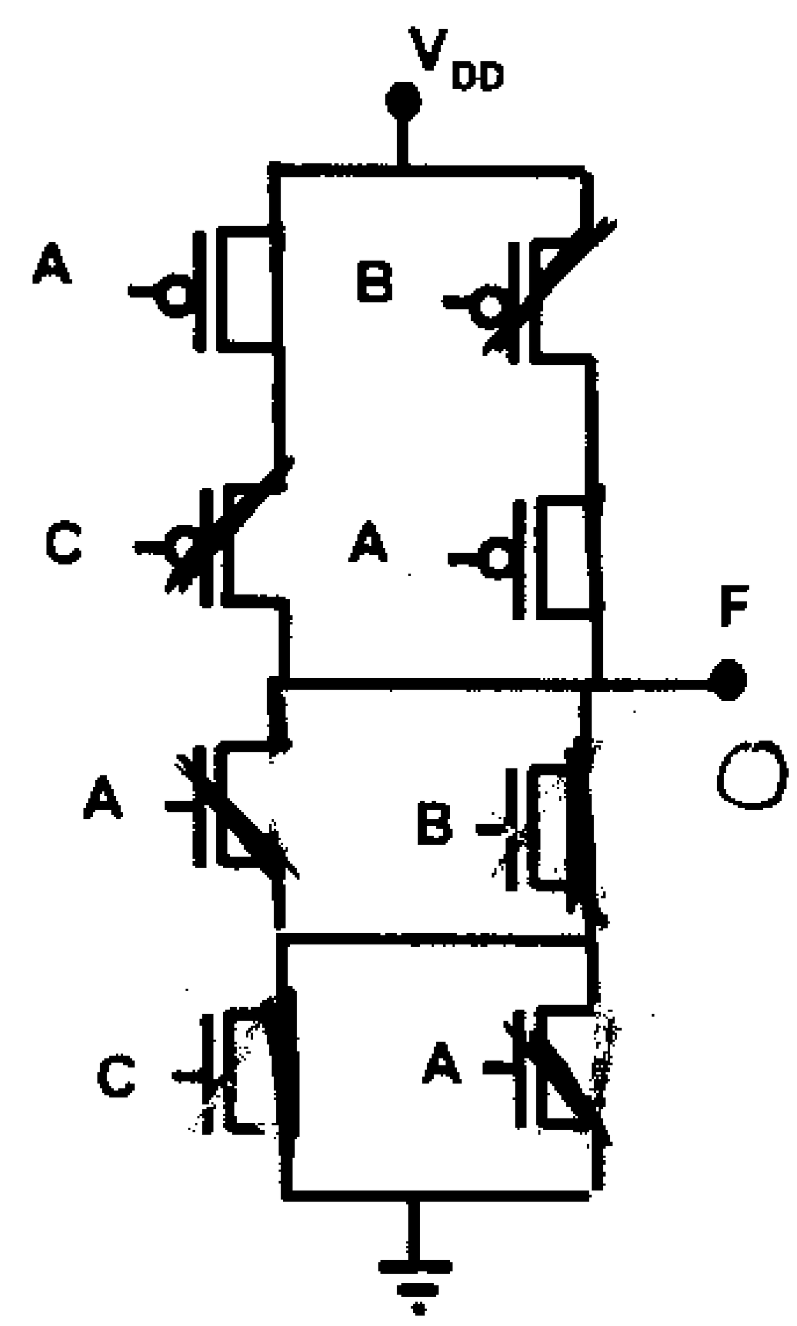

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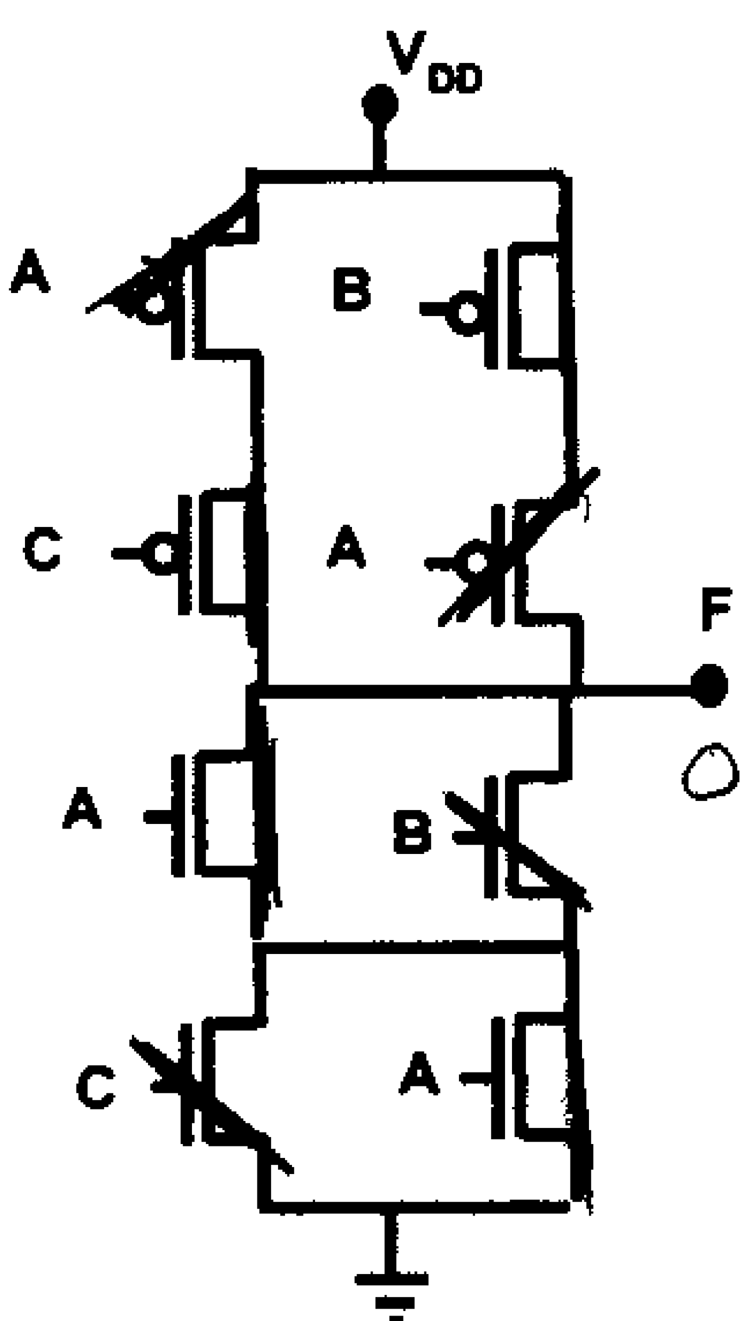

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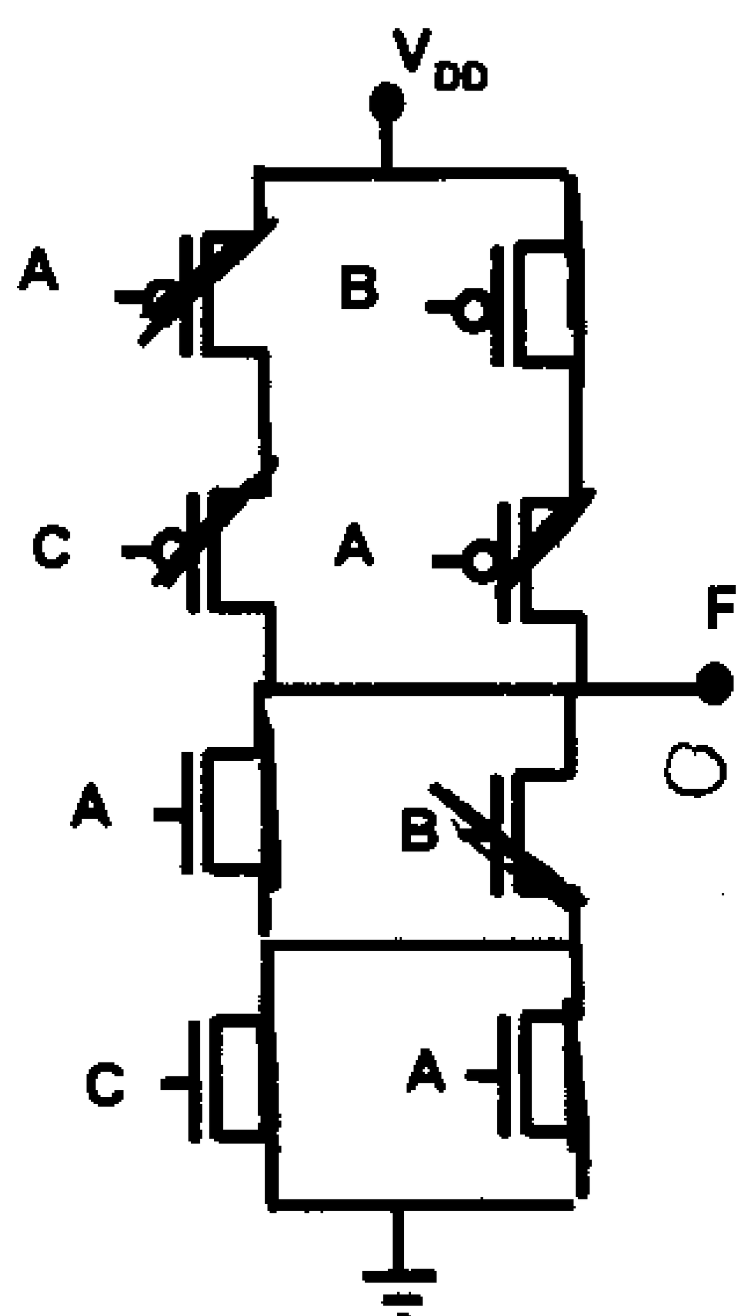

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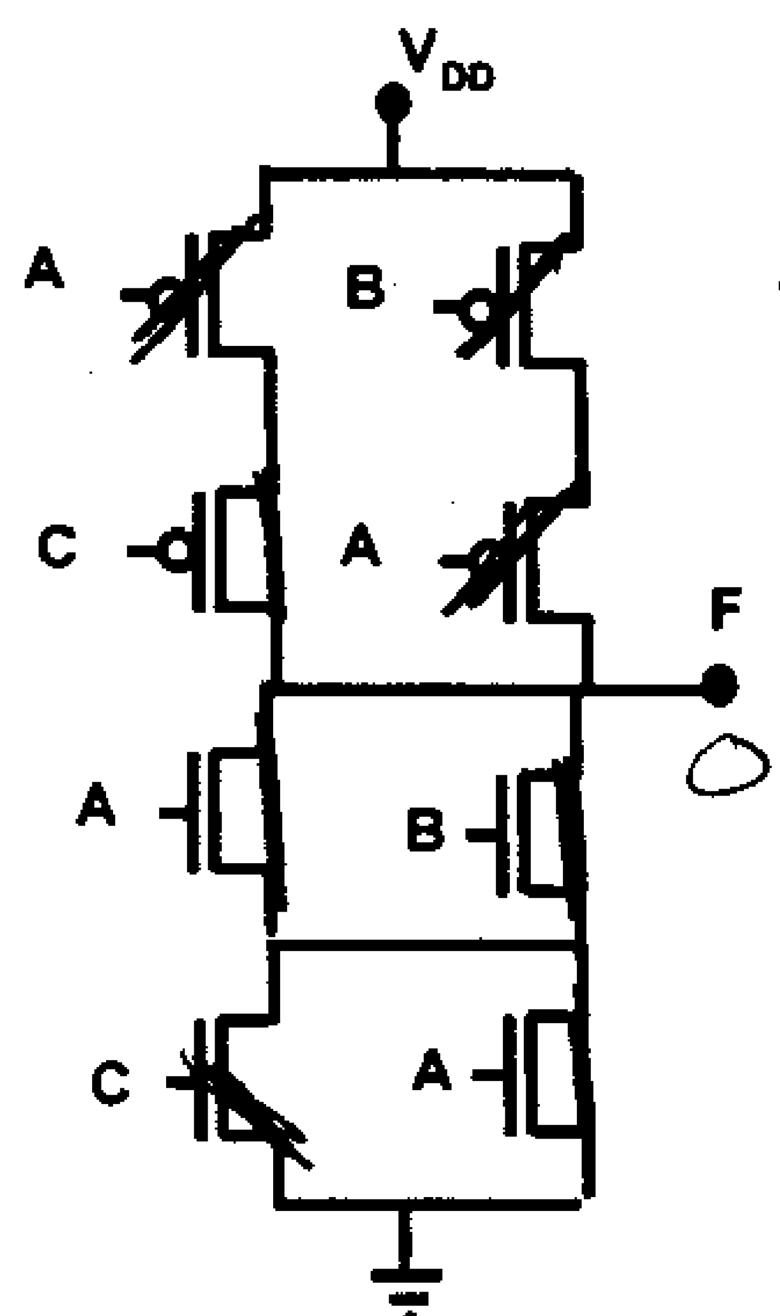

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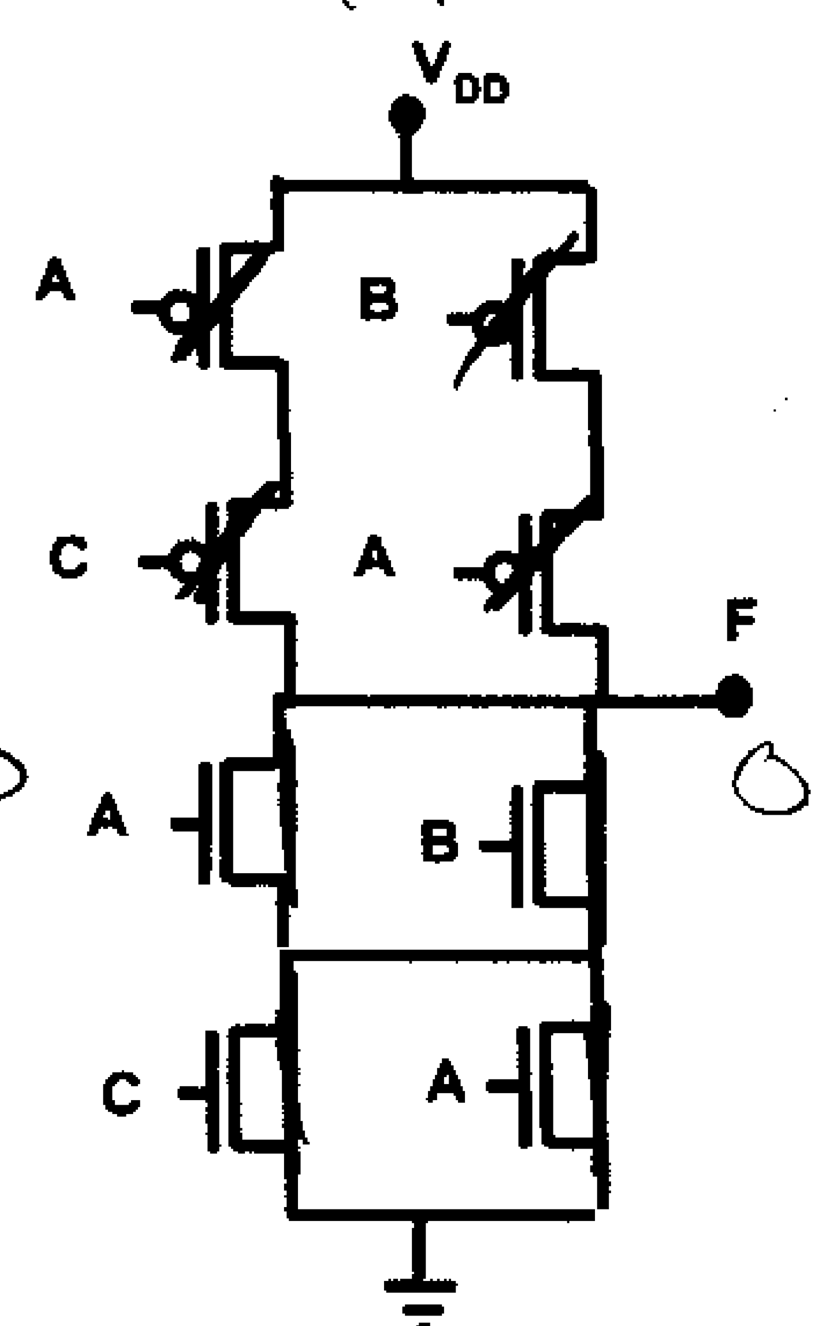

$$F = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}\,B\,\overline{C}$$

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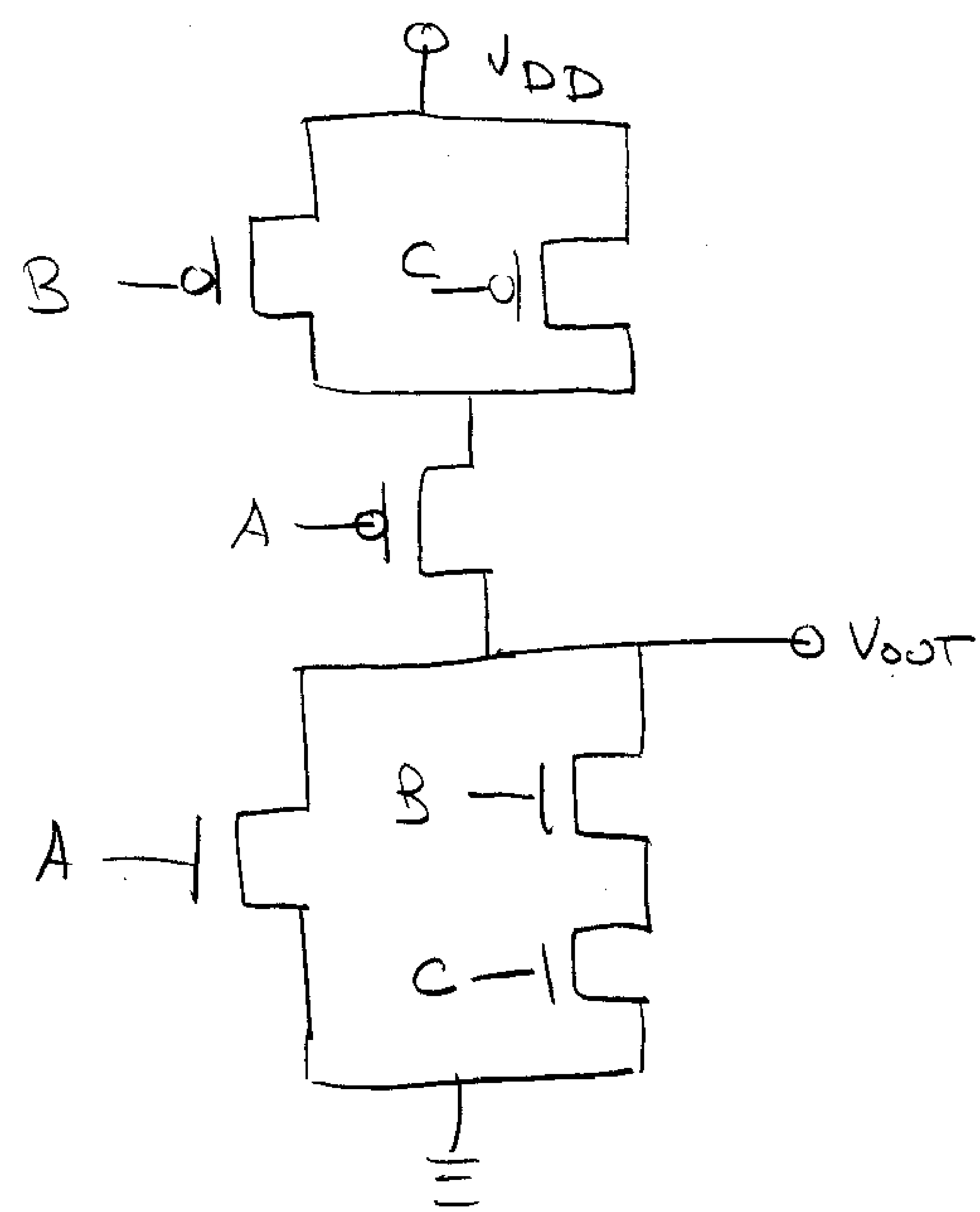
Problem 3 Workspace

Simpler expression is $F = \bar{A}(\bar{B}+\bar{C})$

Pmos: A input in series with (B input, C input in parallel)

NMOS is complement: A input in parallel with (B input, C input in series)



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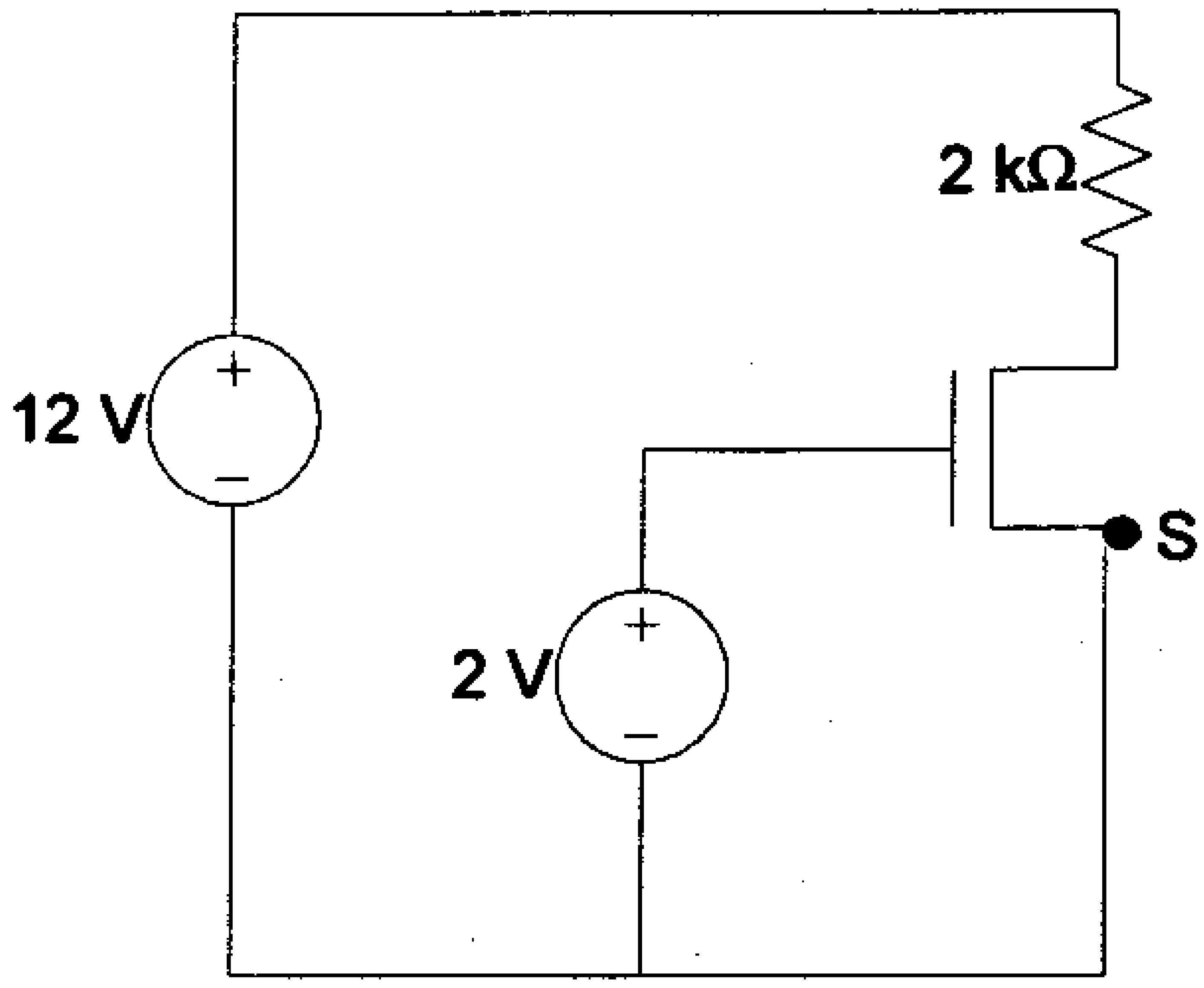
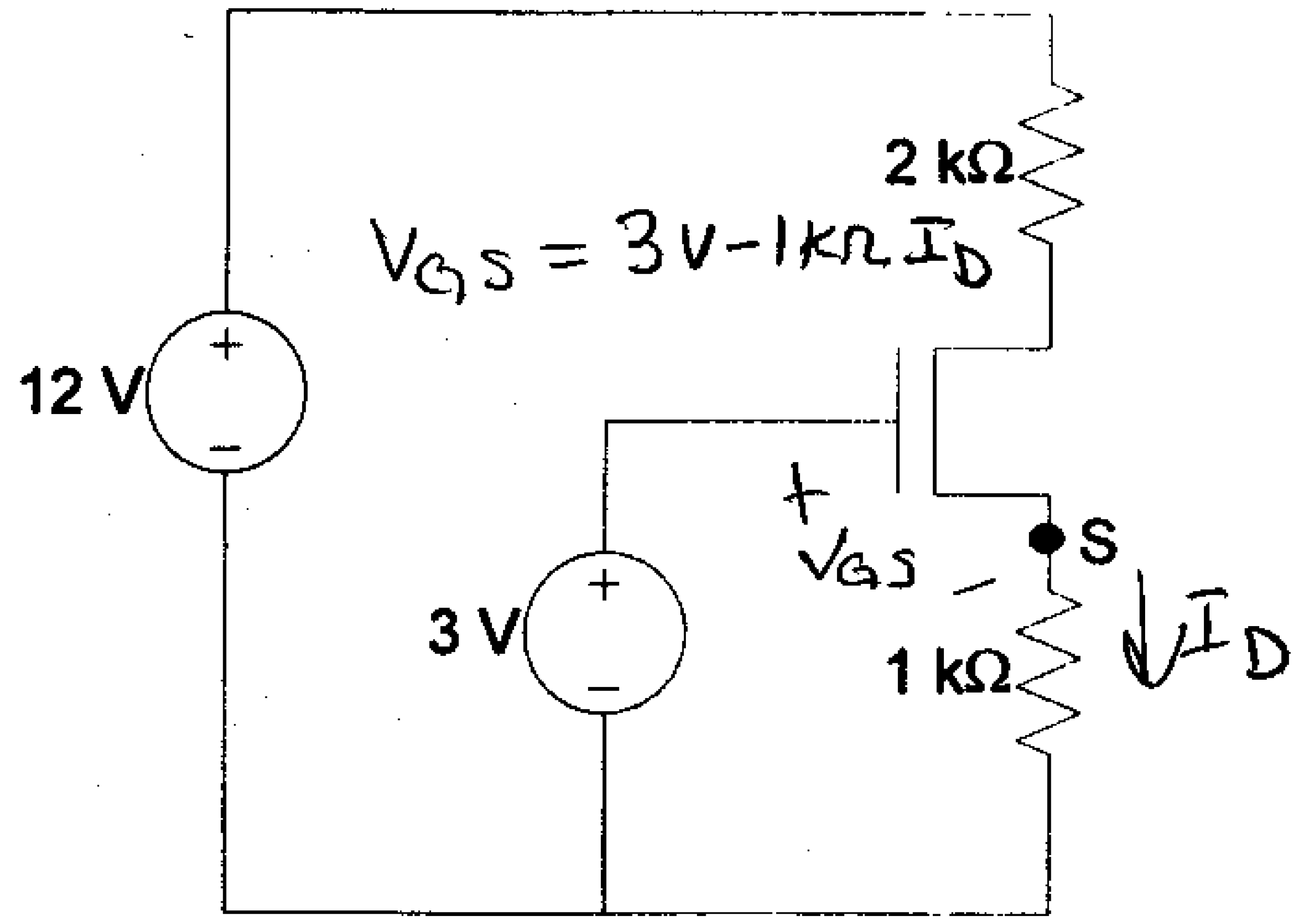
Problem 4: 15 Points Possible



Circuit A



Circuit B

Consider the two circuits above, where $W/L\ \mu_N C_{OX} = 2\ mA/V^2$, $V_{TH} = 1\ V$, and $\lambda = 0$ for both transistors, at room temperature. In this situation, both transistors are in saturation, with constant $I_D = 1\ mA$.

Suppose the circuit temperature rises significantly, doubling μ_N (not realistic, but bear with me).

Find the I_D values for the higher temperature: $I_{D(A)}$ for Circuit A and $I_{D(B)}$ for Circuit B.

$$I_{D_A} = \tfrac{1}{2} \cdot \tfrac{W}{L} \mu_N C_{ox} (V_{GS} - V_{TH})^2 = \tfrac{1}{2} \cdot 4mA/V^2 (2V - 1V)^2$$

$I_{DA} = 2mA$ $\quad V_{DS_A} = 12V - 2k\Omega \cdot 2mA = 8V$ Ok.

$$I_{D_B} = \tfrac{1}{2} \cdot \tfrac{W}{L} \mu_N C_{ox} (V_{GS} - V_{TH})^2 = \tfrac{1}{2} \cdot 4mA/V^2 (3V - 1k\Omega I_{D_B} - 1V)^2$$

$$0 = 2000 I_{D_B}^2 - (8+1) I_{D_B} + .008$$ $\quad I_{D_B} = 1.22mA$

Solutions: $I_{D_B} = \{3.28\ mA,\ 1.22mA\}$

V_{GS_B} for $I_{D_B} = 3.28\ mA$: $\quad V_{GS_B} = 3V - 1k\Omega(3.28mA)$
$= -0.28V$ Impossible!

V_{GSB} for $I_{DB} = 1.22mA$: $\quad V_{GSB} = 3V - 1k\Omega(1.22mA)$
$= 1.78\ V$ Ok.

V_{DS_B} for $I_{D_B} = 1.22mA$: $\quad V_{DSB} = 12V - 3k\Omega(1.22mA) = 8.34V$
Ok.

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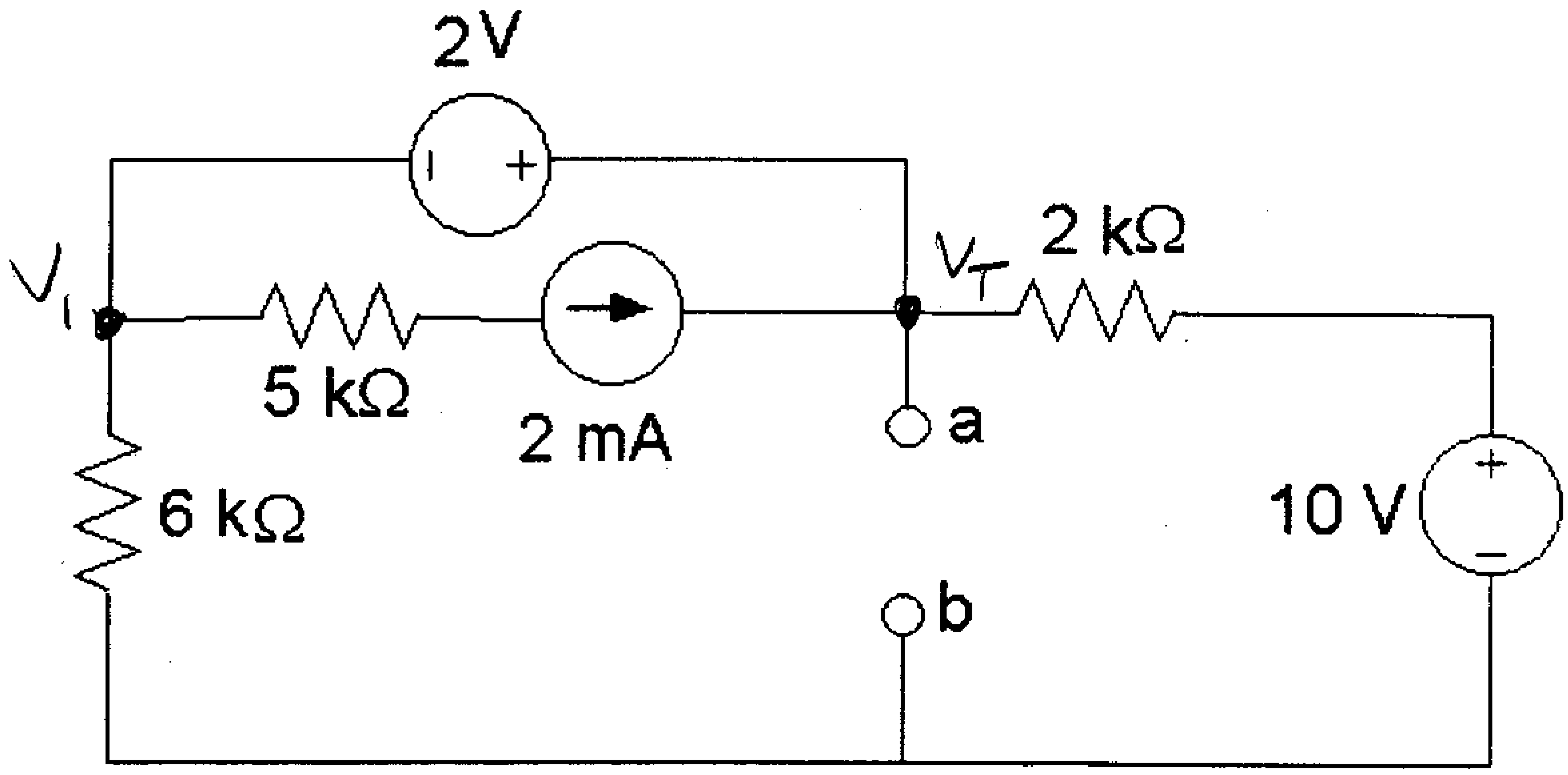
Problem 5: 15 Points Possible

Find the Thevenin equivalent circuit with respect to points a and b for the circuit below.



Find open-circuit voltage from a to b:

Nodal analysis with nodes above:

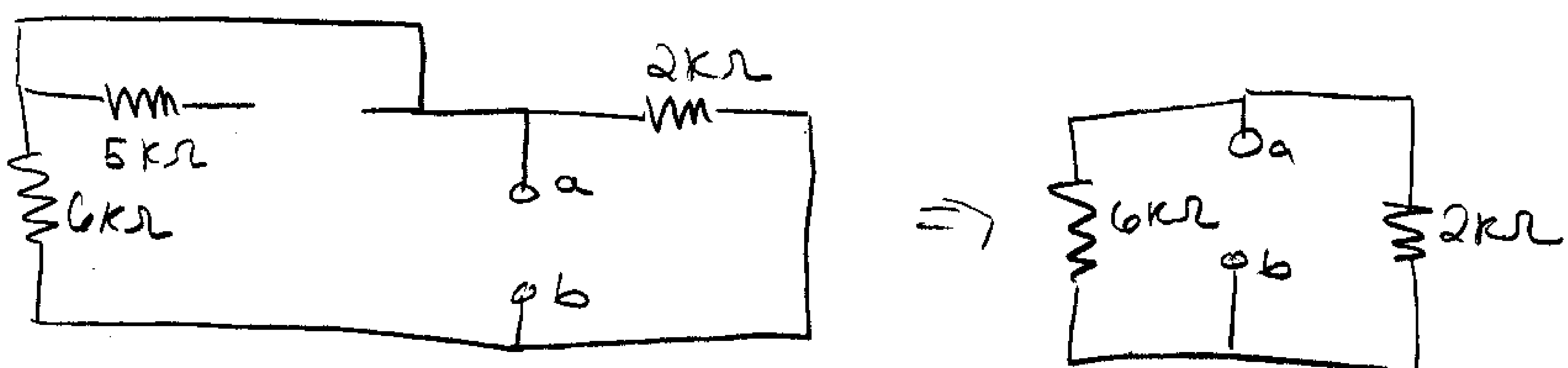
$$\underbrace{\frac{V_1}{6k\Omega} + \frac{V_T - 10}{2k\Omega} = 0}_{\text{supernode}} \qquad V_T - V_1 = 2V$$

Solution:

$V_T = 8V$

$V_1 = 6V$

Find R_T by turning off sources:



$R_T = 6k\Omega \parallel 2k\Omega = 1.5\,k\Omega$

Source transformations also work here.

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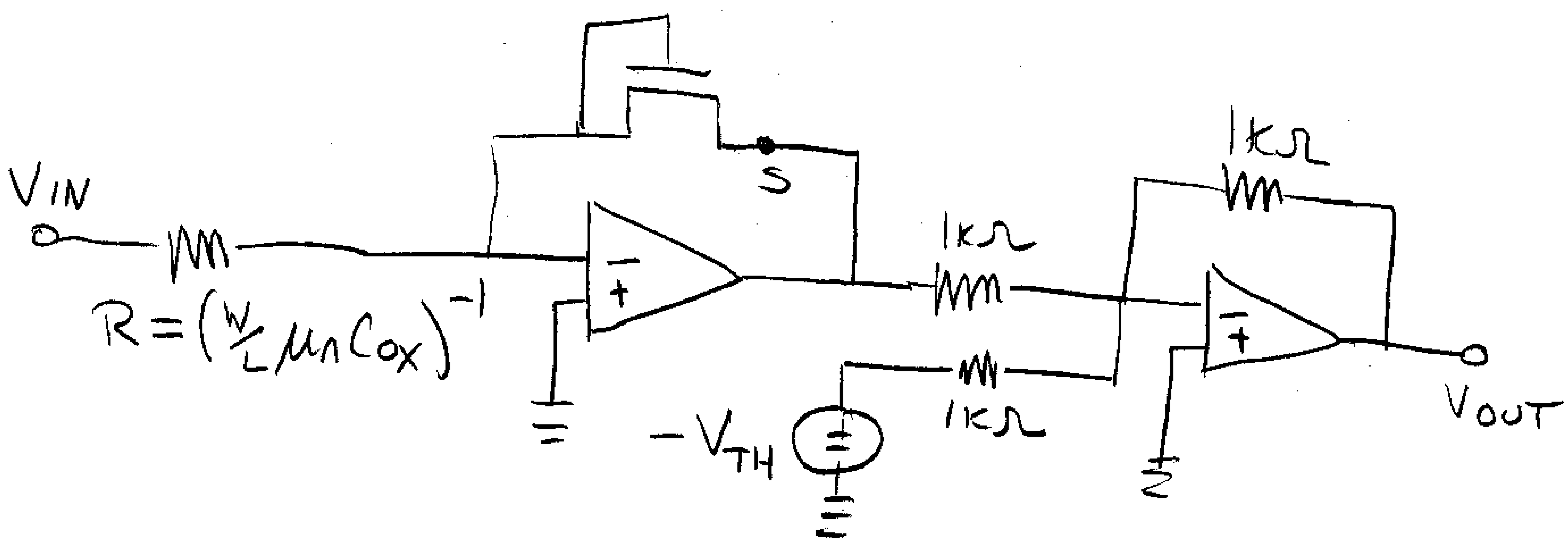
Problem 6: 45 Points Possible

Complete 3 of the following 5 choices worth 15 Points each. If you complete more than 3 choices, your 3 highest-scoring choices will count towards your Problem 6 total.

Problem 6 Choice 1:

Design a circuit for which $V_{OUT} = \sqrt{V_{IN}}$.

Your design only needs to work "on paper".



One of many possible designs.

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Problem 6 Choice 2:

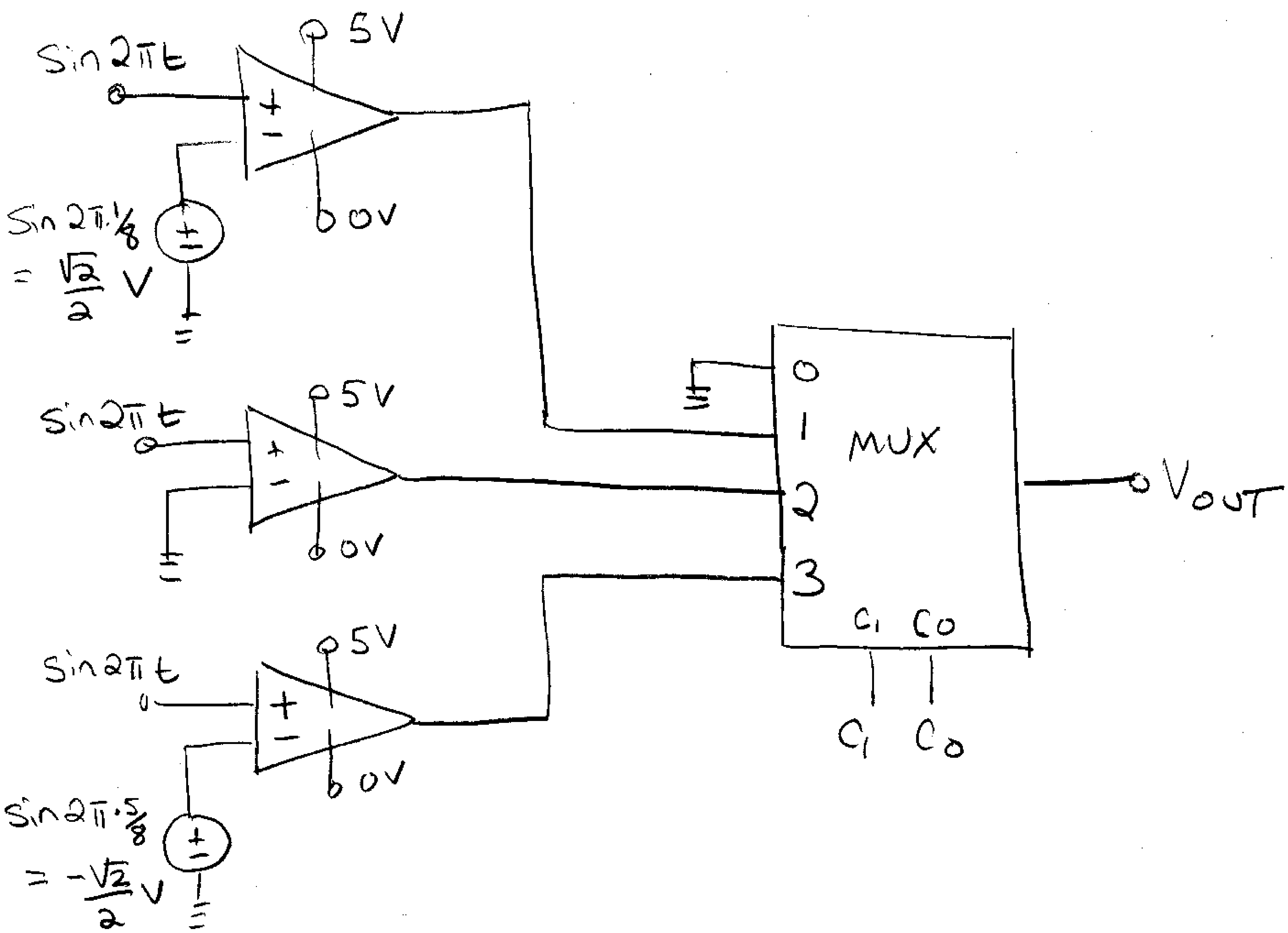
You are given an input $V_{IN} = \sin 2\pi t$.

Design a circuit that creates 1 Hz square waves of duty cycle 25%, 50%, and 75%.
(Duty cycle is the percentage of time that a square wave is high.)
The low and high values for the square waves should be logic 0 (0V) and logic 1 (5 V) respectively.

The circuit output should be:

0 V when the binary control signal $C_1\ C_0$ = 0 0
25% duty cycle wave when $C_1\ C_0$ = 0 1
50% duty cycle wave when $C_1\ C_0$ = 1 0
75% duty cycle wave when $C_1\ C_0$ = 1 1 .

You may use any of the circuits discussed in class, including the multiplexer.



If you use Schmitt Triggers, you must "trick" them to handle 0 or negative thresholds by adding negative offset voltage to ground + V_{DD} terminals.

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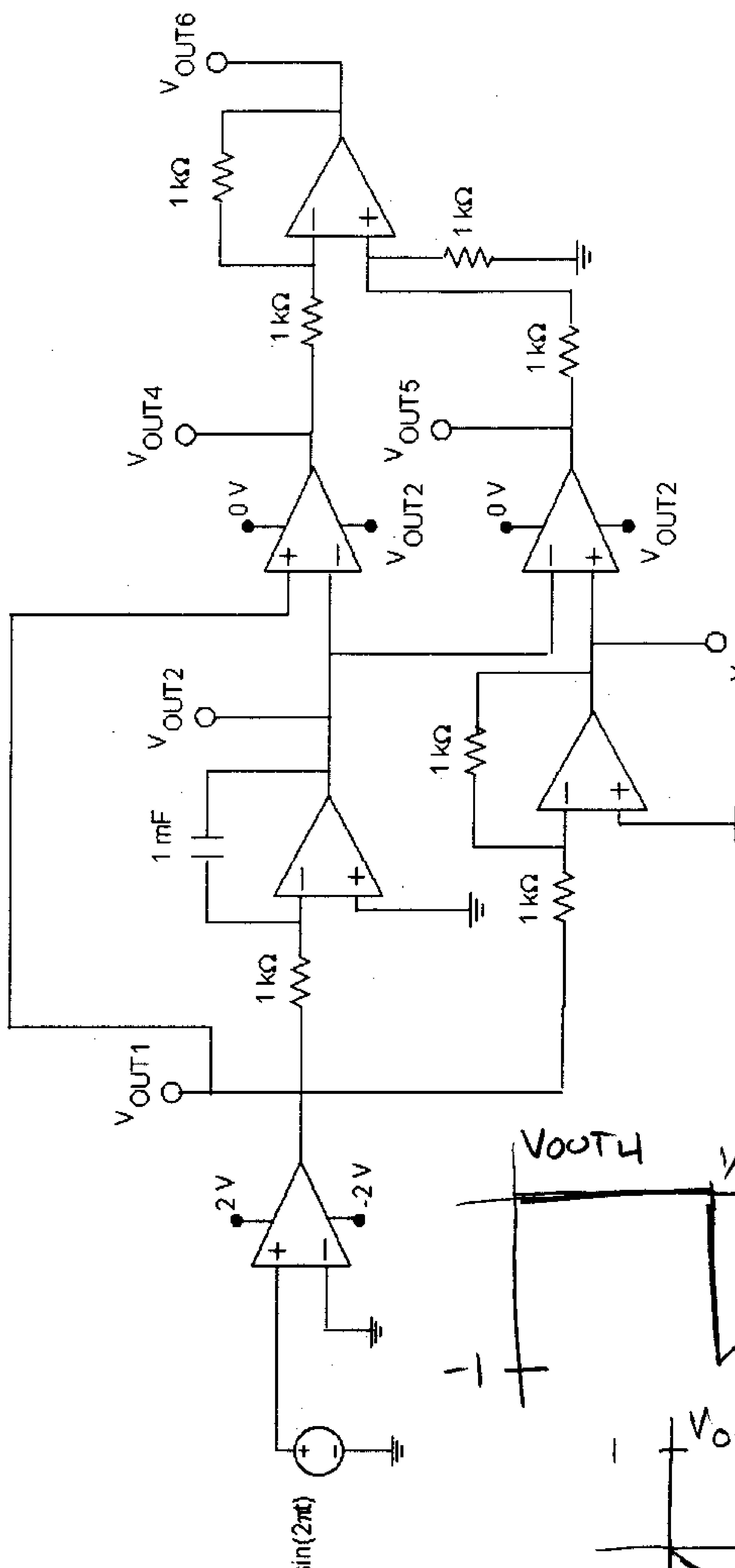
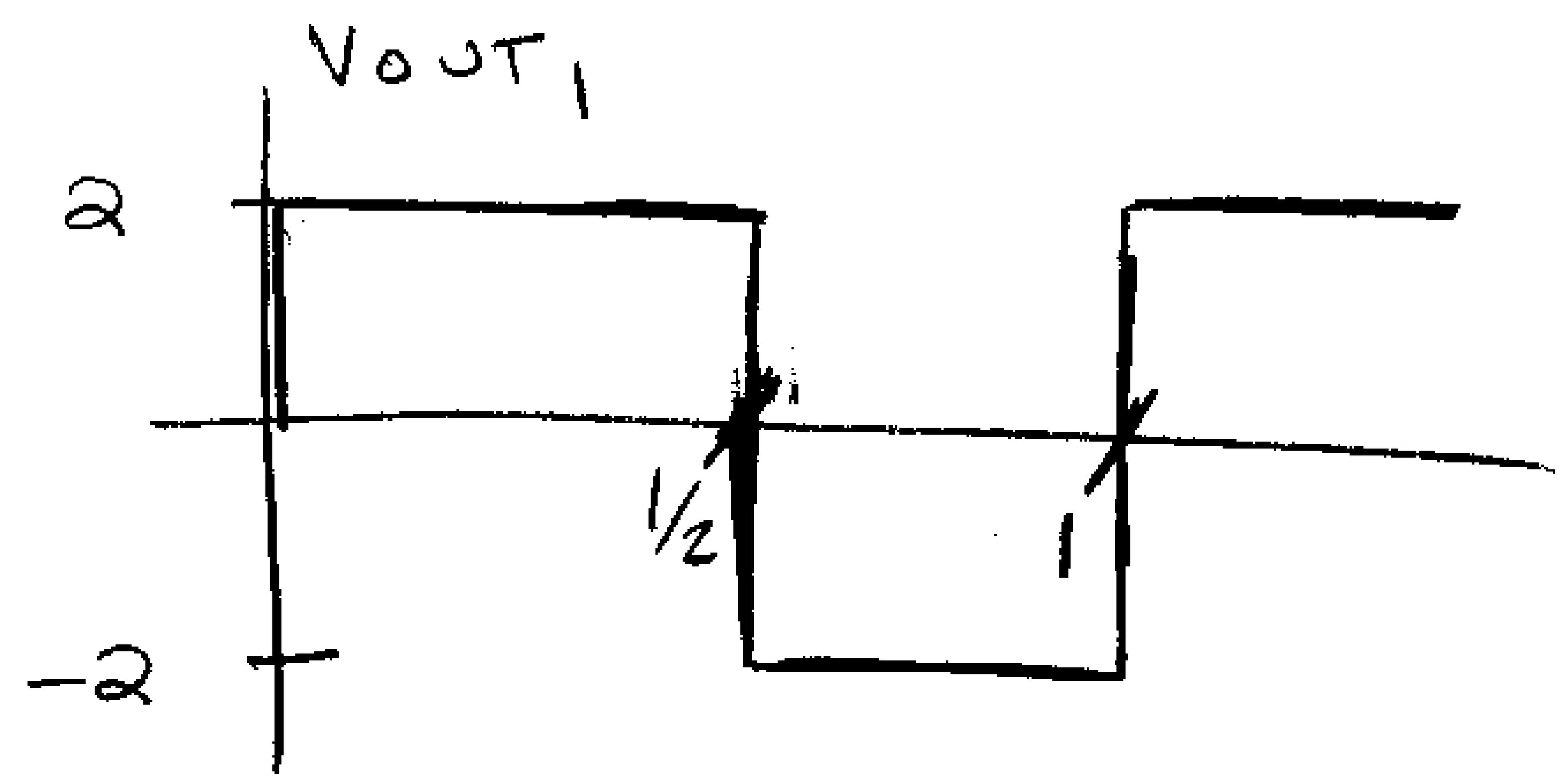
Problem 6 Choice 3

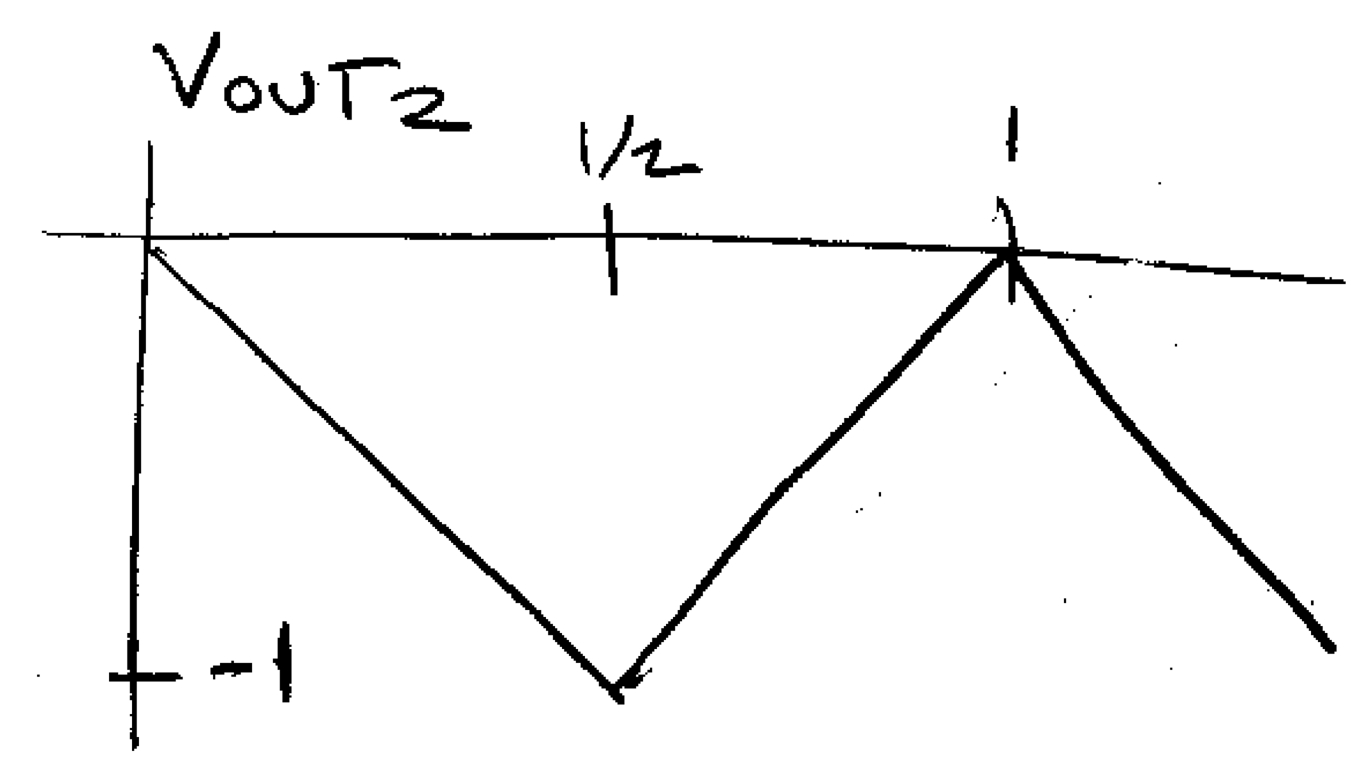
Sketch V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}, V_{OUT5}, and V_{OUT6} for the following circuit.

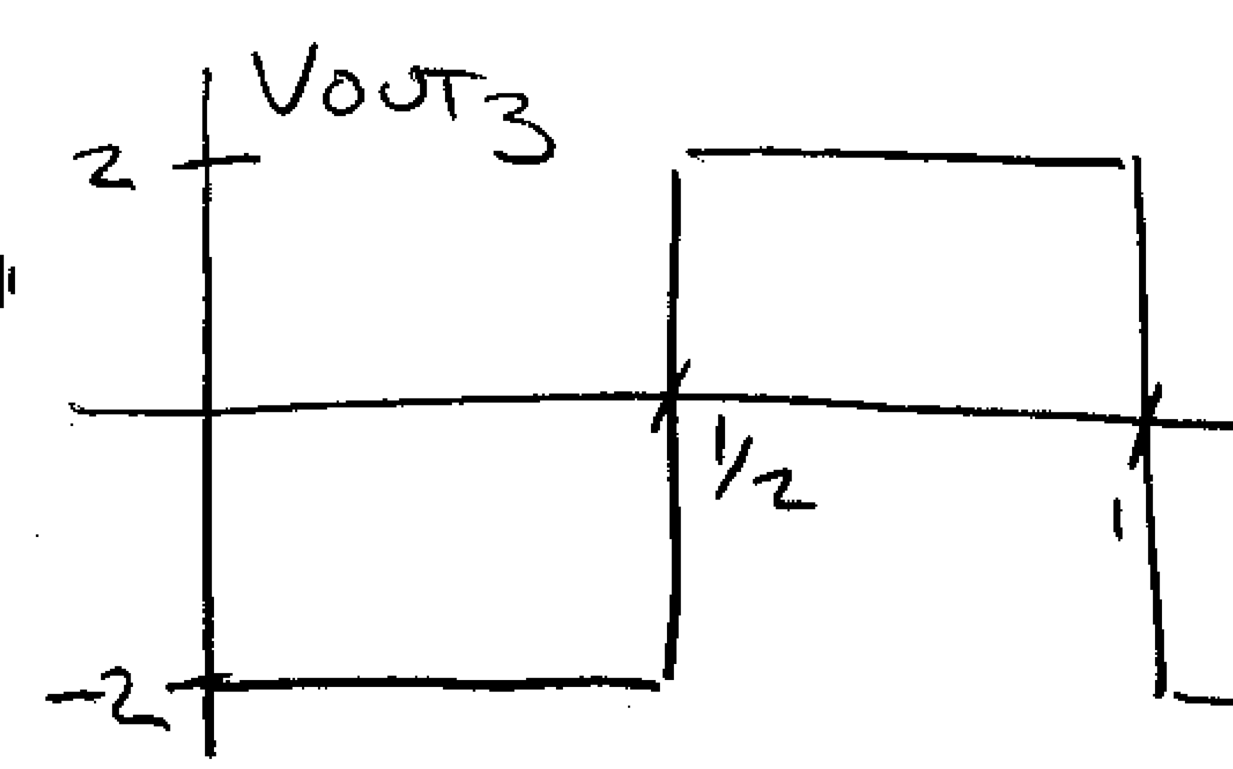
Be sure to show peak values. Pay close attention to time intervals and +/- terminals on amplifiers.

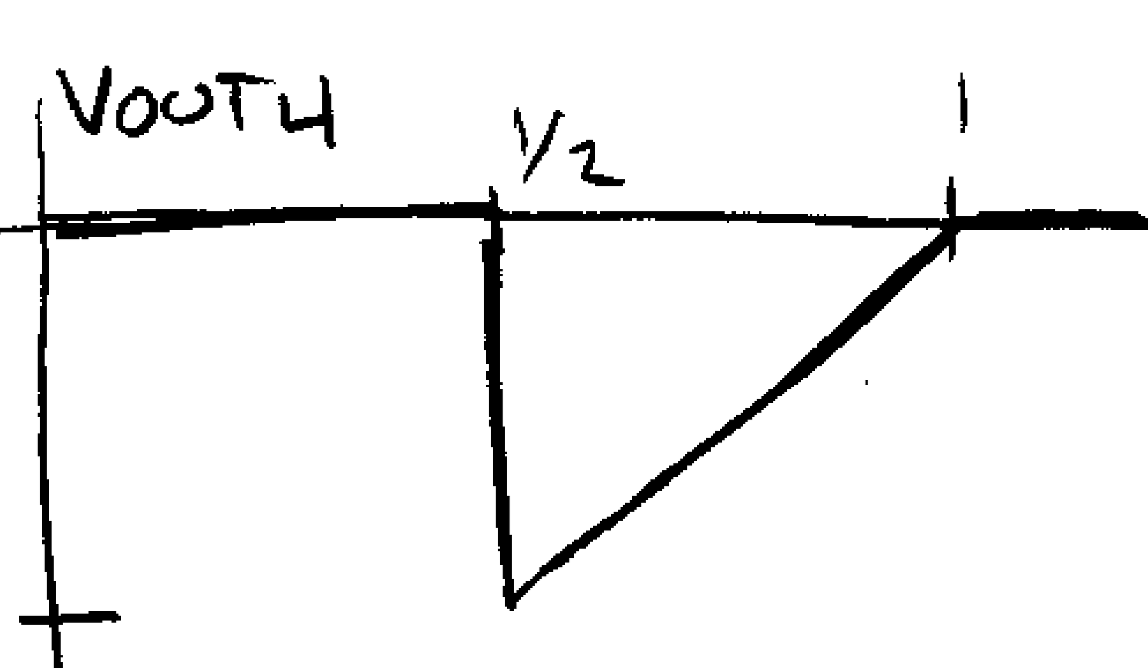
Assume that the capacitor is discharged at t = 0. Use the ideal diode model.

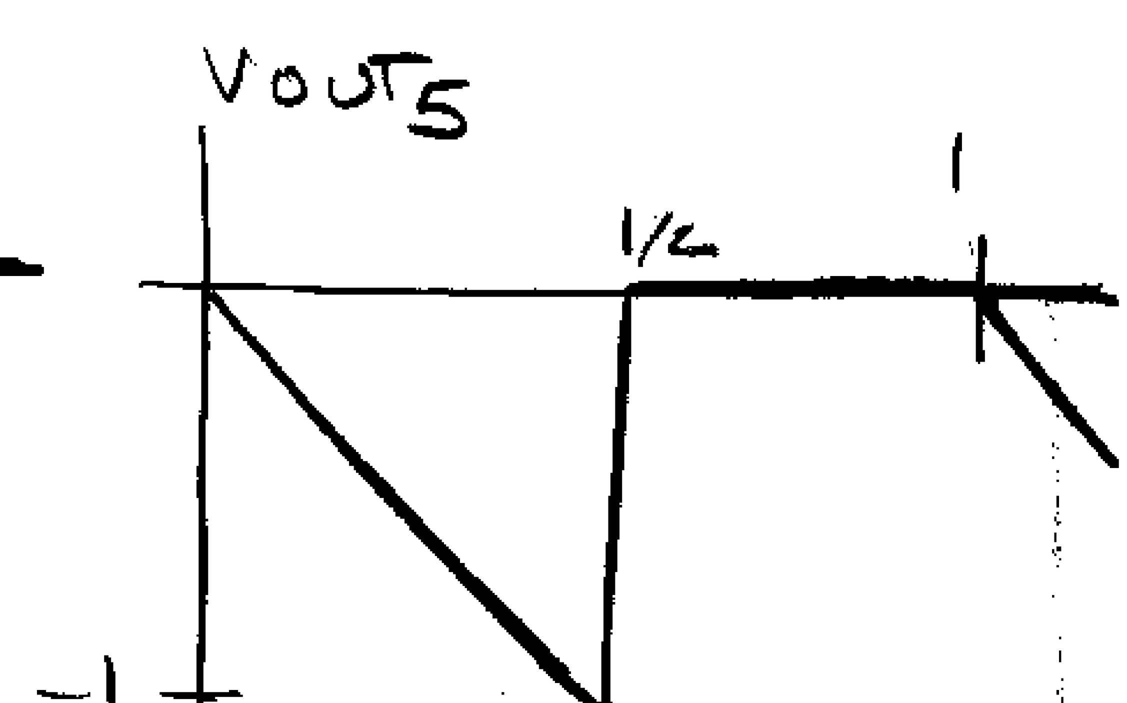


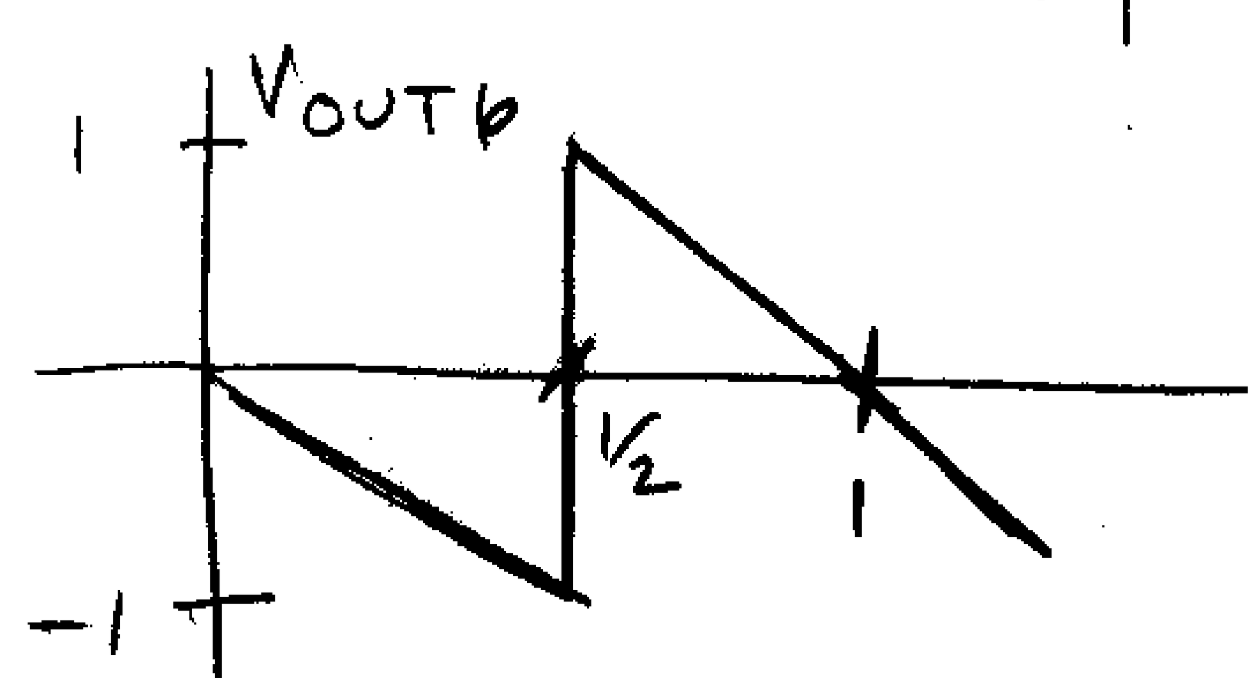












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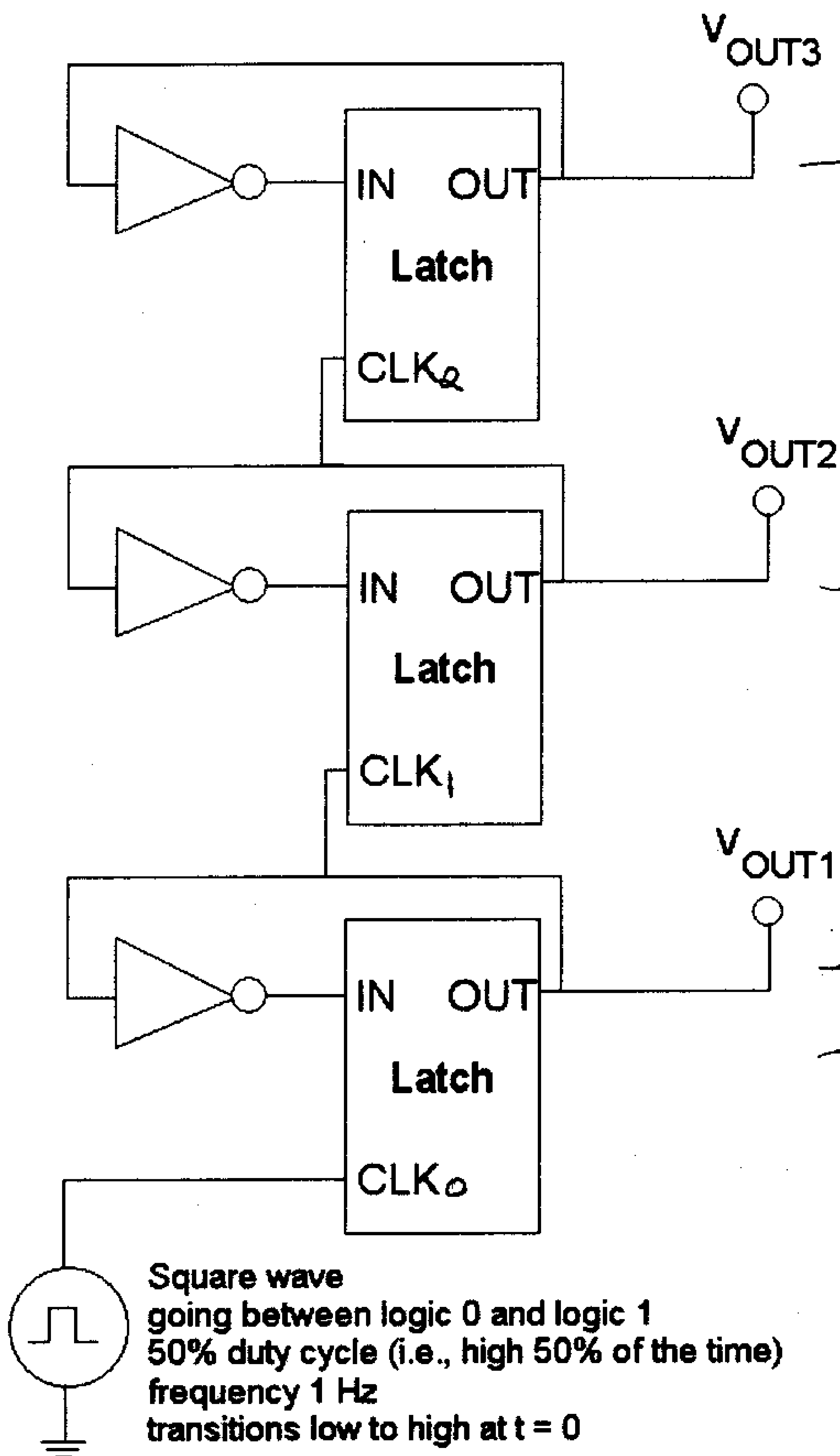
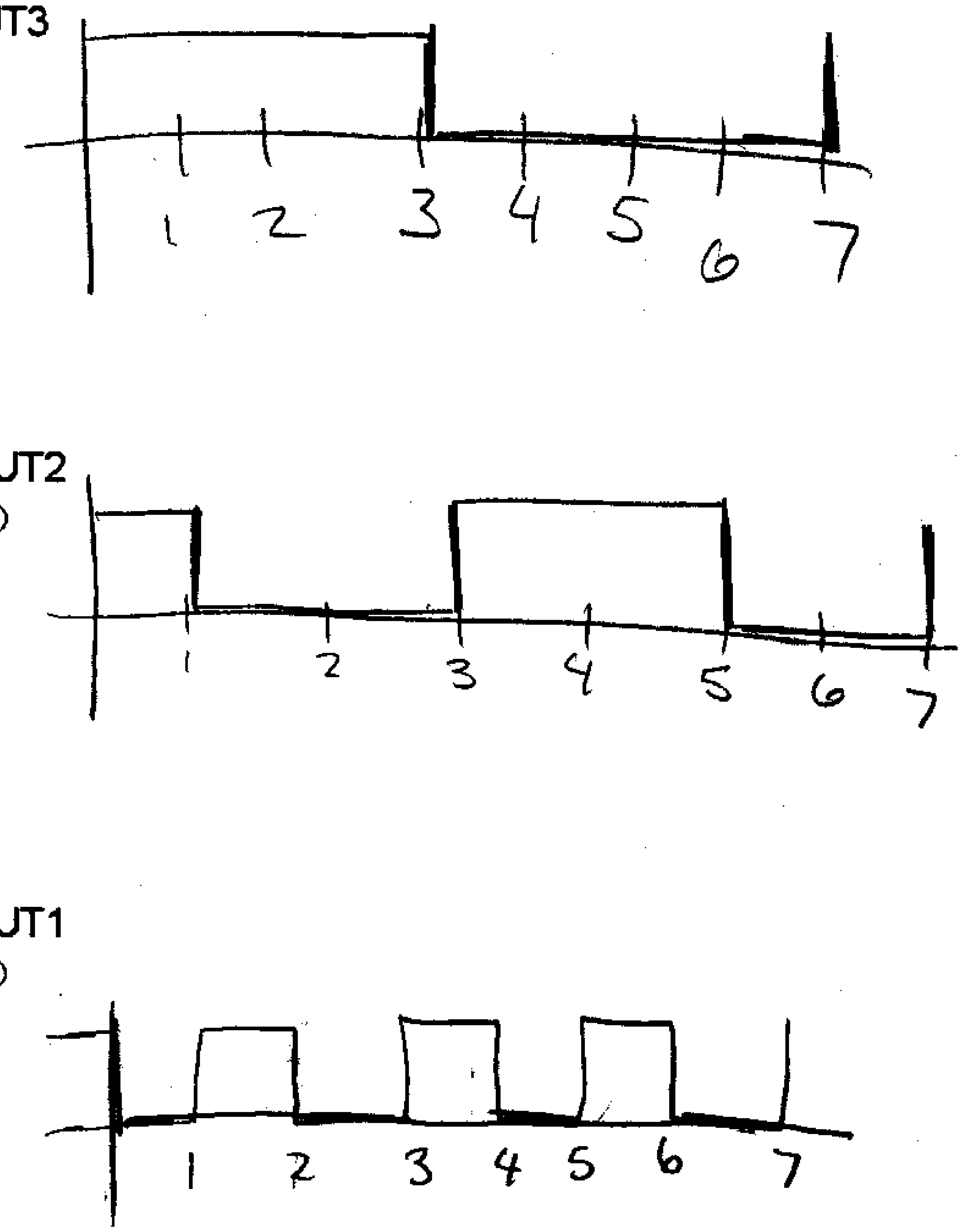
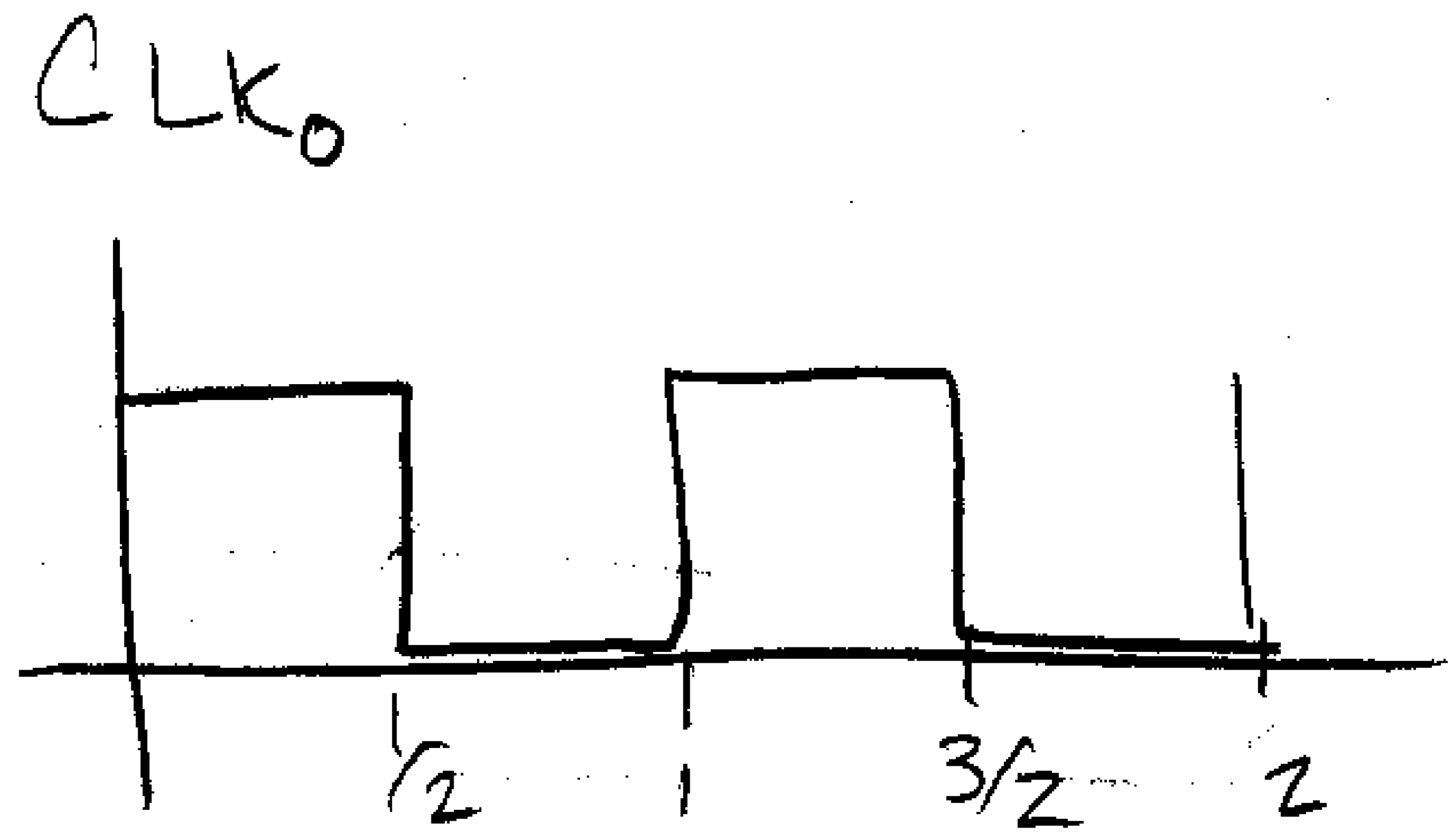
Problem 6 Choice 4

Sketch the logical voltages V_{OUT1}, V_{OUT2}, and V_{OUT3} over a time period of 7 seconds.
Assume that there is no delay in the latch; the output is refreshed the instant the clock signal goes high.
Assume that all of the latches have an initial output of logic 1 just before t = 0.







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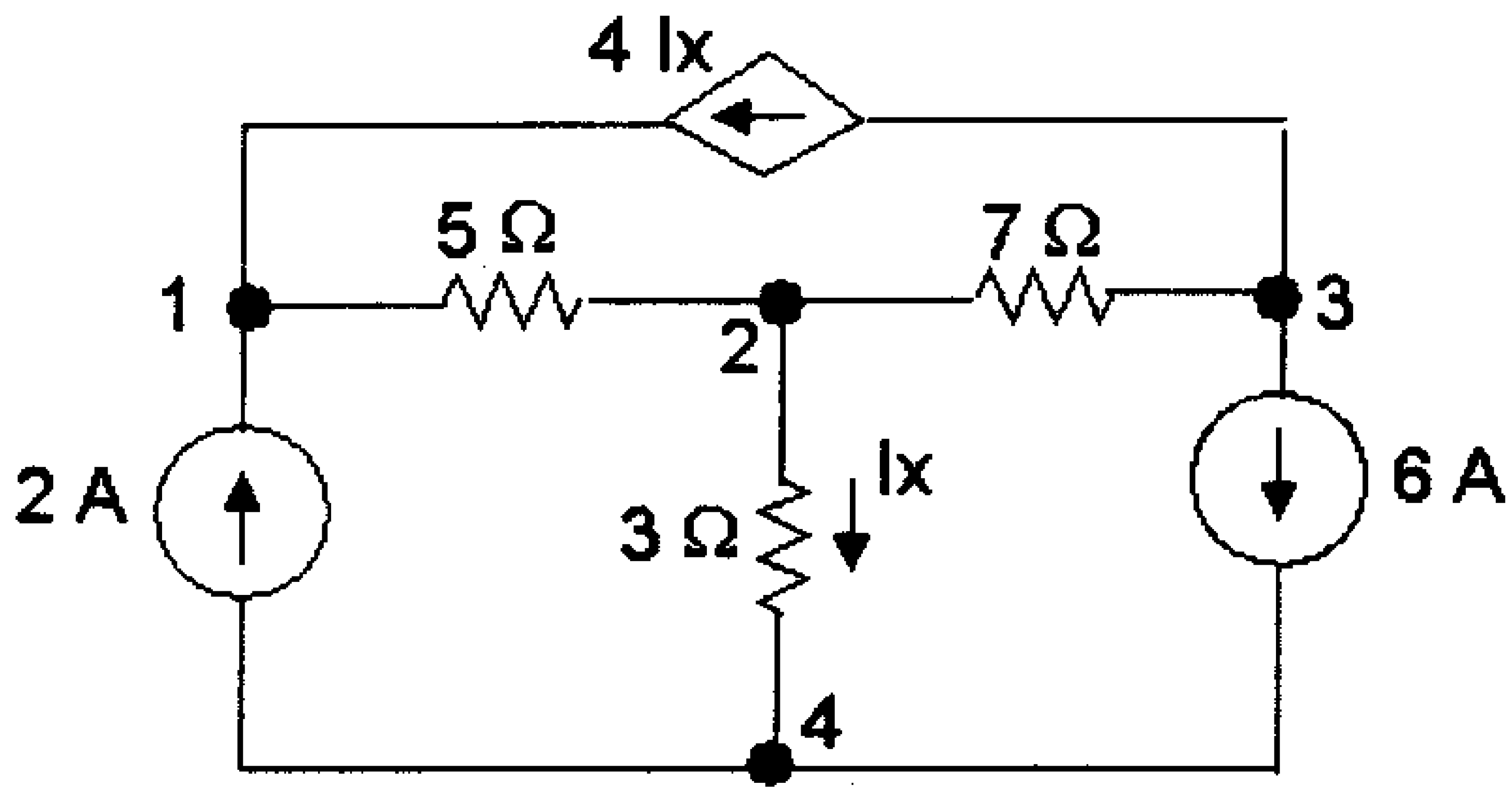
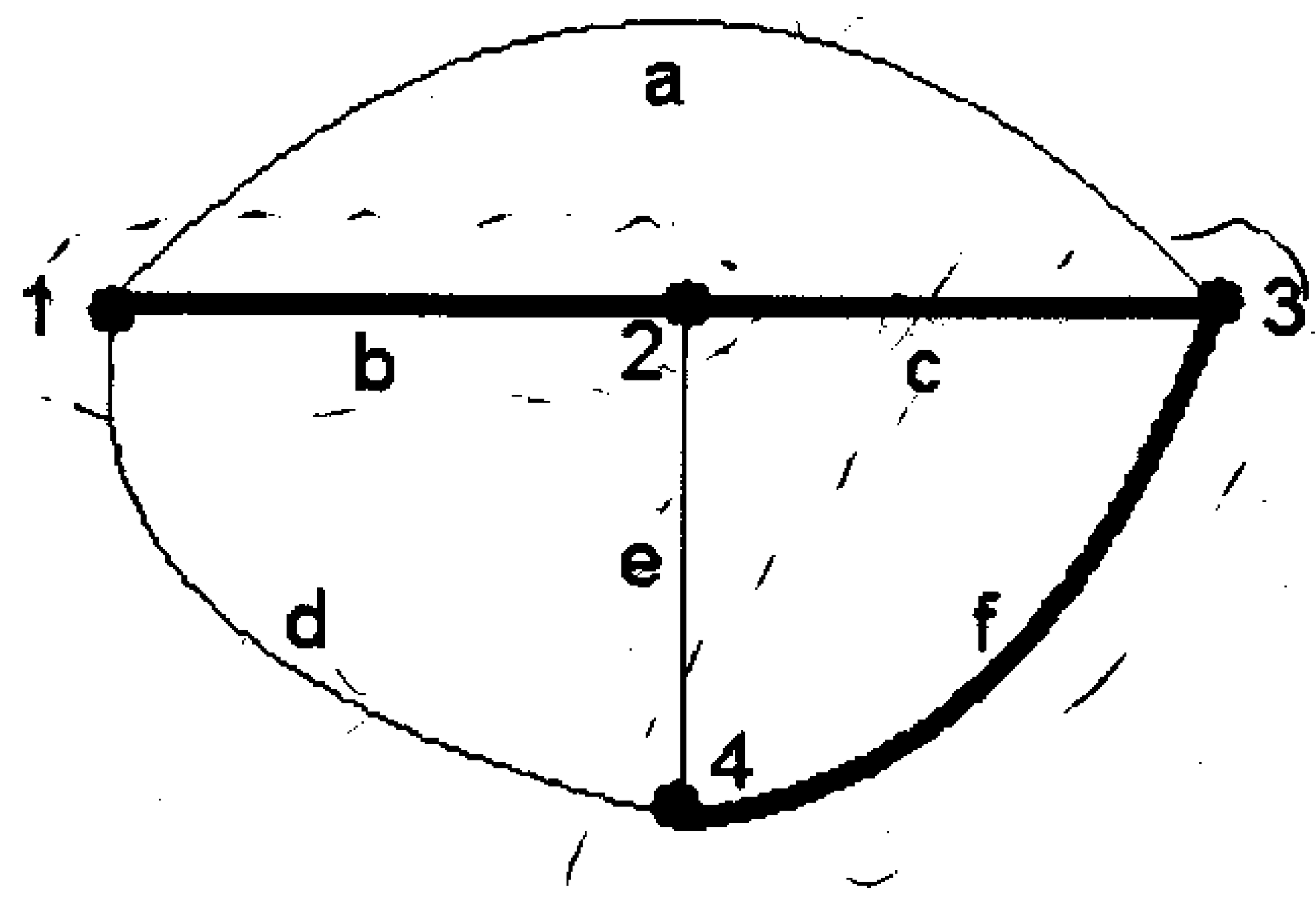
Problem 6 Choice 5:

Given the electric circuit, graph, and tree (bolded edges) below, write the KCL equation associated with each fundamental cut set in terms of node voltages. Do not solve the equations.





Fundamental Cut Sets:

for b: {b, a, d} (separates {1} from {2, 3, 4})

for c: {c, a, d, e} (separates {1, 2} from {3, 4})

for f: {f, e, d} (separates {1, 2, 3} from {4})

Using {b, a, d}:

$$2A + 4\left(\frac{V_2 - V_4}{3\Omega}\right) + \frac{V_2 - V_1}{5\Omega} = 0$$

Using {c, a, d, e}

$$4\left(\frac{V_2 - V_4}{3\Omega}\right) + \cancel{\ } - I_x + \frac{V_3 - V_2}{7\Omega} + 2A$$

$*\left(= \frac{V_2 - V_4}{3}\right)$

Using {f, e, d}:

$$6A + \frac{V_2 - V_4}{3} - 2A = 0$$

You can set any 1 voltage to 0V for reference.