Fall 2009

EE40 Homework #8

Due Oct 30 (Thursday), 12:00 noon in Cory 240

Reading Assignments

Chapter 7 of Hambley

Problem 1: Decimal and Binary Numbers (Hambley 7.20)

Perform these operations by using 8-bit signed two's complement arithmetic:

a) $17_{10} + 15_{10}$

b) $17_{10} - 15_{10}$

c) $33_{10}-37_{10}$

d) $15_{10}-63_{10}$

e) $49_{10}-44_{10}$

Problem 2 : DeMorgan Laws *(Hambley 7.33)*

Replace the AND operations by ORs and vice versa by applying DeMorgan's Laws to each of these expressions: (note: /X denotes the logic inverse of X)

a) F= AB+(/C+A)/D
b) F=A(/B+C)+D
c) F=A/BC+A(B+C)
d) F=(A+B+C)(A+/B+C)+(/A+B+/C)
e) F=ABC+A /B C+/A B /C

Problem 3 Circuit diagram to Logic Truth Table *(Hambley P7.35)*

Consider the circuit shown below. The switches are controlled by logic variables, such that, if A is high switch A is closed and if A is closed, switch A is closed. Conversely, if B is high, the switch label /B is open, and if B is low, the switch label /B is closed. The output variable is high (logic "1") if the output voltage is 5V, and the output variable is low if the output voltage is 0 (logic "0"). Write a logic expression for the output variable.
Construct the truth table for the circuit.

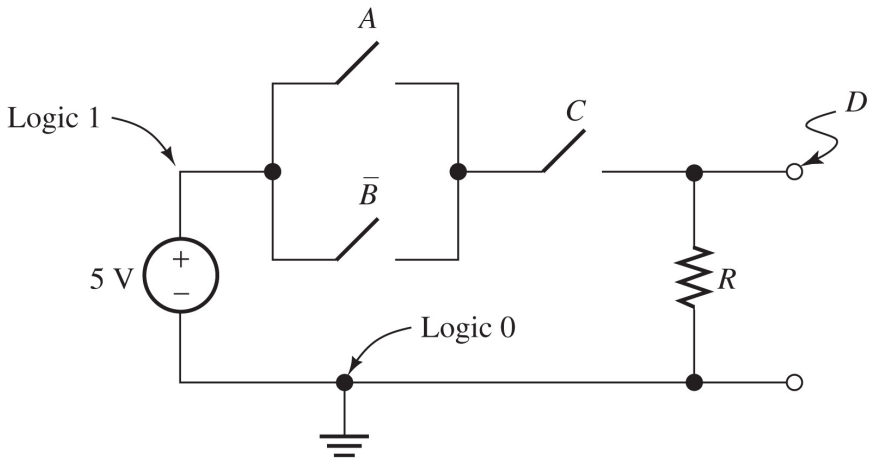

Fig.3 Logic Circuit

Problem 4 Logic Circuit Synthesis *(Hambley P7.52)*

[Hint: This problem is to test your understanding, the solution is relatively simple]

Suppose that two numbers in signed two's complement form have been added, S1 is the sign bit of the first number,S2 is the sign bit of the second number, and ST is the sign bit of the total. Suppose that we want a logic circuit with output E that is high if either overflow or underflow has occurred, otherwise, E is to remain low.

a) write the truth table

b) find an SOP expression composed of minterms for E

c) draw a circuit that implements E using AND , OR and NOT gates

Problem 5 Minimization of Logic Circuits I *(Hambley P7.55)*

A Logic circuit has inputs A,B and C. The output of the circuit is given by:

$$\pi M(1,3,4,6)$$

a) *Construct the Karnaugh Map for D*

b) *Find the minimal SOP Expression*

c) *Find the minimal POS Expression*

Problem 6 Minimization of Logic Circuits II *(Hambley P7.66)*

A City council has three members, A,B and C. Each member votes on a proposition, 1 for yes, 0 for no. Find a minimized SOP logic expression having inputs A,B,C and output X that is high when the majority vote is yes, and low otherwise. Show that the minimized logic circuit checks to see if any pair of the three board members has voted yes. Repeat for a council of five members. (Hint: In this case the circuit checks to see if any group of 3 has voted yes)

Problem 7 Sequential Circuit Execise I *(Hambley P7.83)*

The D-Flip-Flops of Fig. 7 below are positive-edge triggered. Assuming that prior to t=0 the states are $Q_0=Q_1=0$ Sketch the voltage waveforms at Q_0 and Q_1 as a function of time. Assume voltage levels of 0 and 5V

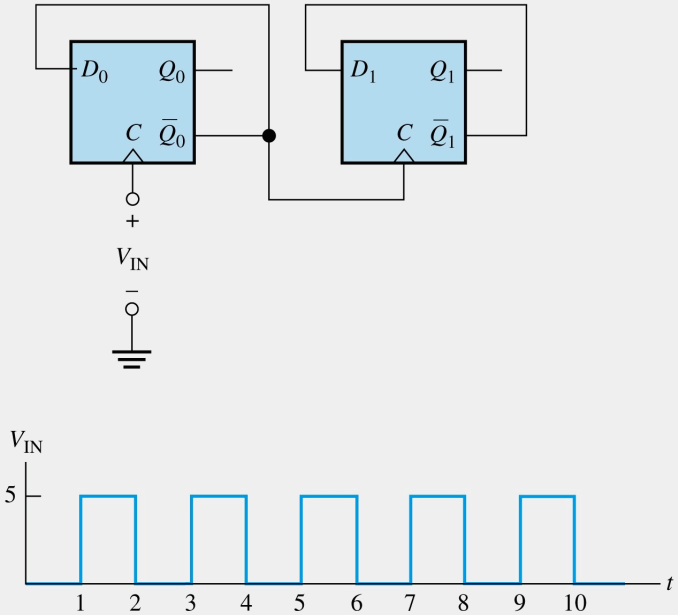

Fig.7: Divide-by 4 circuit

Problem 8 Sequential Circuit Execise II *(Hambley P7.84)*

The D flip-flops of figure 8 below are positive edge-triggered and the Cl input is an asynchronosous clear. Assume that the states are Q_0=Q_1=Q_2=Q_3=0 at t=0, the clock input Vin is shown in figure 7 above. Sketch the voltage waveforms at Q_0,Q_1,Q_2,Q_3 versus time . Assume voltage levels are 0V and 5V

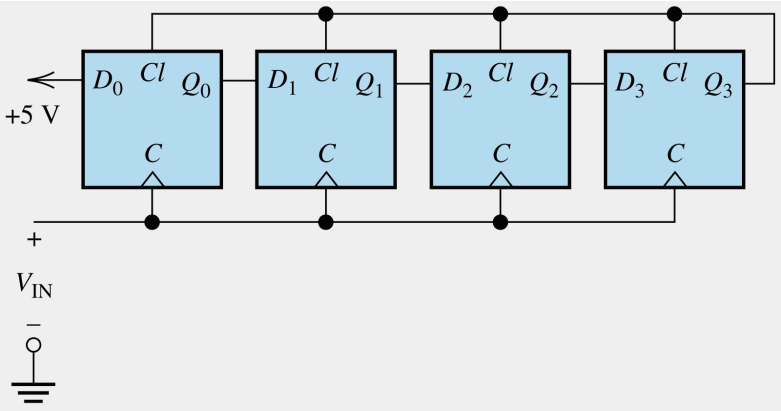

Figure 8.1: Shift-Register Circuit

Problem 9 LED Circuit Design *(Hambley 7.88)*

For Light Emitting Diodes (LEDs) are arranged at the corners of a diamond, as illustrated in figure 9 below. When logic 1 is applied to an LED, it lights. Onlt 1 diode is to be on at a time. The on state should move from diode to diode either clockwise or counter-clock wise, depending on wether S is high or low, respectively. One complete revolution should be completed in each 2-second interval.

a) What is the frequency of the clock?

b) Draw a suitable logic circuit for the counter
c) Construct the truth table and use Karnaugh Maps to determine the minimum SOP expression for D_1-D_4 In terms of S, Q_1 and Q_2

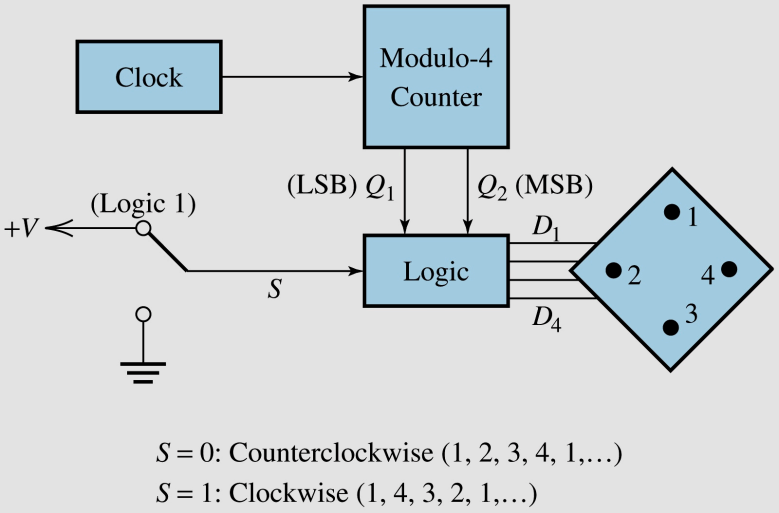

Fig 9: LED Circuit