UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

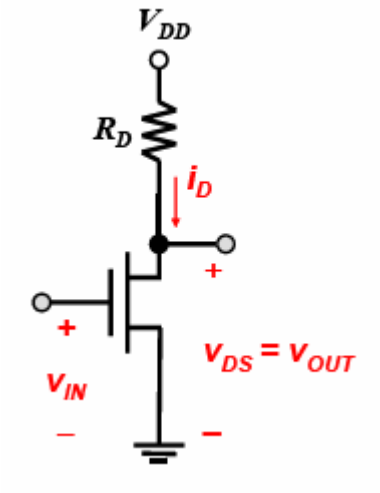
EECS 40

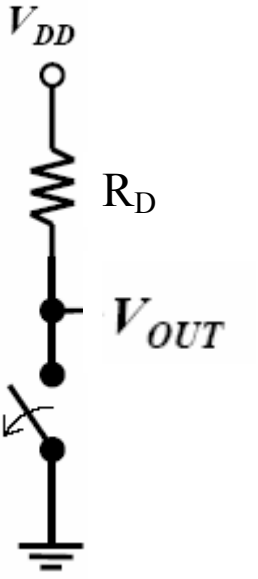
Fall 2003

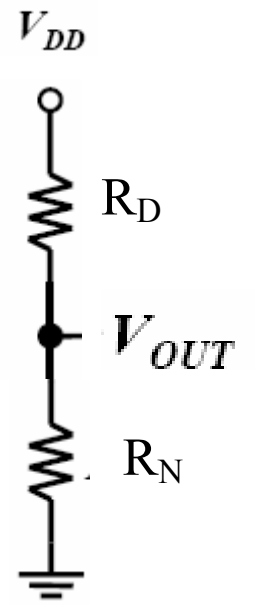
Homework #9 Solutions

Problem 1: Inverter Circuits and Noise Margins

a) Describe qualitatively how an NMOS inverter circuit (below left) works. Explain how relatively large noise margins ***NMH*** and ***NML*** can be achieved. (Refer to Slide 6 of Lecture 26 for the definitions of ***NMH*** and ***NML***).

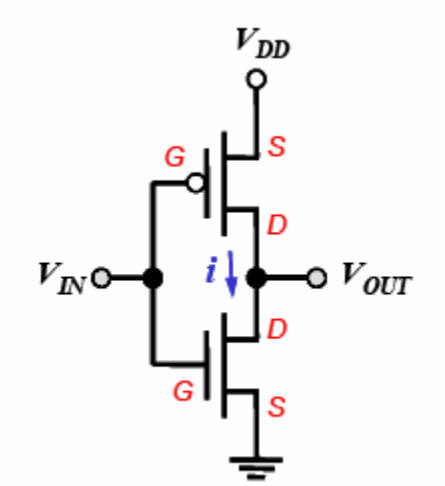


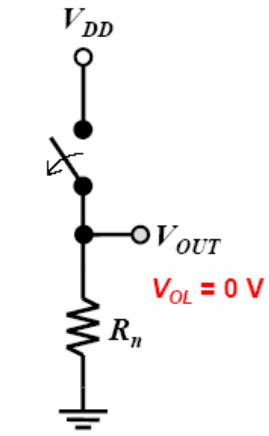
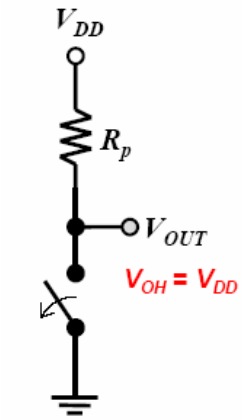
When the input is low the NMOS is cut-off. The resulting circuit is as seen on the right. Therefore, for low input voltages the output voltage is Vdd.	 $V_{IN} = 0$ V

For Vin high the NMOS is on, and behaves as a resistor. Therefore, Vout = Vdd*Rn/(Rn+Rd). With a sufficiently large Rd, one can make Vout satisfactorily small. Recall, Rn= $\frac{3}{4}\frac{V_{DD}}{I_{DSATn}}\left(1-\frac{5}{6}\lambda_n V_{DD}\right)$	 $V_{IN} = V_{DD}$

Lowering V_{OL} will increase the noise margin. This allows for a greater swing (V_{OH}=Vdd, V_{OL}=0) which in turn increases the noise margins. For an NMOS inverter, one can do this by increasing Rd, increasing W, or replacing Rd with a PMOS.

b) Describe qualitatively how a CMOS inverter (below right) works. What are its advantages (with respect to noise margins, power consumption, and size) as compared with the NMOS inverter?

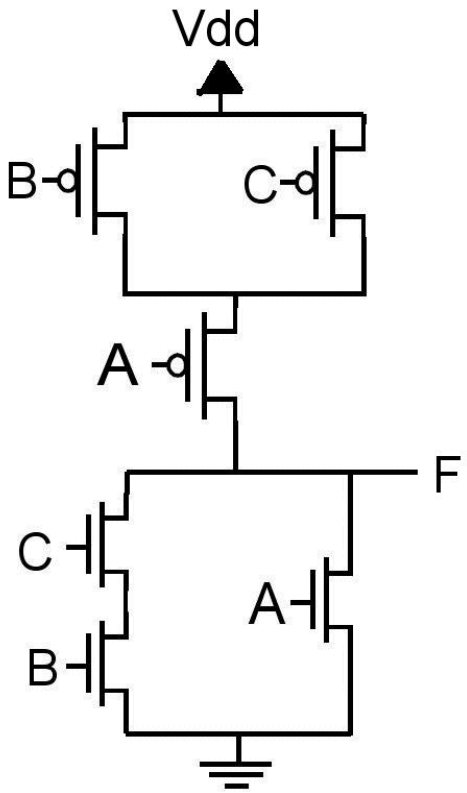


When the input is high, the PMOS is off (a open circuit) and the NMOS is on (treated as a resistor). Vout sees a direct path to ground. Therefore when the input is high the output is low.	 $V_{IN} = V_{DD}$
When the input is high, the NMOS is off (a open circuit) and the PMOS is on (treated as a resistor). Vout now sees a direct path to Vdd. Therefore when the input is low the output is high.	 $V_{IN} = 0$ V

The CMOS inverter has a larger output voltage swing than the NMOS inverter, which cannot pull the output voltage all the way to zero. This results in better noise margins. Also, the CMOS inverter takes up less space and uses less energy than the NMOS inverter. Resistors take up much more space on the IC than a PMOS, especially for large resistors. Also, with the CMOS inverter at least one of the two MOSFETs is in the cutoff region during steady-state; however, the NMOS inverter is in the triode mode when the input is high. Therefore the CMOS inverter uses practically no power while in steady-state, while the NMOS does.

Problem 2: CMOS Logic Gates
Design a complex CMOS logic gate to implement the function $\mathbf{F} = \overline{(\mathbf{A} + \mathbf{B}\cdot\mathbf{C})}$

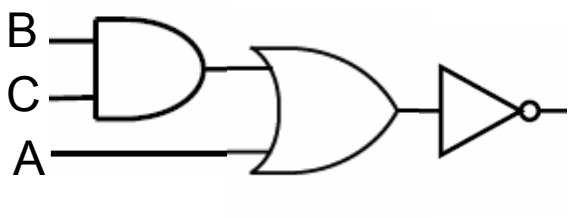
Using DeMorgan's rule (to find pull up network): $F=\bar{A}\cdot\overline{(B \cdot C)} = \bar{A} \cdot (\bar{B} + \bar{C})$



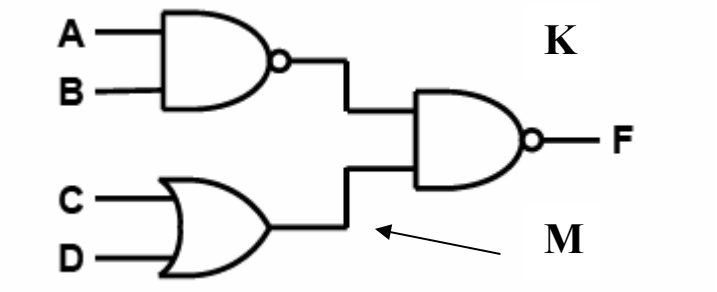
Problem 3: Combinational Logic Circuits

a) Write the truth table for the following Boolean expression: $\mathbf{F} = \overline{(\mathbf{A} + \mathbf{B}\bullet\mathbf{C})}$. Draw a logic circuit to realize this expression using AND, OR, and NOT gates.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



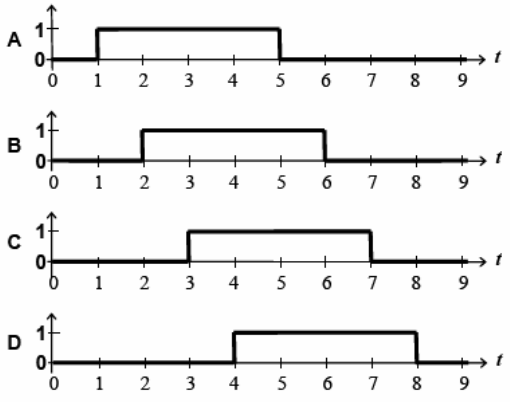
b) Consider the following logic circuit:

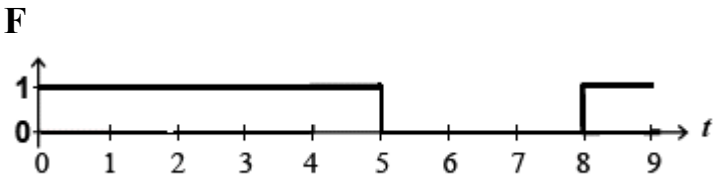


i) Write the Boolean expression for **F**.

$$F=\overline{(A\bullet B)\bullet(C+D)}=\overline{(A\bullet B)}+\overline{(C+D)}=A\bullet B+\overline{C}\bullet\overline{D}$$

ii) Suppose the values of the four input variables **A B C D** as a function of time are as shown in
the timing diagram below. Draw **F** as a function of time.





Problem 4: Logic Circuit Synthesis
Consider the adder circuit whose truth table is given in Slide 8 of Lecture 29.
a) Write a "sum-of-products" expression for the sum bit **S0**.

Input			Output	
A	B	C	S_1	S_0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$S0=\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

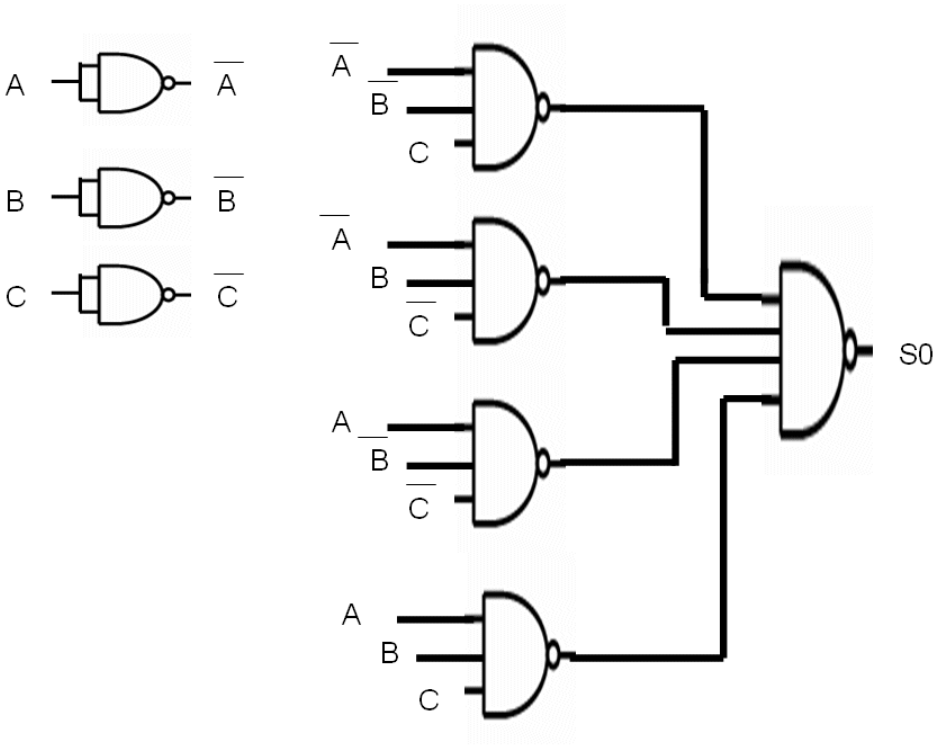
b) Simplify this logical expression.

S0	BC				
		00	01	11	10
A	0	0	1	0	1
	1	1	0	1	0

S0 cannot be simplified anymore using NAND and NORs, but it can be simplified using exclusive-or.

S0=(A <XOR> B <XOR> C)

c) Draw the logic circuit for **S0** using only NAND gates.


A
$\overline{A}$
B
$\overline{B}$
C
$\overline{C}$
$\overline{A}$
B
C
$\overline{A}$
B
$\overline{C}$
A
B
$\overline{C}$
A
B
C
S0