UNIVERSITY OF CALIFORNIA AT BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

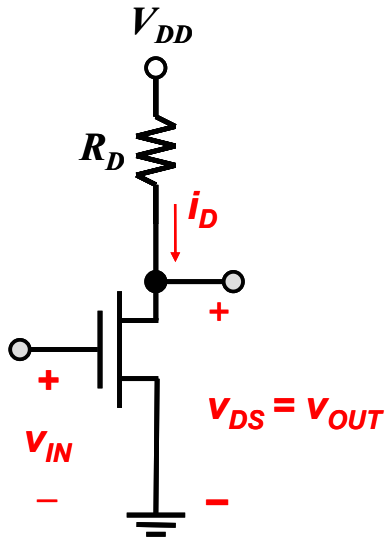
EECS 40 **Fall 2003**

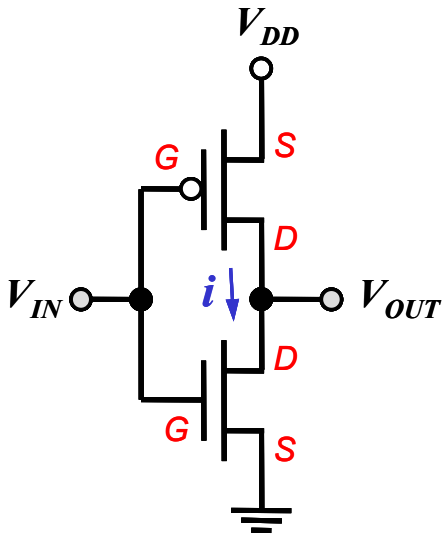
Homework Assignment #9
Due at 11:00 AM in 240 Cory on Friday, 11/14/03
* Be sure to put your **Discussion Section number** on your paper; **otherwise 5 pts will deducted from your score!**

Problem 1: Inverter Circuits and Noise Margins

a) Describe qualitatively how an NMOS inverter circuit (below left) works. Explain how relatively large noise margins NM_H and NM_L can be achieved. (Refer to Slide 6 of Lecture 26 for the definitions of NM_H and NM_L).

b) Describe qualitatively how a CMOS inverter (below right) works. What are its advantages (with respect to noise margins, power consumption, and size) as compared with the NMOS inverter?





Problem 2: CMOS Logic Gates

(Read: pp. 199-202 of Section 6.2.1, Rabaey *et al.*)

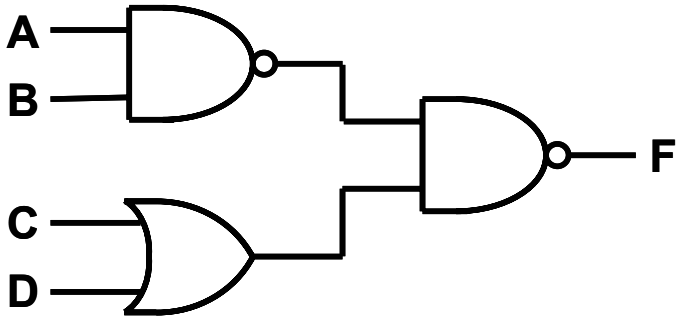
A static CMOS logic gate is a combination of two networks: a *pull-up network* of PMOS transistors, and a *pull-down network* of NMOS transistors. The pull-up network provides a connection between the output and the power-supply V_{DD} anytime the output of the logic gate is meant to be **1** (based on the inputs). The pull-down network provides a connection between the output and *GND* anytime the output of the logic gate is meant to be **0** (based on the inputs). Remember that NMOS devices are turned on with a high (logic **1**) input voltage, whereas PMOS devices are turned on with a low (logic **0**) input voltage, and that transistors connected in series correspond to an AND function, whereas transistors connected in parallel correspond to an OR function. (Refer to Slides 5 & 6 of Lecture 27.)

Design a complex CMOS logic gate to implement the function $\mathbf{F} = \overline{(\mathbf{A} + \mathbf{B} \cdot \mathbf{C})}$

Problem 3: Combinational Logic Circuits

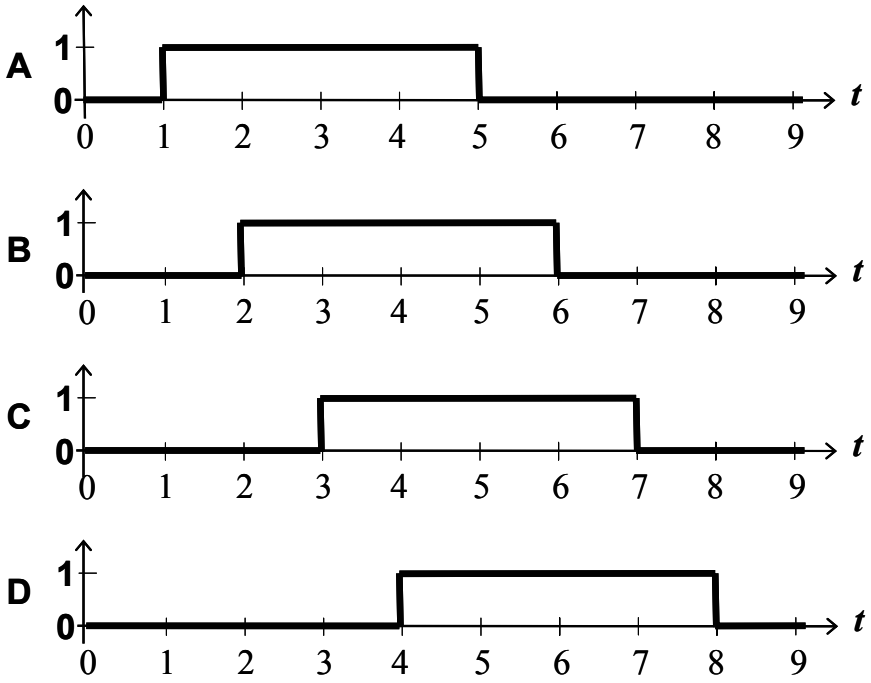
a) Write the truth table for the following Boolean expression: $\mathbf{F} = \overline{(\mathbf{A} + \mathbf{B} \cdot \mathbf{C})}$. Draw a logic circuit to realize this expression using AND, OR, and NOT gates.

b) Consider the following logic circuit:



i) Write the Boolean expression for **F**.

ii) Suppose the values of the four input variables **A B C D** as a function of time are as shown in the timing diagram below. Draw **F** as a function of time.



Problem 4: Logic Circuit Synthesis

Consider the adder circuit whose truth table is given in Slide 8 of Lecture 29.

a) Write a "sum-of-products" expression for the sum bit $\mathbf{S_0}$.

b) Simplify this logical expression (using either the method used to simplify the expression for $\mathbf{S_1}$ in class on 11/7, or a Karnaugh map).

c) Draw the logic circuit for $\mathbf{S_0}$ using only NAND gates.