UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Fall 2003**

Homework #8 Solutions

Problem 1

a) S = n(kT/q)(ln 10); assume room temperature. We know that (kT/q)(ln 10) = 60mV at room temperature. Then S = 1.15(60) mv/decade = 69 mV/decade

b) Part a) tells us that for each decade rise in drain current, we need to increase V_{GS} by 69mV. The normalized drain current at the threshold voltage is given to be 100nA and for a device where W=L, I_D at V_T is given to be 100nA/1 = 100nA. We cannot have more than 100pA of current when V_{GS} is exactly 0. Then from V_{GS} = 0V to V_{GS}=V_T, we can have a minimum 100nA/100pA = 1000 = 3 decades rise in drain current. This implies that the minimum V_T we can have for the device is V_{Tmin} = 3 x 69mV = 207mV which limits the drain current to a maximum of 100pA at V_{GS} = 0.

c) For a leakage current requirement of 0.1pA when V_{GS} = 0V, we need to increase the threshold voltage to a much higher value than the one calculated in part b) since 100nA/0.1pA = 1 x 10^6 = 6 decades; this gives V_{Tmin} = 414mV. The saturation current is given by the following equation:

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

In this case, increasing to a larger threshold voltage reduces the saturation current, I_{DSAT} as compared to part b).

Problem 2

a) In the on-state, the transistor is saturated because the gate-to-source voltage is very high (e.g. V_{DD}). Using the following equation for current when the transistor is saturated, we can obtain the saturation current as shown below.

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

I_{DSAT} = 50 μA/V^2 x ½ x 100μm/10μm x $(5 - 0.7)^2$ = 4.62mA
Then R_{eq} = ¾ x 5V/4.62mA x (1 – 5/6(0)5V) = 811.2 Ω

b) Approaches to lowering R_{eq} are:
   1. Reducing the threshold voltage will increase I_{DSAT} which will reduce R_{eq}.
   2. Increasing the width of the transistor will reduce R_{eq} as the resistance is inversely proportional to width. This increases the saturation current for the transistor.
   3. We can also reduce the length of the transistor to reduce the resistance since resistance is directly proportional to length, so a smaller length transistor will have a higher saturation current.

c) For a very short-channel MOSFET, the saturation current and saturation voltage are given by the following two equations:

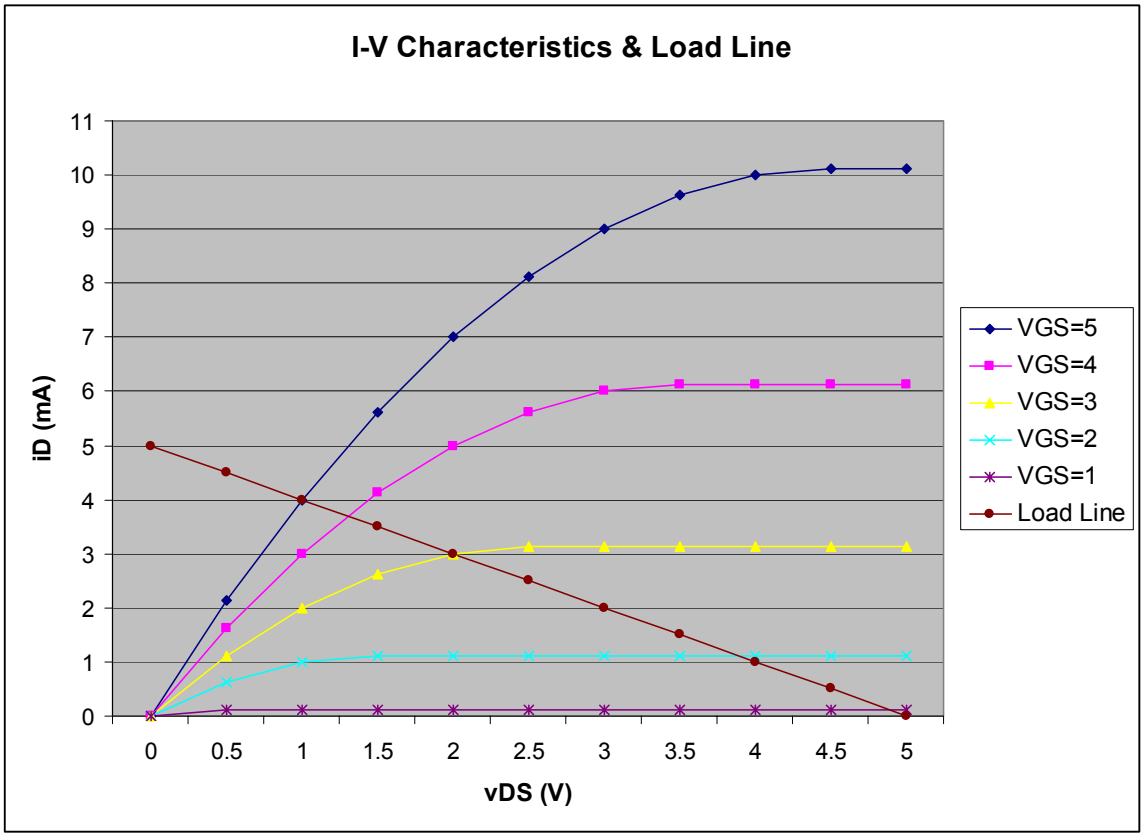
$$I_{DSAT} = WC_{ox}\left[V_{GS} - V_T - \frac{V_{DSAT}}{2}\right]v_{sat}$$

$$V_{DSAT} = \frac{L}{\mu_n}v_{sat}$$

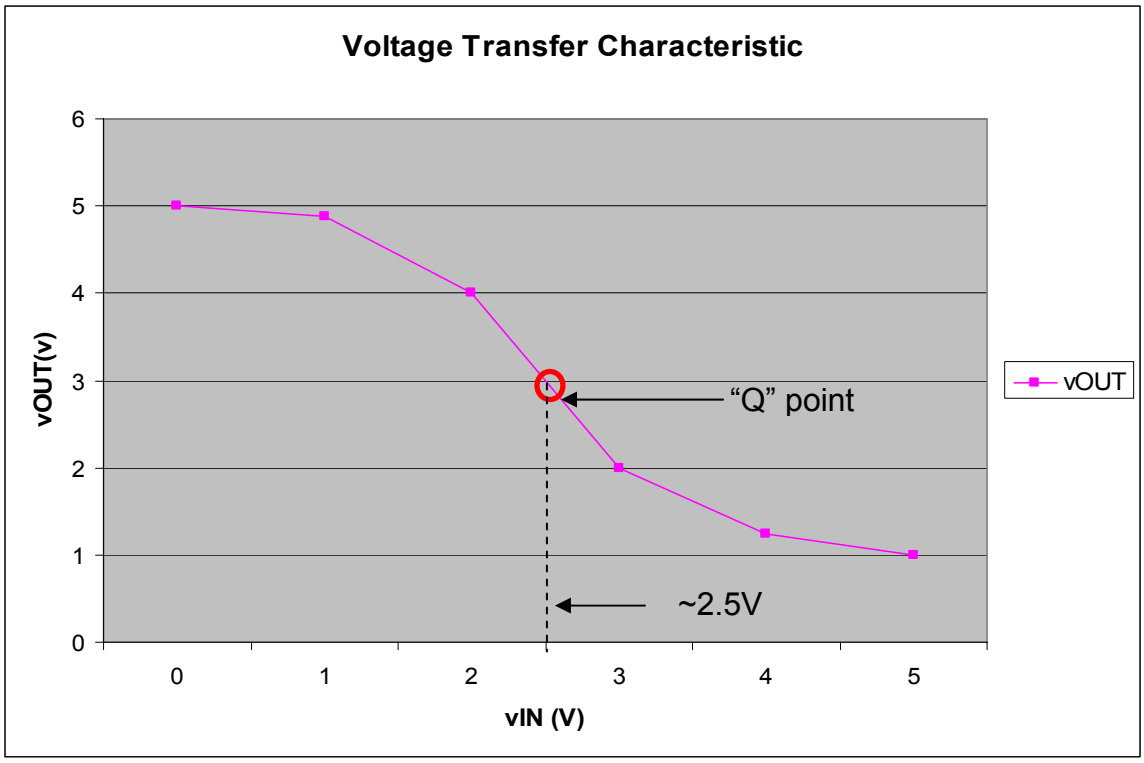
V_{DSAT} = 0.1 x 10^{-4} cm/300cm^2/Vs x 10^7cm/s = 0.33 V and
I_{DSAT} = 1 x 10^{-4} cm x 2 uF/cm^2[1 – 0.4 – 0.33/2][V]10^7 cm/s = 0.87 mA.
R_{eq} = ¾(1V/0.87mA)(1 – 5/6(0.1)) = 790 Ω

Problem 3

a)

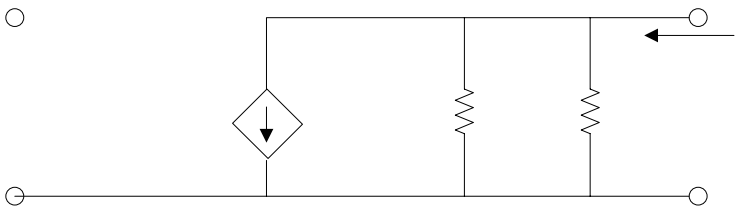


b)



c) From the voltage characteristic, the optimal operating point, or "Q" point occurs where the gain of the circuit is the highest or when the slope of the VTC is the steepest. We find that the "Q" point is approximately 2.5V as determined in the above graphical analysis. Thus, $V_{BIAS} \approx 2.5V$.

The open-circuit voltage gain is given as $A_v = v_{out}/v_{in}$. We must use the small signal model for the NMOS and draw the small-signal equivalent circuit as shown below.



Then $v_{out} = -(g_m)(v_s)(r_o||R_D)$ and $v_{in} = v_s$. Thus $A_v = -(g_m)(r_o||R_D)$. We can calculate g_m and r_o to be the following: (note $V_{GS} = V_{BIAS}$ for largest gain)
$g_m = (W/L)(k')(V_{GS} - V_T) = 1000uA/V^2 \times (2.5 - 0.5) = 0.002$ siemens
$r_o = 1/g_o = 1/\lambda I_D = \infty$. Then $A_v = (-0.002 \text{ siemens})(1k\Omega) = -2$.