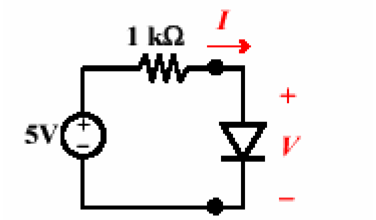
UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Fall 2003**

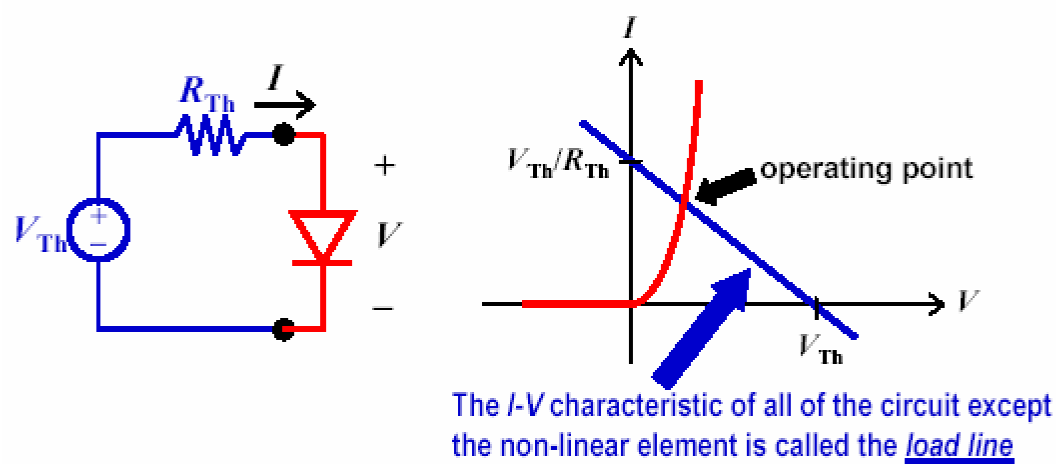
Homework #7 Solutions

Problem 1

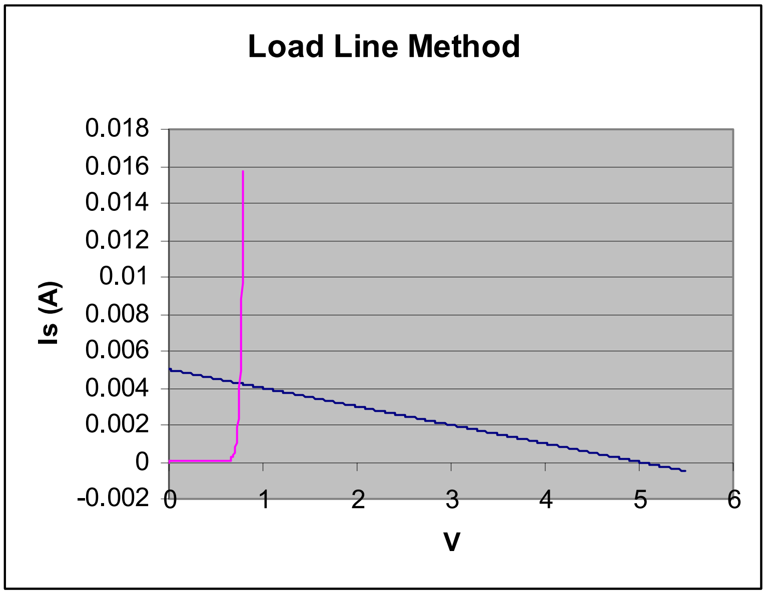


a)

Remember this from class:



Here, Vth=5V & Rth=1k
Vth/Rth=5mA
I_D= Is *(exp{ q*V_D / kT } – 1)
= (10^-15) (exp{ V_D / .026 } – 1)



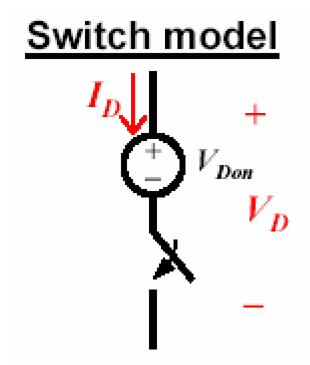
The solution is where the lines cross. Therefore,
I=4.5mA
V=.75V

b)

Replace the Diode with the large signal model.
Assume diode is ON.
Do KVL: -5V +I*1k+.7=0

I=4.3mA
V=.7V

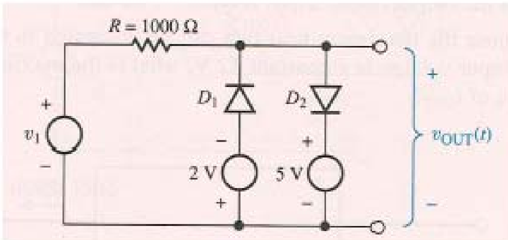
This solution, using the large signal approximation, is relatively close to the solution in part a. Therefore the model worked well.



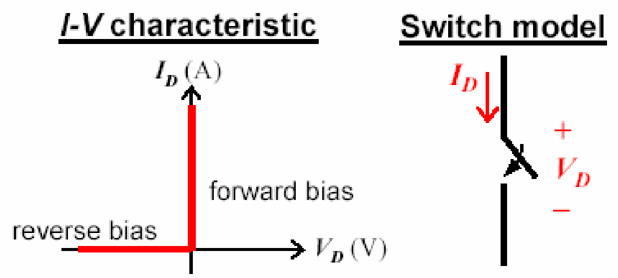
c)

I will decrease and ***V*** will increase when the silicon diode is replaced by an AlGaAs LED. From Slide 11 of Lecture 20, we know that the AlGaAs LED emits photons of wavelength 650 nm. The energy of these photons is larger than that of photons which would be emitted by a Si diode (wavelength ~1000nm). Therefore, the energy needed to generate an electron-hole pair in AlGaAs is larger than that need to generate an electron-hole pair in Si. Hence, for a given temperature (*e.g.* 300K), n_i^2 will be much smaller for AlGaAs than for Si. This means that the diode saturation current I_S will be much smaller for the AlGaAs LED than for the Si diode, so that a larger diode voltage ***V*** will be required to achieve a comparable diode current.

Problem 2



D1 and D2 are perfect rectifiers. Therefore their I-V characteristics are as follows:



(Note: remember that "on" refers to a short circuit and "off" refers to an open circuit, and according to the perfect rectifier model current can only flow forward through a diode.)

From the circuit diagram, you can see that v1 must be greater than 5V for D2 to be on, and v1 must be less than 2V for D1 to be on. Therefore they are both off when the input voltage is between -2 and 5 volts.

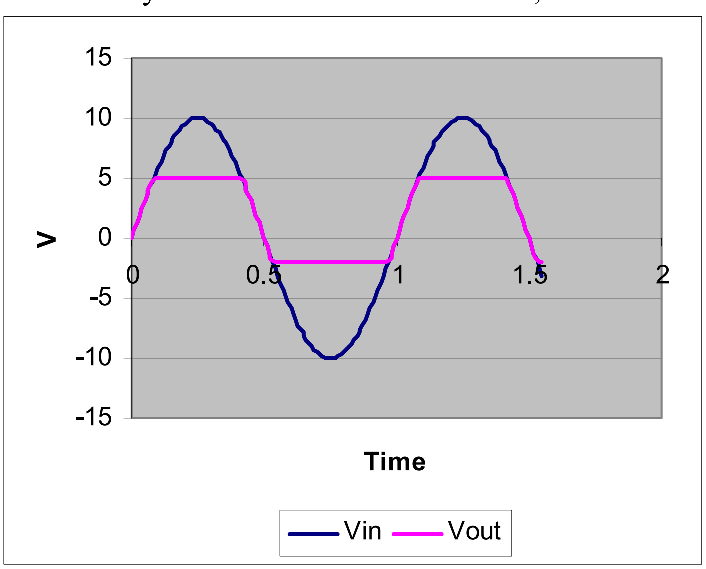
When D2 is on:

Vout=5V

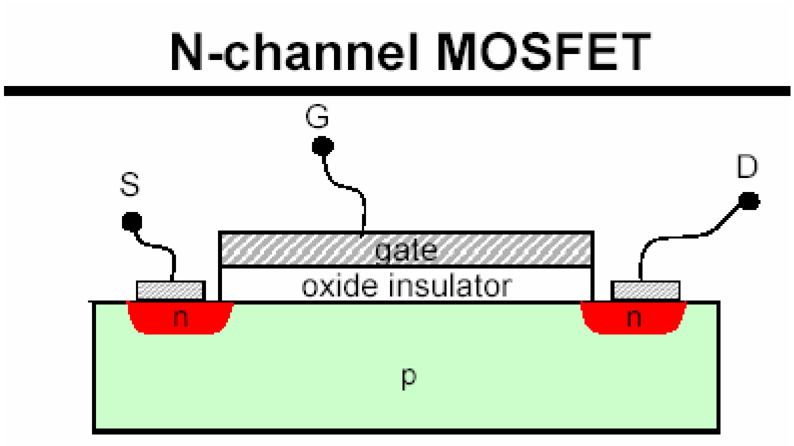
When D1 is on:

Vout=-2V

When they are both off no current flows, therefore Vout=Vin



Problem 3



a) When a positive voltage (relative to the source potential and body potential) is applied to the gate electrode, the positive charge on the gate will repel mobile holes away from the surface of the semiconductor channel, depleting this region. Thus, negative charge (consisting of immobile acceptor ions) is induced in the channel. As the magnitude of the gate voltage is increased above the threshold voltage, conduction electrons (either supplied from the source region, or by thermal generation in the channel region) will be attracted to the surface of the channel. (Increases in gate voltage – or positive charge on the gate – induce increases in mobile negative charge in the semiconductor, when the gate voltage exceeds the source voltage by more than the threshold voltage.) The surface of the semiconductor channel thus becomes n-type (higher concentration of conduction electrons than holes), and a conductive path (n-type semiconductor) is formed between the n-type source and drain regions. The resistance of this "inversion layer" decreases, since the concentration of conduction electrons increases, with increasing gate voltage.

b) The resistance between the source and drain (defined as V_{DS}/I_D) will be independent of the drain voltage, for very small values of drain voltage. As the drain voltage increases, the inversion-layer charge density at the drain end of the channel will decrease significantly (because of the resultant decrease in the potential difference between the gate and the channel), and so the resistance between the source and drain will increase. (Recall that the "sheet resistance" of the channel is inversely proportional to the inversion-layer charge density; see Slides 5-6 from Lecture 22.) When the drain voltage increases above V_G-V_T, the inversion-layer charge density at the drain end of the channel is zero, *i.e.* the channel is "pinched off". Further increases in drain voltage will not result in increases in voltage applied across the inversion-layer conductive path (refer to Slide 8 of Lecture 22), so the drain current saturates. The resistance between the source and drain will therefore continue to increase with increasing V_D.

c) If the channel length is very short, so that velocity saturation occurs at a drain voltage lower than that required to pinch off the inversion layer at the drain, then the drain current will saturate sooner (as the drain voltage is increased), and the resistance between the source and drain will begin to increase at a lower value of drain voltage. Since the resistance between the source and drain is proportional to the channel length, the resistance for the very-short-channel MOSFET may still be lower than that of a long-channel MOSFET.

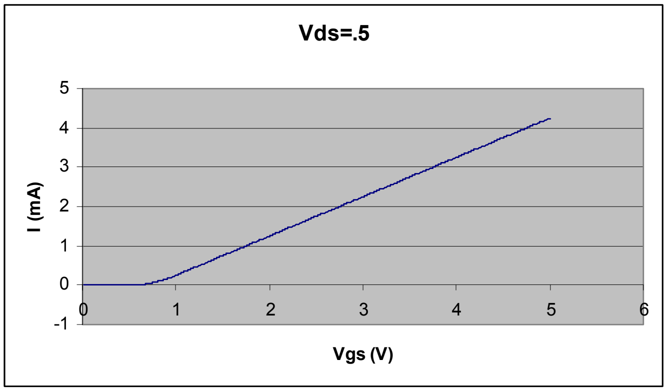
a) Problem 4

$Vt = 0.5$ V; kn'= 0.2 mA/V^2; $L = 1$ um; $W = 10$ um

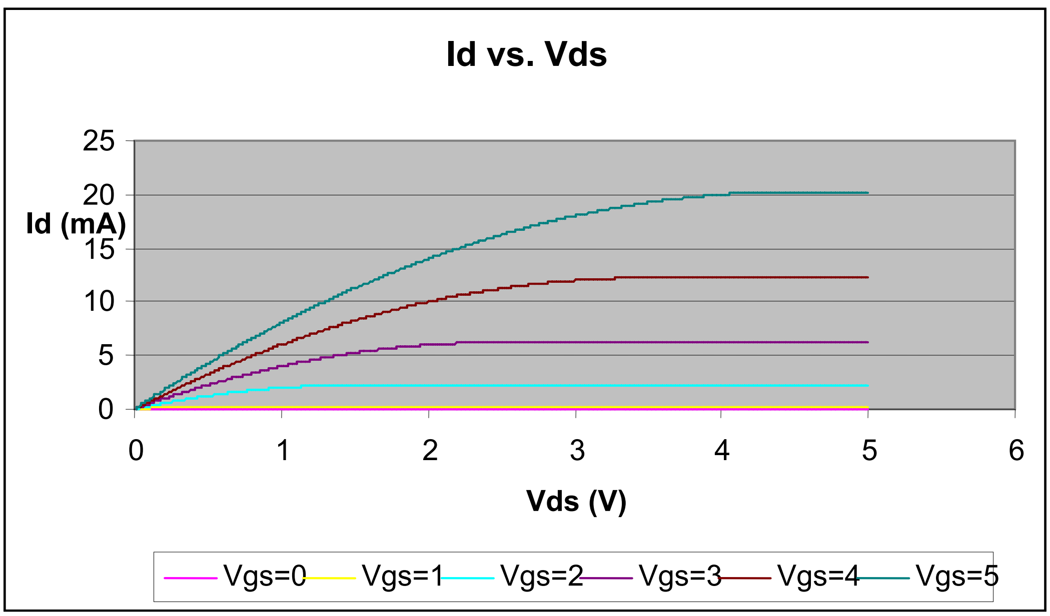
a) Vds=.5V

Vds<Vgs-Vt   Id=kn'(W/L)*[(Vgs-Vt)Vds - 1/2 Vds*Vds]

Vds>Vgs-Vt   Id = 0.5 kn' (W/L) $(Vgs - Vt)^2$



b)



i) $V_{GS} = 1$ V and $V_{DS} = 5$ V

Vgs>Vt

Vds>Vgs-Vt

Saturation Region

ii) $V_{GS} = 1$ V and $V_{DS} = 0.5$ V

Vgs>Vt

Vgs-Vt=Vds

Edge of Saturation Region (or border between Linear Region and Saturation Region)

iii) $V_{GS} = 0$ V and $V_{DS} = 5$ V

Vgs<Vt

Cut Off Region