UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Fall 2003**

Homework Assignment #6 Solutions

Problem 1

a) Mobile electrons and holes can come into existence in a pure (undoped) semiconductor through the following two methods:
   1. By heat (temperature); this is known as thermal generation.
   2. By application of light (irradiation); this is known as optical generation.

   In each case, an electron escapes from a covalent bond (because it gains thermal energy or optical energy) and as a result can move about freely in the semiconductor; it thus becomes a mobile negatively charged particle. The half-filled covalent bond ("hole") which is left behind when the electron escapes can also move about freely in the semiconductor (because an electron from a neighboring covalent bond can move in to fill the half-filled covalent bond, thus resulting in the half-filled covalent bond moving to that neighboring atom); it is associated with a positive charge (because the atom from which the electron escaped has a net positive charge) and can be considered a mobile positively charged particle. Note that for each method of generation, conduction electrons and holes are created in pairs. (This is in contrast to doping, by which either mobile conduction electrons or holes are created in conjunction with immobile positive donor ions or negative acceptor ions, respectively.)

   Assuming that hole and electron mobilities are not a strong function of temperature, the resistivity will decrease with increasing temperature as more mobile conduction electrons and holes are created that can conduct current: The density of conduction electrons (n) and the density of holes (p) increases exponentially with increasing temperature, so the resistivity of an intrinsic semiconductor should decrease exponentially with increasing temperature.

   The resistivity (ρ) is dependent not only on the mobile charge-carrier concentrations, but also the carrier mobilities:

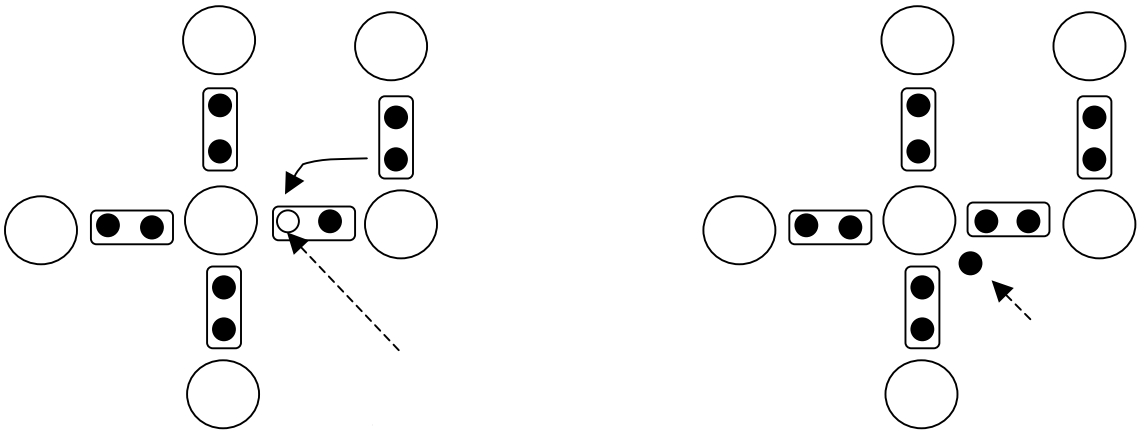
$$\rho = \frac{1}{q\mu_n n + q\mu_p p}$$

   In reality, the mobility of conduction electrons and holes decreases noticeably with increasing temperature T, roughly proportionately with $T^{-3/2}$. (This is due to thermal energy that causes lattice atoms to oscillate about their equilibrium positions, thus increasing the probability for collisions with mobile carriers. The more frequently collisions occur, the lower the carrier mobility.) The temperature dependence of mobility is not as strong as that of the carrier concentration, however, so the resistivity of an intrinsic semiconductor sample actually does decrease with increasing temperature.

b) A Column-III atom has one less valence electron than a Si atom. When it resides on a lattice site in a silicon crystal, all three of its outer-shell valence electrons participate in covalent bonds with neighboring Si atoms. This leaves room for one electron (from a neighboring covalent bond) to be "accepted" into its outer-shell (to complete covalent bonding with all four neighboring Si atoms). The Column-III atom is thus easily ionized (having a net negative charge), resulting in a half-filled covalent bond (which originally contributed the electron to fill the outer shell of the Column-III atom) with an associated positive charge ($+q$), that can easily move from one lattice site to another. Each Column-III atom therefore contributes one mobile positive charge (a hole) and one negative immobile charge (ionized Column-III "acceptor" atom) to the Si lattice.

A Column-V atom has one more valence electron than a Si atom. When it resides on a lattice site in a silicon crystal, only four of its outer-shell valence electrons participate in covalent bonds with neighboring Si atoms. The fifth valence electron easily escapes (so that the Column-V element becomes positively ionized) and can move freely about in the lattice. Each Column-V atom therefore contributes one mobile negative charge (a conduction electron) and one positive immobile charge (ionized Column-V "donor" atom) to the Si lattice.

The pictures below illustrate these points.



c) Ga is a Column-III element and Si is a column-IV element, so Si has one more valence electron than Ga. When a Si atom resides on a Ga site in a GaAs crystal, only three of its valence electrons will participate in covalent bonding with neighboring As atoms. Its fourth valence electron can easily escape (*i.e.* the Si atom is easily ionized with positive charge), to move about freely in the GaAs lattice. Thus, a Si atom residing on a Ga site contributes one mobile negative charge (a conduction electron) and one positive immobile charge to the GaAs lattice, and the material is n-type (more conduction electrons than holes).

As is a Column-V element, so Si has one less valence electron than As. When a Si atom resides on a As site in a GaAs crystal, all four of its valence electrons will participate in covalent bonding with neighboring Ga atoms. There is room for one more valence electron to be "accepted" from a nearby covalent bond, to fill the outer shells of each of the neighboring Ga atoms. Thus, the Si atom is easily ionized with negative charge, resulting in a half-filled covalent bond (which originally contributed the electron to fill the outer shells of the neighboring Ga atoms) with an associated positive charge ($+q$), that can easily move from one lattice site to another. Thus, a Si atom residing on an As site contributes one mobile positive charge (a hole) and one negative immobile charge to the GaAs lattice, and the material is p-type (more holes than conduction electrons).

Problem 2

a) The material is p-type, since Boron is a Column-III element and behaves as an acceptor (contributing one hole per B atom) when it resides on a lattice site in a Si crystal. At room temperature, the intrinsic carrier concentration in Si is $n_i = 10^{10}$ cm^{-3}. $N_A = 10^{15}$ cm^{-3}; $N_D = 0$. Since $N_A - N_D >> n_i$, we can use the equations on Slide 14 of Lecture 17:
$p = N_A - N_D = 10^{15}$ cm^{-3}; $n = n_i^2/(N_A - N_D) = (10^{10}$ cm$^{-3})^2 / 10^{15}$ cm$^{-3} = 10^5$ cm^{-3}.
Since p > n, the material is p-type.
The majority carrier concentration $p = 10^{15}$cm^{-3} and the minority carrier concentration $n = 10^5$ cm^{-3}.

b) Arsenic is a Column-V element and behaves as a donor (contributing one conduction electron per As atom) when it resides on a lattice site in a Si crystal. Since $N_D - N_A >> n_i$, we can use the equations on Slide 14 of Lecture 17:
$N_D = 10^{17}$ cm^{-3}, $N_A = 10^{15}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3}
Majority carrier concentration: $n = N_D - N_A = 10^{17} - 10^{15}$ cm$^{-3} = 9.9 \times 10^{16}$ cm^{-3}
Minority carrier concentration: $p = n_i^2/(N_D - N_A) = (10^{10}$ cm$^{-3})^2 / 9.9 \times 10^{16}$ cm$^{-3} = 1010$ cm^{-3}.

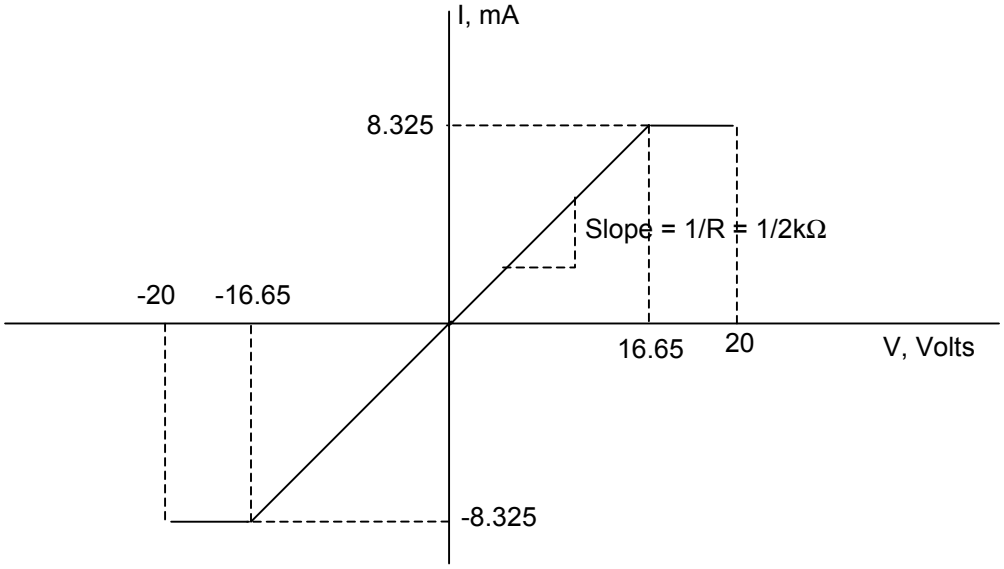
c) Using the graph on Slide 11 of Lecture 17, for $n_i = 9.9 \times 10^{17}$ cm^{-3} the temperature is approximately 1000K.

Problem 3

a) $N_D = 10^{18}$ cm^{-3}, $N_A = 0$, $n_i = 10^{10}$ cm^{-3} at room temperature. Since $N_A - N_D >> n_i$, we can use the equations on Slide 14 of Lecture 17.
$n = N_D - N_A = 10^{18}$ cm^{-3}, $p = n_i^2/(N_D - N_A) = (10^{10}\text{ cm}^{-3})^2/10^{18}\text{ cm}^{-3} = 10^2$ cm^{-3}.
$\mu_n = 300$ cm^2/V·s from chart on Slide 7 of Lecture 18.
Then $\sigma = qn\mu_n + qn\mu_p \approx qn\mu_n = 1.6 \times 10^{-19} \times 10^{18} \times 300 = 1/\rho$, and $\rho = 0.021\ \Omega\cdot$cm.
This value for ρ can also be obtained from the graph on Slide 10 of Lecture 18.
The sheet resistance is given by $R_s = \rho/t = 0.02\ \Omega\cdot\text{cm}/0.5 \times 10^{-4}\text{cm} = 400\ \Omega/\square$

b) $R = \rho L/Wt = 0.02\Omega\cdot\text{cm} \times 5\mu\text{m} / (1.0\mu\text{m} \times 0.5\ \mu\text{m}) = 2\ \text{k}\Omega$ (5 squares)

c) $\upsilon_{sat} = \varepsilon_{sat} \times \mu_n \Rightarrow \varepsilon_{sat} = \upsilon_{sat}/\mu_n = 10^7$ cm/s / 300 cm^2/V·s $= 3.33 \times 10^4$ V/cm
Then the saturation voltage is given by $V_{sat} = \varepsilon_{sat} \times L = 3.33 \times 10^4$ V/cm $\times$ 5 x 10^{-4} cm = 16.65 V and $I_{sat} = V_{sat}/R = 16.65\text{V} / 2\ \text{k}\Omega = 8.325\text{mA}$. The I-V characteristic is sketched below.



Problem 4

a) The junction capacitance is given by: $C_j = \varepsilon_{Si} A_D / W_j$. In this case, $\varepsilon_{Si} = 10^{-12}$ F/cm, A_D=2μm x 5μm and W_j = 1μm.
Then $C_j = 10^{-12}$ F/cm x 2 x 10^{-4}cm x 5 x 10^{-4}cm / 1 x 10^{-4}cm = 10^{-15} F = 1 fF.

b) When $V_D < 0$, the junction is reverse-biased and the potential barrier to carrier diffusion is increased, which implies that the width of the depletion region increases (see Slide 9 of Lecture 19). Since the width of the depletion region increases, the capacitance will decrease since junction capacitance is inversely proportional to the width of the depletion region.

Key Points to Remember about pn-Junction Capacitance

- A region depleted of mobile charge carriers ("the depletion region") exists at the junction between p-type and n-type material, because the majority carriers which were originally located in this region diffused across the junction, leaving behind the immobile dopant ions. (Diffusion of mobile particles occurs whenever a gradient in their concentration exists. The particles diffuse from the region of higher concentration to the region of lower concentration.)
- The charge density in the depletion region is non-zero because of the dopant ions (negatively charged acceptor ions on the p-side, and positively charged donor ions on the n-side). Charge is therefore "stored" in the depletion region of a pn junction (negative charge on the p-side, positive charge on the n-side).
- The charge distribution in the depletion region results in a "built-in" electric field (pointing from the n-side to the p-side) and therefore a "built-in" voltage (higher potential on the n-side) across the depletion region. This built-in electric field counteracts the diffusion of carriers across the junction, so that at equilibrium (V_D = 0 V) no net current flows across the junction. (The built-in electric field results in hole drift from the n-side to the p-side, and electron drift from the p-side to the n-side; this movement of carriers is opposite to that due to diffusion. You can visualize equilibrium as a situation in which the diffusion and drift currents exactly cancel out, or as a situation in which a potential barrier exists to prevent diffusion across the junction.)
- A forward bias ($V_D > 0$, *i.e.* higher voltage applied to the p-side than to the n-side) counteracts the built-in voltage, so that carriers can diffuse across the junction. Because the voltage dropped across the depletion region is reduced, the charge stored in the depletion region is reduced. This means that the width of the depletion region is reduced. (Note that the charge density in the depletion region is dictated by the net doping concentration, and does not change with bias; thus, the only way to change the amount of charge stored in the depletion region is to change its width.) When the forward bias is applied, the circuit must supply carriers to the diode in order to cause the depletion width to shrink: holes flow into the p-side to "cover up" some of the ionized acceptor ions at the edge of the depletion region; electrons flow into the n-side to "cover up" some of the ionized donor ions at the edge of the depletion region.
- A reverse bias ($V_D < 0$, *i.e.* higher voltage applied to the n-side than to the p-side) enforces the built-in voltage, so that the voltage dropped across the depletion region is increased and no carriers can diffuse across the junction. (The only current which can flow across the junction is that due to drift of minority carriers, *e.g.* electrons in the p-side of the depletion region drifting into the n-side due to the force of the electric field in this region.) This means that the width of the depletion region is increased. When the reverse bias is applied, the circuit must remove carriers from the diode in order to cause the depletion width to increase: holes flow out of the p-side to "uncover" ionized acceptor near the edge of the depletion region; electrons flow out of the n-side to "uncover" ionized donor ions near the edge of the depletion region.
- In summary, mobile charge must be added to (in the case of increasing forward bias) or removed from (in the case of increasing reverse bias) each side of a pn junction when the applied voltage changes. This charge is effectively added/subtracted at the edges of the depletion region, *i.e.* separated by a distance equal to the depletion width. This behavior of the diode is modeled as a capacitance: the "plates" of the capacitor are the conductive p-type and n-type quasi-neutral regions; the "dielectric" between the plates of the capacitor is the depleted region of Si.