UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

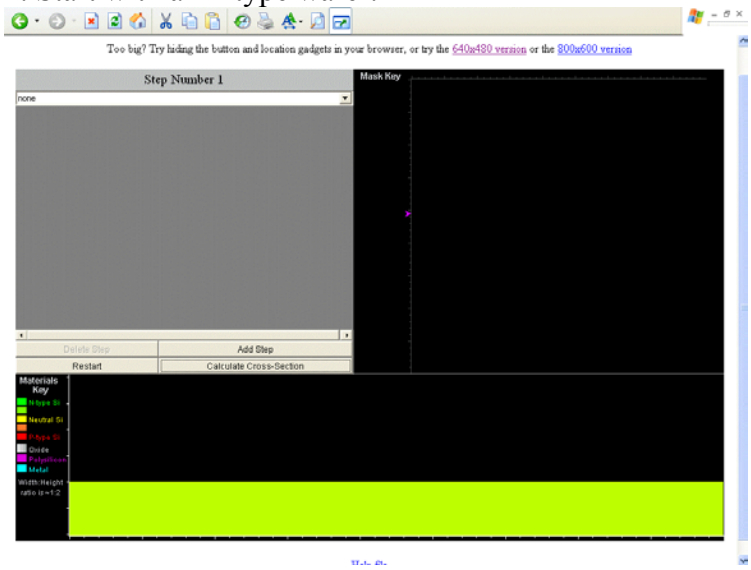
EECS 40 **Fall 2003**

Homework #11 Solutions

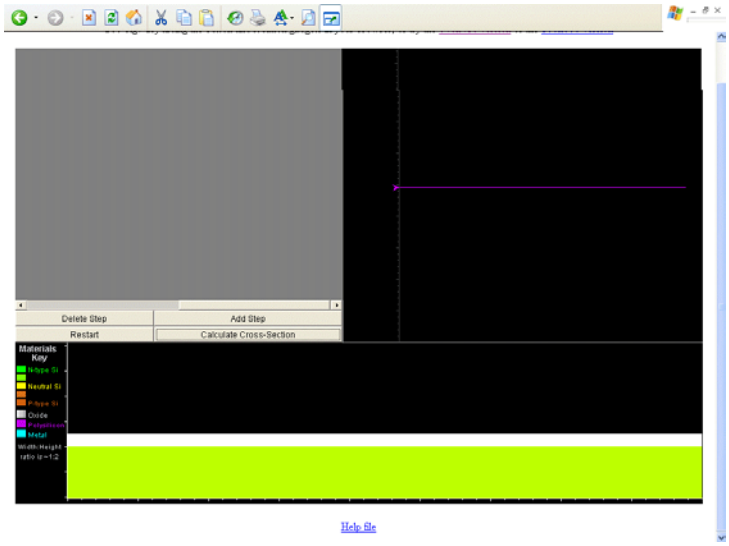
Problem 1:

Create a fabrication process and mask set using SIMPLer for a simple metal-oxide-semiconductor (MOS) capacitor structure which uses metal (aluminum) for the upper electrode and doped Si as the lower electrode:

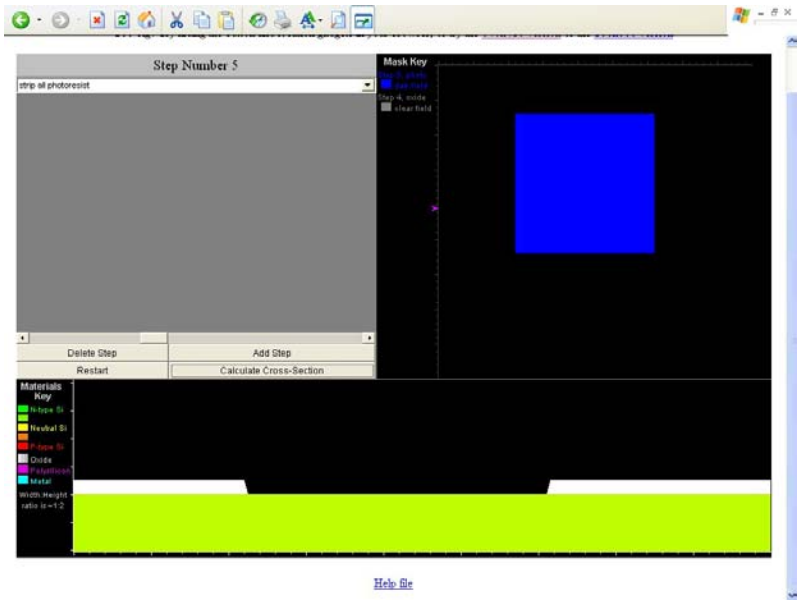
1. Start with an n-type wafer.



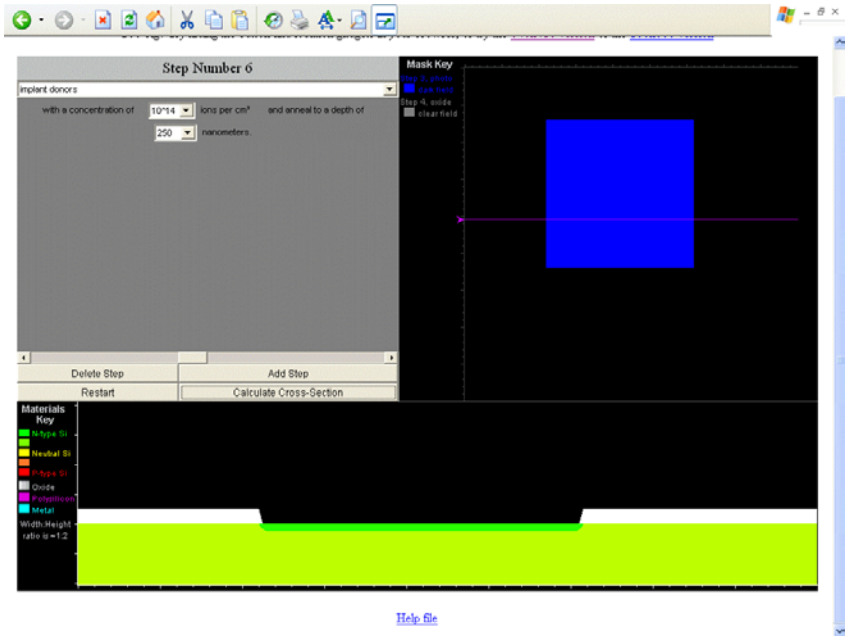
2. Grow 500 nm of silicon dioxide (SiO2).



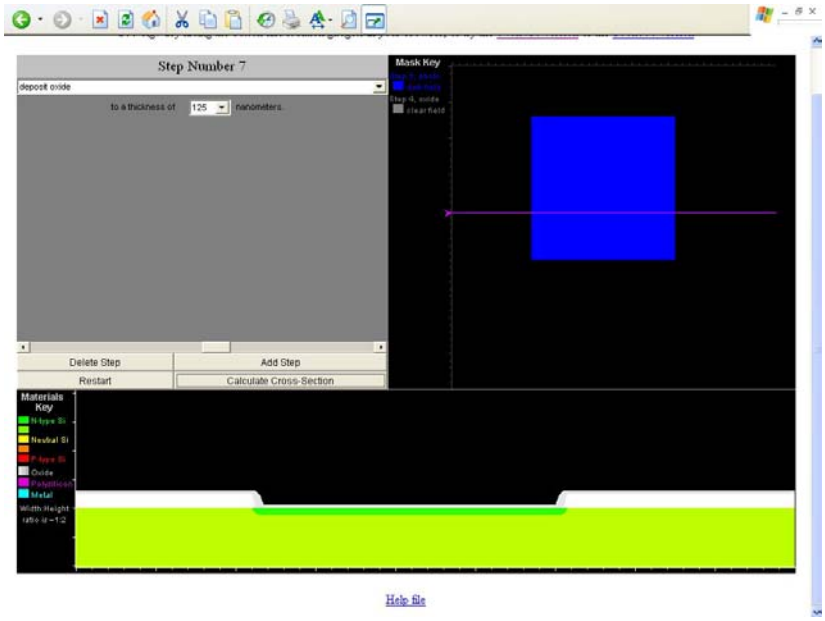
3. Pattern the oxide:
a. Deposit photoresist
b. Pattern the photoresist so that it covers the wafer except in a square region 10 µm × 10 µm.
c. Etch away the oxide in the 10 µm × 10 µm square region, using an etchant that does not attack either the photoresist or silicon. (In SIMPLer, use a "pattern oxide" step.)
d. Strip the photoresist



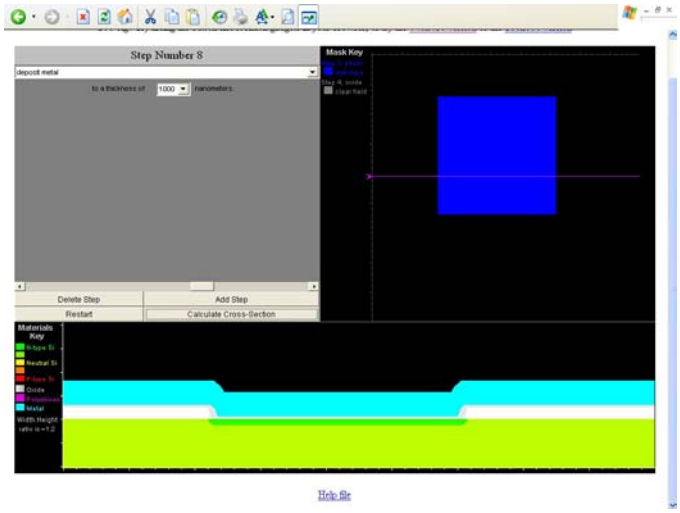
4. Implant phosphorus donor atoms (dose = 1014 cm-2); anneal to a depth of 250 nm.



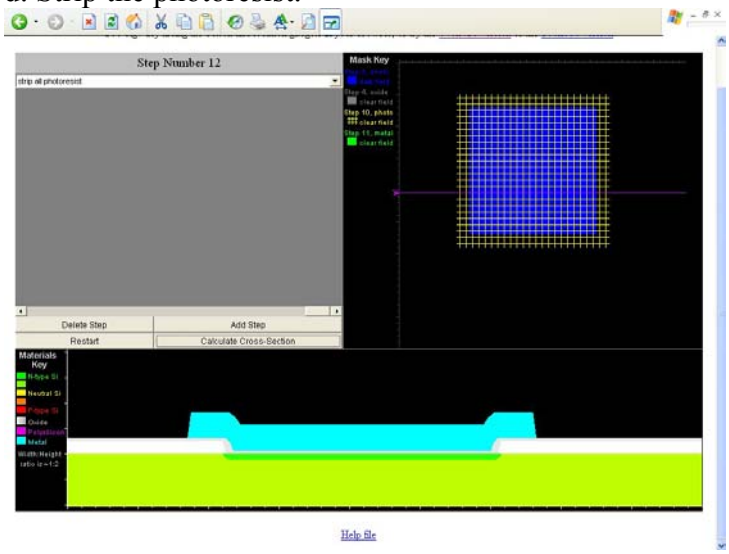
5. Grow 50 nm silicon dioxide.



6. Deposit a 1 µm thick aluminum layer.

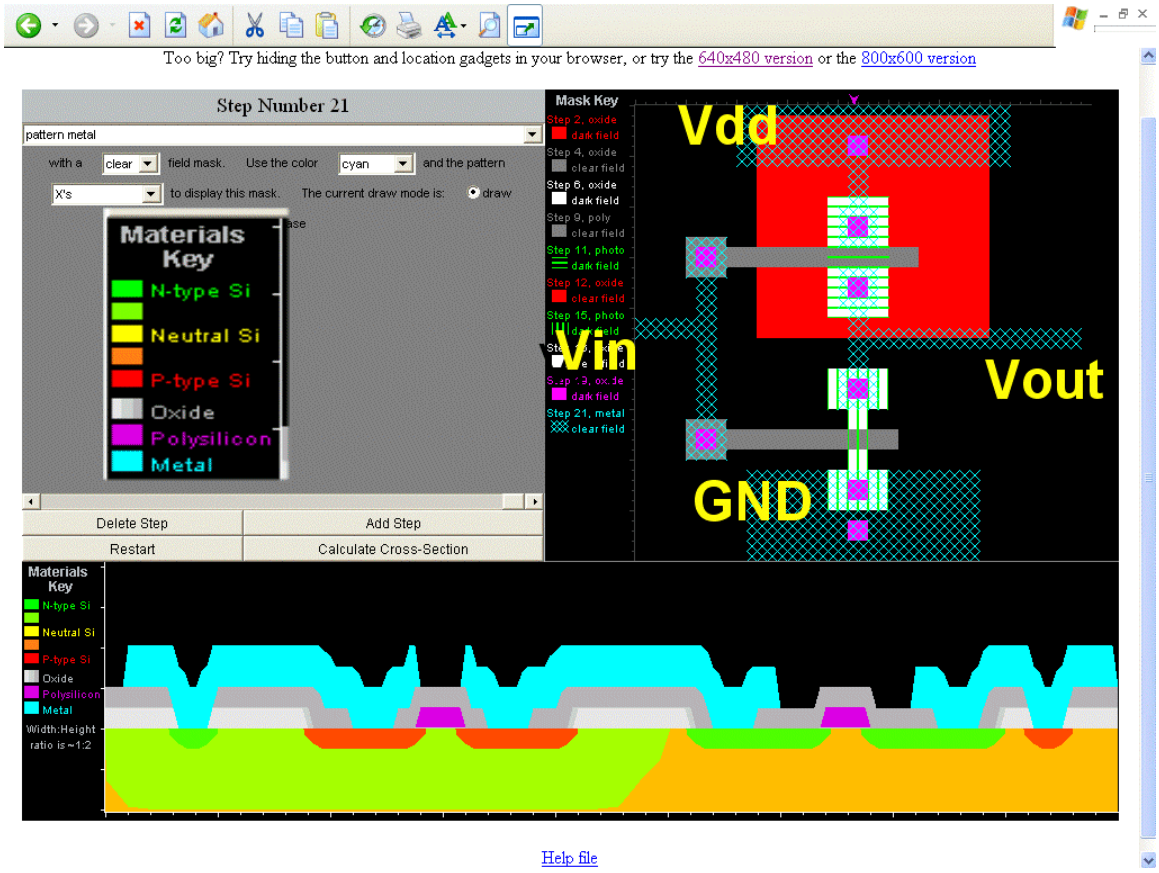


7. Pattern the metal:
a. Deposit photoresist
b. Pattern the photoresist so that only a region 12 µm × 12 µm square remains, centered over the region of thin oxide.
c. Etch away the metal outside the 12 µm × 12 µm region, using an etchant that does not attack either the photoresist or oxide.
d. Strip the photoresist.



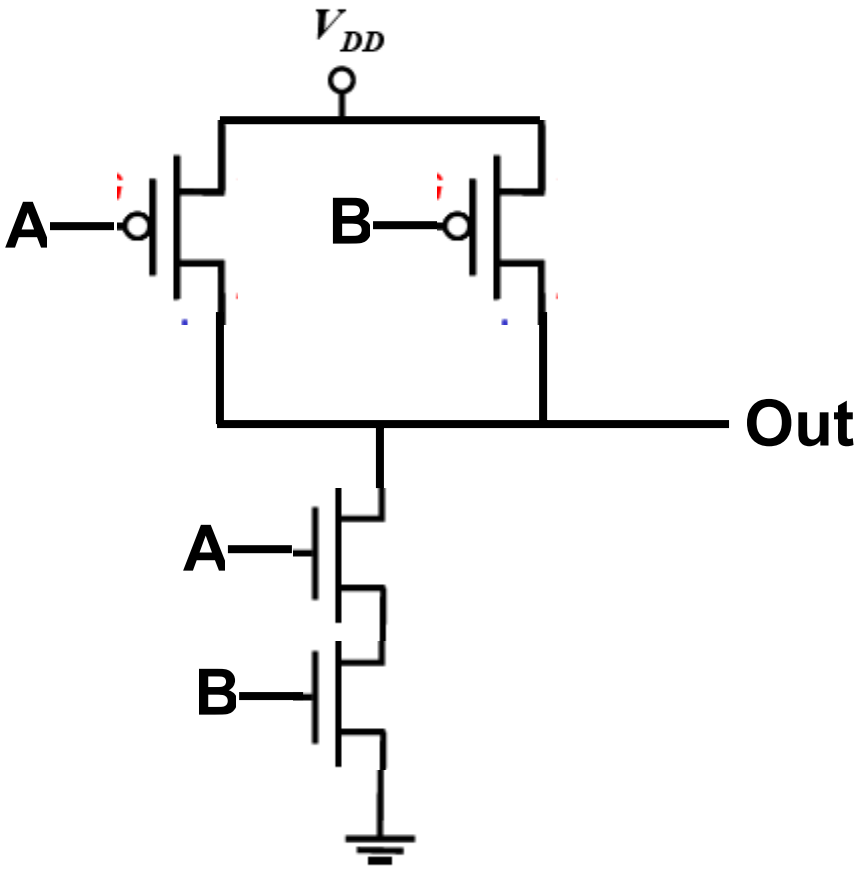
Problem 2:

Note that (W/L) for the PMOS is three times as large as (W/L) for the NMOS.



Problem 3:

Vout=$\overline{(AB)}$



Problem 4: IC Fabrication Technology Advancement

The number of square dice ("chips") per wafer can be estimated to be $N = \pi (R - S)^2 / S^2$, where R is the radius of the wafer and S is the length of one side of the dice. Suppose that the cost of processing a single 200mm-diameter wafer in a particular process (0.18 μm minimum feature size) is $2000, and that 90% of the dice fabricated are good (*i.e.* "yield" is 90%).

a) Determine the processing cost per good die, for a die size of 0.5 cm.

N=Pi*(100mm- 5 mm)^2/(5 mm^2)= 1134 dice/wafer
N*Yield=1134.1 *.9 = 1020 dice/wafer
Cost/(N*yield)=2000 / 1020 = $1.961 / die

b) By scaling the technology from 0.18 μm minimum feature size to 0.13 μm minimum feature size, the chip size can be proportionately reduced. However, the yield goes down to 70%. Determine the cost per good die for the scaled technology.

Length/die = 5mm * (.13/.18) = 3.611mm
N=Pi*(100mm- 3.6 mm)^2/(3.6 mm^2)= 2238 dice/wafer
N*Yield=2238 *.7 = 1566 dice/wafer
Cost/(N*yield)= 2000 / 1566 = $1.277 / die

c) Suppose the cost of processing a 300mm-diameter wafer in the 0.13 μm process is $3,000. What is the minimum yield required in order to make it worthwhile to run 300mm-diameter wafers instead of 200mm-diameter wafers?

for the 300mm wafer Cost/(N*yield) <= $1.277 / die

$3000/ (Pi*(150mm- 3.6 mm)^2/(3.6 mm^2) * Yield)<= $1.277 / die

3000 / (5163 * Yield) <= $1.277 / die

Yield >= 45.5 %

Minimum yield is 46%. Therefore it is more cost effective to manufacture chips on larger-diameter wafers, if reasonable yields (>50%) can be achieved.