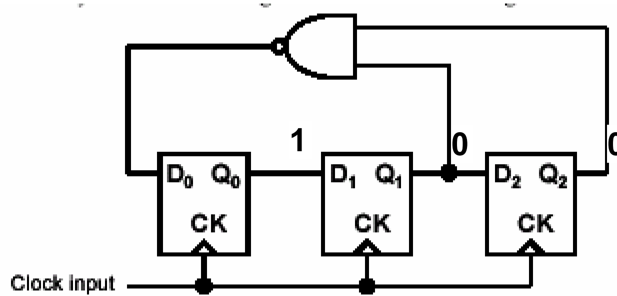
UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 **Fall 2003**

Homework #10 Solutions

Problem 1

Initial state:



Time	Q_0	Q_1	Q_2	$D_0 = Q_1$ NAND Q_2
Start	1	0	0	1
1st Shift	1	1	0	1
2nd Shift	1	1	1	0
3rd Shift	0	1	1	0
4th Shift	0	0	1	1
5th Shift	1	0	0	1

The circuit returns to its initial state after 5 shifts.

Problem 2

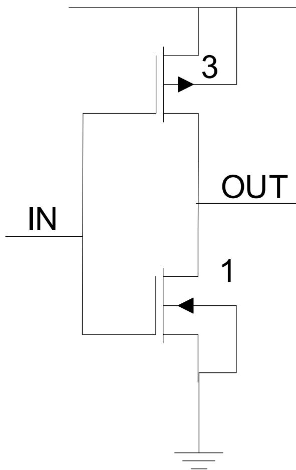
1. Decrease gate-oxide thickness T_{ox}:
   Decreasing the gate-oxide thickness will increase the MOSFET gate capacitance, since $C_{gate} = W \times L \times C_{ox}$ where $C_{ox} = \varepsilon_{ox}/T_{ox}$ (units: F/cm^2). The extrinsic component of the output capacitance C_L that is associated with the fanout logic gate(s) will therefore increase. (The driving logic gate "sees" the gate capacitances at the input(s) to the fanout logic gate(s).) Dynamic power consumption due to C_L charging, $P_{dyn} \propto C_L V_{DD}^2$, therefore increases.

2. Increase power-supply voltage V_{DD}:
   Increasing the power-supply voltage V_{DD} will increase the dynamic power consumption due to C_L charging, since $P_{dyn} \propto V_{DD}^2$. (It takes more energy to charge a capacitance to a higher voltage.)

3. Reduce MOSFET channel length L:
   Reducing the channel length L reduces the MOSFET gate capacitance (see 1 above). This results in decreased C_L and hence decreased dynamic power consumption P_{dyn}. However, the subthreshold MOSFET leakage current I_{leak} increases, so that the static component of power consumption, $P_{stat} = I_{stat}V_{DD} = I_{leak}V_{DD}$ increases. (Overall, the power consumption will decrease.)

Problem 3

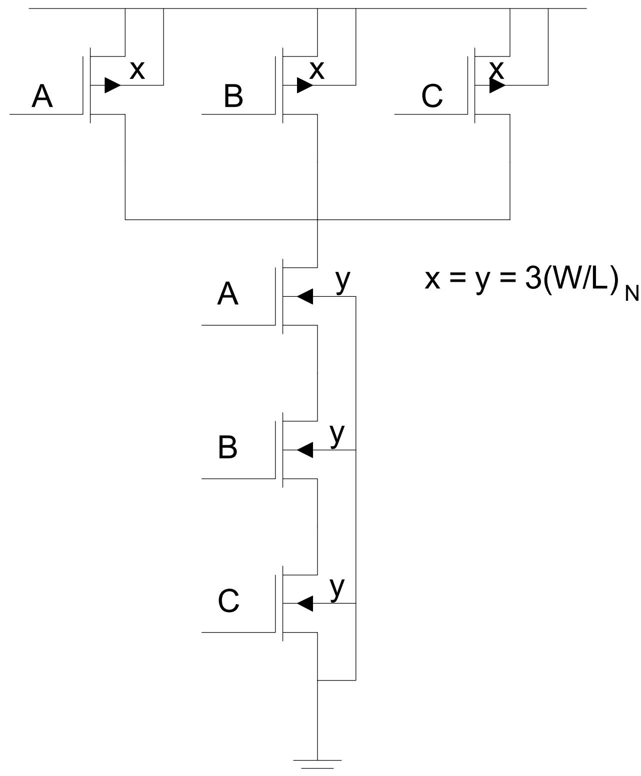
a) It is given that $(W/L)_P = 3(W/L)_N$ in order for R_P to be comparable to R_N. The relative sizes of the transistors for the inverter are shown below for best performance and balanced H-L and L-H propagation delays. Let R_N and R_P be the equivalent on-resistances for the NMOS and PMOS transistors for the inverter shown below.



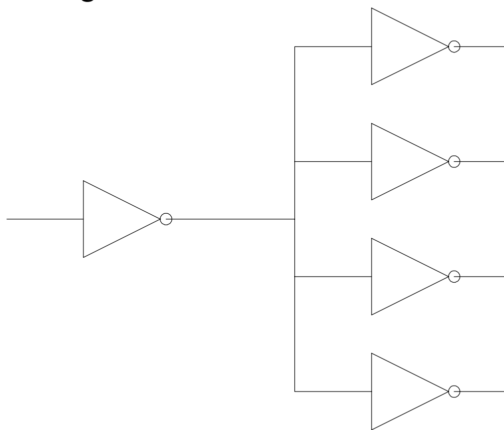
Let x be the size $(W/L)_P$ of the PMOS transistors in the 3-input NAND gate shown below. Let y be size $(W/L)_N$ of the NMOS transistors in the circuit. The worst-case pull-up delay occurs when only one PMOS transistor is on. The worst-case pull-down delay occurs when all three NMOS transistors are on.

For the NAND gate, the pull-up delay is given by: $t_{pLH} = 0.69(R_P/x)C_L$ and the pull-down delay is given by $t_{pHL} = 0.69(3R_N/y)C_L$. For the inverter, the pull-up delay is given by $t_{pLH\text{-}INV} = 0.69(R_P)C_L$ and the pull-down delay is given by $t_{pHL\text{-}INV} = 0.69(R_N)C_L$. If we want the pull-up and pull-down delays of the NAND gate to be comparable to the inverter, then x = 1 and y = 3. This means that PMOS size is $(W/L)_{P\text{-}NAND} = (W/L)_{P\text{-}INV} = 3(W/L)_{N\text{-}INV}$ and the NMOS transistor sizes must be tripled so that the equivalent resistance is the same as the pull-down equivalent resistance of the inverter: $(W/L)_{N\text{-}NAND} = 3(W/L)_{N\text{-}INV}$. This implies that the PMOS and NMOS transistors in the NAND gate have equal widths:
$(W/L)_{P\text{-}NAND} = (W/L)_{N\text{-}NAND}$.

The NMOS transistors have to be sized the same as the PMOS transistors because adding devices in series slows down the circuit, hence the NMOS devices must be made wider to avoid the performance penalty.



b) The figure below shows our circuit under analysis:



In Lecture 32 and Example 5.4 in Rabaey *et al.* the NMOS W/L ratio is given as 0.375/0.25 = 1.5 and the PMOS W/L ratio is given as 1.125/0.25 = 4.5. Hence R_P = 31kΩ/4.5 = 6.89 kΩ and R_N = 13kΩ/1.5 = 8.67 kΩ.

Using Table 5-2 in Rabaey *et al.*:
The extrinsic load capacitance for both H-L and L-H transitions is given as:
$C_{extrinsic-L} = 4(C_{G3} + C_{G4}) + C_W = 4(2.28 + 0.76) + 0.12$ [fF] = 12.28 fF.
The intrinsic capacitance for the H-L transition is given by:
$C_{intrinsic-L} = (C_{GD1} + C_{GD2} + C_{DB1} + C_{DB2}) = (0.23 + 0.61 + 0.66 + 1.5)$ [fF] = 3 fF.

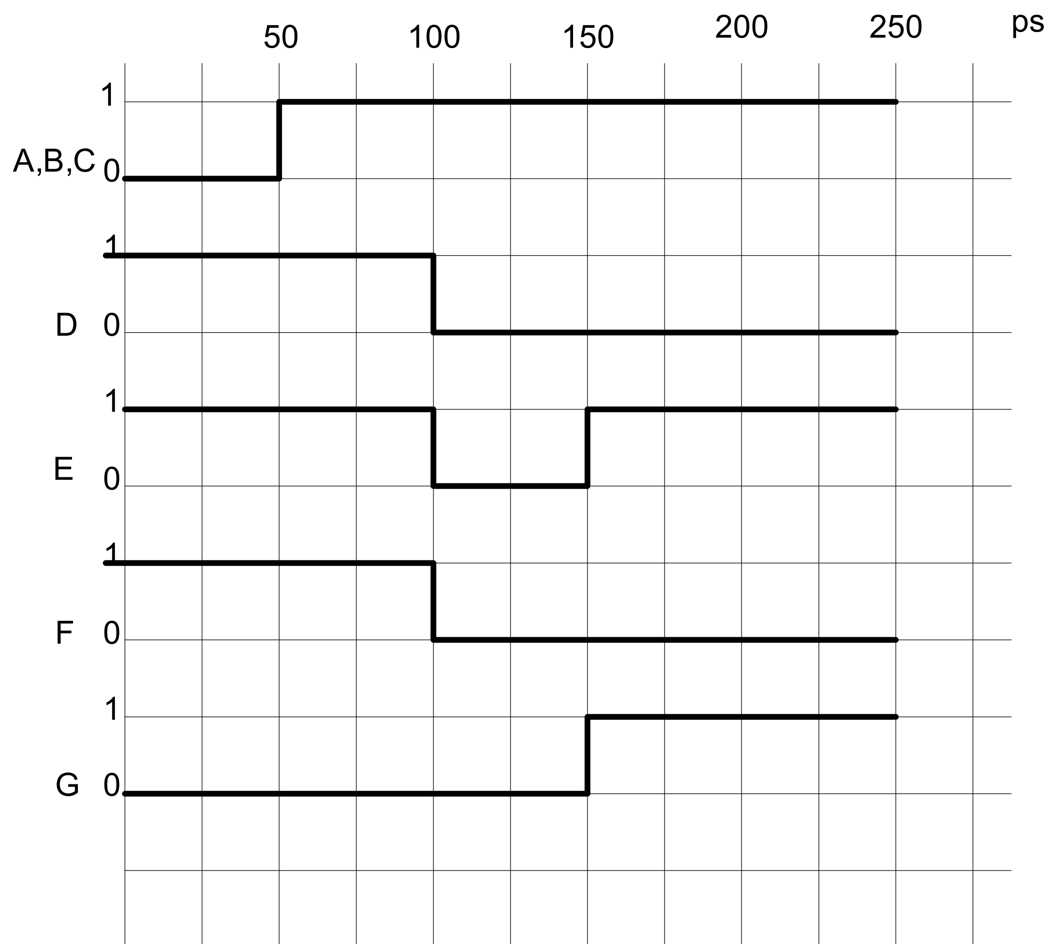
The intrinsic capacitance for the L-H transition is given by:
$C_{intrinsic\text{-}L} = (C_{GD1} + C_{GD2} + C_{DB1} + C_{DB2}) = (0.23 + 0.61 + 0.90 + 1.15)$ [fF] = 2.89 fF.

The total load capacitance for the H-L transition is: 12.28 + 3 = 15.28 fF
The total load capacitance for the L-H transition is: 12.28 + 2.89 = 15.17 fF

The propagation delays for each transition are calculated as follows:
$t_{pHL} = 0.69 R_N C_{L\text{-}HL} = 0.69(8.67\ k\Omega)(15.28\ fF) = 91.4$ ps
$t_{pLH} = 0.69 R_P C_{L\text{-}LH} = 0.69(6.89\ k\Omega)(15.17\ fF) = 72.1$ ps

The propagation delay is the average of the two numbers calculated above:
$t_p = (t_{pHL} + t_{pLH})/2 = 81.75$ ps

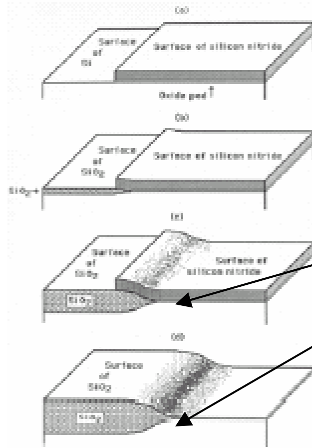
c)



Problem 4

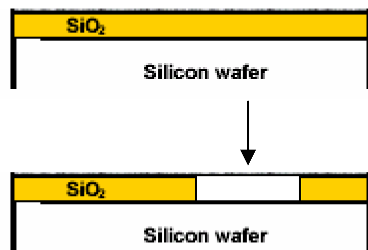
a) Approach 2 results in less surface topography (variation in surface height = oxide thickness/2) and therefore better step coverage since the LOCOS process creates a smoother surface with no abrupt transitions. Approach 1 results in more surface topography (variation in surface height = oxide thickness) and abrupt transitions. The approaches are contrasted in the pictures below.

Local Oxidation (LOCOS)



Resulting surface varies in height by ½ times the oxide thickness, with smooth transitions from the surface of SiO_2 to Si.

Deposition and Patterning



SiO_2 is deposited uniformly on the wafer and selectively removed to create a window. The resulting surface varies in height by the full oxide thickness, with abrupt transitions between the SiO_2 and Si.

b) From the last equation, we get: $r = m\nu^2/q\nu B$. From the first equation, $\nu = (2qV/m)^{1/2}$. Substituting, we get: $r = (m/qB)(2qV/m)^{1/2} = (1/B)(2mV/q)^{½}$. Hence, r is dependent on both m/q and V.

Each ion has a unique mass-to-charge ratio. Varying V affects the kinetic energy of the ions, and hence the velocity ν. Since the radius of curvature r for the ions depends on the mass-to-charge ratio and the applied voltage V, we can select a particular ion species (*e.g.* As^+) by varying V so that r is "just right" to allow the selected ions to pass through the resolving aperture of the accelerator, to be accelerated and implanted into the wafers.