UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 40 — Fall 2003
Introduction to Microelectronic Circuits — Prof. King

MIDTERM EXAMINATION #2

November 3, 2003
Time allotted: 50 minutes

NAME: SOLUTIONS, _____
(print) **Last** **First**

Signature: _____ **STUDENT ID#:** _____

Discussion Section: _____

1. This is a **CLOSED BOOK** exam. However, you may use 2 sheets of notes and a calculator.
2. **SHOW YOUR WORK or REASONING** on this exam.
   (Make your methods clear to the grader.)
3. **Write your answers clearly (legibly) in the spaces (lines, boxes, or plots) provided.**
4. Remember to specify the units on answers whenever appropriate.

SCORE: 1 _____ / 16

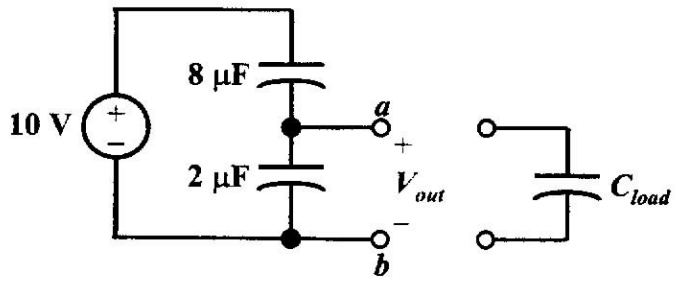
2 _____ / 17

3 _____ / 17

Total: _____ / 50

Problem 1: Energy-Storage Elements and 1st-Order Circuits [16 points in total]

a) Consider the capacitive voltage-divider circuit below. Find V_{out}. How will V_{out} change if a small load capacitance $C_{load} < 2\ \mu F$ is connected between terminals ***a*** and ***b***? **[4 pts]**



$$V_{out} = \frac{8\mu F}{8\mu F + 2\mu F}(10\,V) = 8V$$

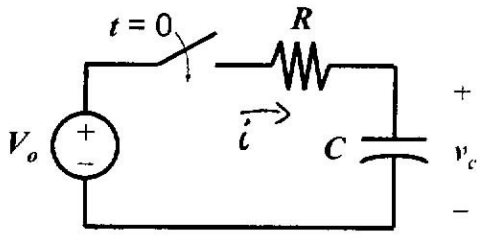
↑ capacitance between terminals a and b

V_{out} = 8 Volts

V_{out} will [increase, (decrease) not change] (circle one) when C_{load} is connected, because

the capacitance between terminals a and b will increase.

b) Consider the following RC circuit:



Provide a physical reason why it takes longer for v_c to reach its final value if R is increased. (Why is the characteristic time constant τ proportional to R?) **[2 pts]**

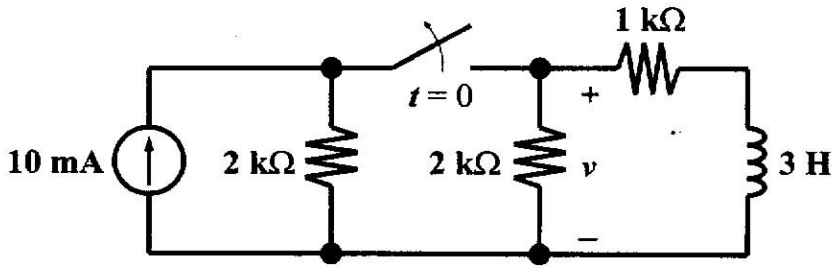
$$i = \frac{V_o - v_c}{R} = C\frac{dv_c}{dt}$$

v_c will take longer to reach its final value if R is increased because

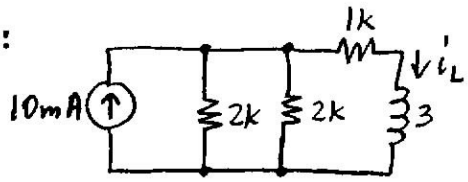
the current flowing through R (to charge C) will decrease, hence it will take longer to deliver the charge $Q = CV_o$.

Problem 1 (continued)

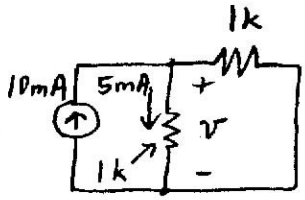
c) Assume that the circuit below is operating in steady state with the switch open for $t < 0$. Find and accurately sketch $v(t)$ for all t. **[10 pts]**



$t<0$:



$\equiv$

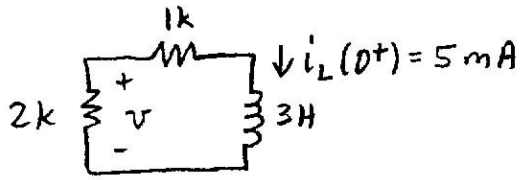


$i_L = 5\,mA$

← inductor behaves as short circuit in steady state

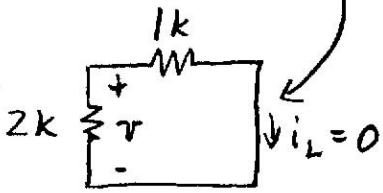
$v(t<0) = 5V$

$t>0$:



$v(0^+) = -10V$

$t=\infty$:

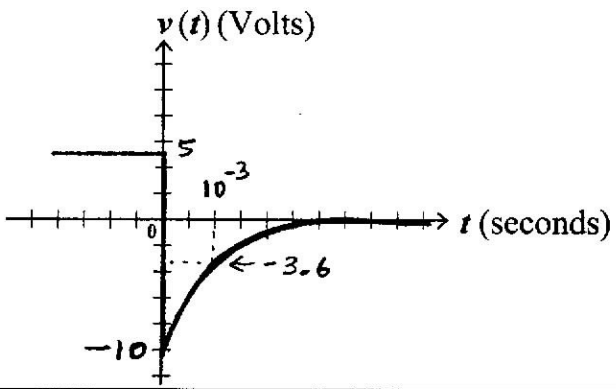


$v(t=\infty) = 0$

$$\tau = \frac{L}{R} = \frac{3H}{2k\Omega + 1k\Omega} = 1\,ms$$

$$v = 0 + [-10 - 0]e^{-t/1ms} = -10e^{-1000t}$$

For $t < 0$: $v(t) =$ 5 V . **For $t > 0$:** $v(t) =$ $-10e^{-1000t}$



Problem 2: Semiconductor Materials and Devices [17 points in total]

a) Consider a Si sample maintained at $T = 300K$, uniformly doped with Arsenic atoms to a concentration 3×10^{16} cm^{-3}. The electron mobility = 1000 cm^2/V•s; hole mobility = 400 cm^2/V•s.

i) Estimate the resistivity of this sample. (Use $q = 1.6\times10^{-19}$ C in your calculation.) **[4 pts]**

As is a Column V element → donor in Si

$N_D = 3\times10^{16}\,cm^{-3}$, $N_A = 0$ $\Rightarrow$ $n = 3\times10^{16}\,cm^{-3}$, $p = \frac{n_i^2}{n} \simeq 3000\ cm^{-3}$

$\rho = [q\mu_n n + q\mu_p p]^{-1} \simeq [q\mu_n n]^{-1}$ since $n >> p$

$\simeq [1.6\times10^{-19} \times 1000 \times 3\times10^{16}]^{-1} = [4.8]^{-1} \simeq 0.2\ \Omega\text{-cm}$

resistivity $\simeq$ 0.2 Ω-cm

ii) How will the resistivity of this sample change if it were to be doped additionally with 3×10^{16} cm^{-3} Phosphorus atoms? **[3 pts]** carrier mobilities would be degraded since $N_D + N_A$ ↑

P is also a Column V element → donor in Si

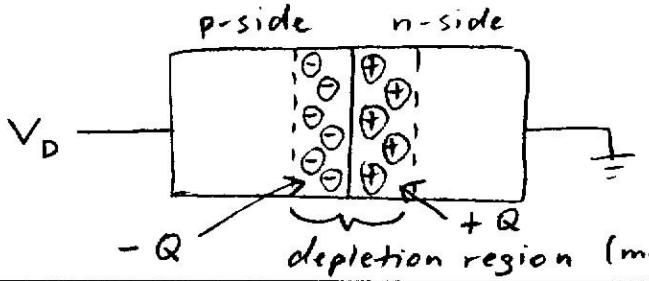
$N_D = 6\times10^{16}\,cm^{-3}$, $N_A = 0$ $\Rightarrow$ $n = 6\times10^{16}\,cm^{-3}$

The resistivity will [increase, (decrease,) not change] (circle one)

by a factor that is [greater than, (less than,) equal to] (circle one) 2 when phosphorus is added because

the number of conduction electrons will double, but μ_n will decrease

b) Explain (using 1 or 2 sentences) why a pn junction has capacitance. **[2 pts]**

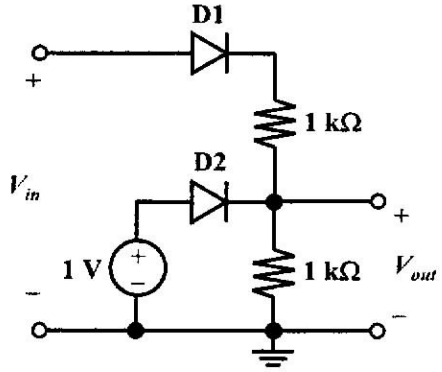


A pn junction has capacitance because

charge is stored in the depletion region of a pn junction. The width of the depletion region, and hence the charge stored, varies with the bias voltage. $C_j \equiv \left|\frac{dQ}{dV_D}\right|$

Problem 2 (continued)

c) Assume the diodes in the circuit below can be modeled as perfect rectifiers.



i) For what values of V_{in} is D1 on? Explain your reasoning. **[3 pts]**

D1 is on for V_{in} > 1 Volt because

forward current can flow in D1 as long as $V_{in} > V_{out}$.

D2 fixes V_{out} at 1V, unless V_{in} causes V_{out} to be > 1 Volt.

ii) For what values of V_{in} is D2 on? Explain your reasoning. **[2 pts]**

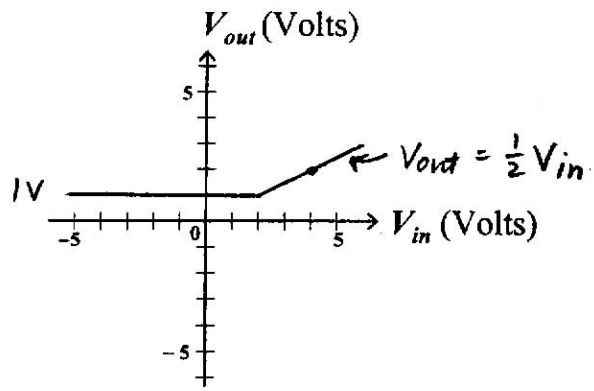
D2 is on for V_{in} < 2 Volts because

if V_{in} exceeds 2V, V_{out} will exceed 1 Volt and D2 will be reverse biased. (If D2 is on for $V_{in} > 2V$, reverse current would have to flow in D2 - which cannot be.)

iii) Accurately plot V_{out} *vs.* V_{in} on the axes provided. **[3 pts]**

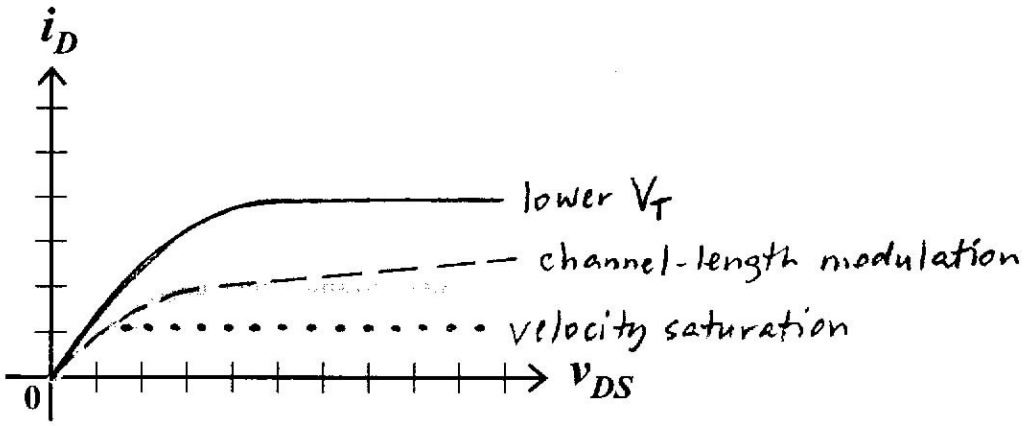
For $V_{in} < 2V$, D2 is on and so V_{out} is fixed at 1V.

For $V_{in} > 2V$, D2 is off and so $V_{out} = \frac{1k\Omega}{1k\Omega + 1k\Omega} V_{in} = \frac{1}{2} V_{in}$



Problem 3: MOSFET and Common-Source Amplifier [17 points in total]

a) The following is the i_D-v_{DS} characteristic of an n-channel MOSFET:



Indicate how this characteristic would change (by drawing the modified i_D-v_{DS} characteristic with appropriate changes in I_{DSAT} and V_{DSAT}):

i) when V_T is lowered – **use a labeled solid line on the plot above [2 pts]**

$I_{DSAT} = k' \frac{W}{2L} (V_{GS} - V_T)^2$ increases

$V_{DSAT} = V_{GS} - V_T$ increases

slope at small $v_{DS} = k' \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2})$ increases

ii) when channel-length modulation is significant – **use a labeled dashed line on the plot above [2 pts]**

no change in V_{DSAT}, slope at small v_{DS}

slope in saturation region > 0

iii) when the current is limited by velocity saturation, rather than pinch-off – **use a labeled dotted line on the plot above [2 pts]**

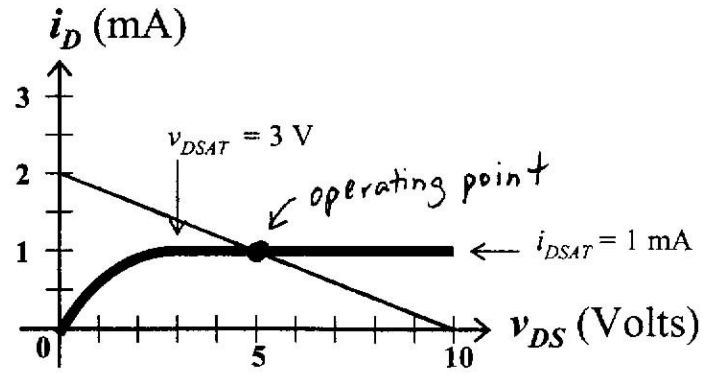
$V_{DSAT} = \frac{L}{\mu} v_{sat} < V_{GS} - V_T$ (decreases)

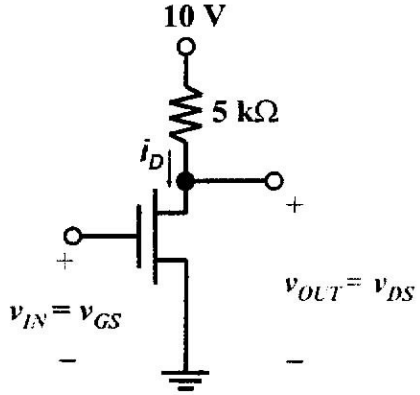
I_{DSAT} decreases

slope at small v_{DS} unchanged

Problem 3 (continued)

b) Below to the left is the i_D *vs.* v_{DS} characteristic for a long n-channel MOSFET with $V_T = 1$ V.





What is V_{GS}? **[2 pts]**

$V_{DSAT} = V_{GS} - V_T$

$3 = V_{GS} - 1 \Rightarrow V_{GS} = 4V$

$V_{GS} =$ 4 Volts

c) Suppose the MOSFET in part (b) is used in the amplifier circuit shown above to the right.

i) Draw the load line on the MOSFET i_D-v_{DS} plot (above to the left). **[3 pts]**

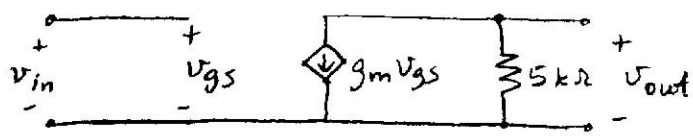
ii) In what region is the MOSFET operating? **[2 pts]**

The MOSFET is operating in the [linear, (saturation), cutoff] (circle one) region because

$v_{DS} > V_{DSAT}$ and $i_D > 0$

iii) What is the incremental change in the output voltage (*i.e.* v_{out}) for a -1 mV change in the input voltage (*i.e.* $v_{gs} = -1$ mV)? **[4 pts]**

small-signal equivalent circuit:



$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{\partial}{\partial v_{GS}} \left[k' \frac{W}{2L} (V_{GS} - V_T)^2 \right]$

$= k' \frac{W}{L} (V_{GS} - V_T)$

$= \frac{2}{9} \frac{mA}{V^2} \times 3V = \frac{2}{3} mS$

$i_{DSAT} = k' \frac{W}{2L} (V_{GS} - V_T)^2 = 1mA$

$\Rightarrow k' \frac{W}{2L} (3)^2 = 1mA$

$k' \frac{W}{L} = \frac{2}{9} mA/V^2$

$v_{out} = -g_m v_{gs} (5k\Omega)$

$= -\frac{2}{3} \times 10^{-3} (-10^{-3})(5 \times 10^3)$

$v_{out} =$ 3.3 mV