UNIVERSITY OF CALIFORNIA
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EE290D — Handout #37
Spring 1999 — T.-J. King

HOMEWORK ASSIGNMENT #4 SOLUTIONS

Problem 1: Amorphous-Si TFT

For a transistor fabricated from a thick semiconductor film with a uniform density of states N_T (cm^{-3}eV^{-1}), we can write Poisson's equation as

$$\frac{d^2\phi}{dx^2} = -\frac{\rho}{\varepsilon_s} = \frac{q^2 N_T \phi}{\varepsilon_s}$$

a) Using the chain rule and the definition of electric potential, we can write

$$\frac{d^2\phi}{dx^2} = -\frac{dE}{dx} = -\left(\frac{dE}{d\phi}\right)\left(\frac{d\phi}{dx}\right) = E\frac{dE}{d\phi}$$

so the Poisson equation becomes

$$E\frac{dE}{d\phi} = \frac{q^2 N_T \phi}{\varepsilon_s}$$

Integrating from the bulk toward the surface yields

$$\int_{bulk}^{surface} E\,dE = \frac{q^2 N_T}{\varepsilon_s}\int_{bulk}^{surface} \phi\,d\phi$$

The electric field E and the potential ϕ are zero in the bulk; thus we obtain

$$\frac{E_s^2}{2} = \frac{q^2 N_T}{\varepsilon_s}\left(\frac{\phi_s^2}{2}\right)$$

where E_s is the surface electric field and ϕ_s is the surface potential. Simplifying, we obtain the following expression for E_s:

$$\boxed{E_s = q\phi_s\sqrt{\frac{N_T}{\varepsilon_s}}}$$

b) At threshold, $\phi_s = \phi_{s(inv)} = \frac{E_G}{2q}$, so

$$\boxed{E_{s(inv)} = \frac{E_G}{2}\sqrt{\frac{N_T}{\varepsilon_s}}}$$

c) The insulator electric field E_i is related to the semiconductor surface electric field by the relationship

$$E_i = \frac{\varepsilon_s}{\varepsilon_i}E_s$$

where ε_i is the dielectric constant for the insulator. At threshold, the insulator electric field is

$$\boxed{E_{i(inv)} = \frac{\varepsilon_s}{\varepsilon_i}\left(\frac{E_G}{2}\sqrt{\frac{N_T}{\varepsilon_s}}\right) = \left(\frac{E_G}{2\varepsilon_i}\sqrt{\varepsilon_s N_T}\right)}$$

d) The voltage across the insulator, V_{ox}, is simply equal to t_iE_i where t_i is the insulator thickness (assuming that there is no charge within the insulator). The threshold voltage is therefore given by the expression

$$V_T = \phi_{s(inv)} + V_{ox(inv)} = \frac{E_G}{2q} + t_iE_{i(inv)} = \frac{E_G}{2q} + t_i\left(\frac{E_G}{2\varepsilon_i}\sqrt{\varepsilon_s N_T}\right) = \frac{E_G}{2q}\left(1 + \frac{qt_i}{\varepsilon_i}\sqrt{\varepsilon_s N_T}\right)$$

e) N_T=10^{17} $cm^{-3}eV^{-1}$; E_G=1.7 eV; t_i = 300 nm; ε_i=7.5:

$$V_T = \frac{1.7}{2}\left(1 + \frac{(1.602x10^{-19})(300x10^{-7})}{7.5x8.854x10^{-14}}\sqrt{(11.7x8.854x10^{-14})(10^{17})/(1.602x10^{-19})}\right) = \mathbf{5.8V}$$

Problem 2: Poly-Si TFT

a) In order to turn on a TFT, the magnitude of the applied gate voltage must be sufficiently large to cause enough energy-band bending in the semiconductor film so that the band edge (conduction-band edge in the case of an n-channel TFT; valence-band edge in the case of a p-channel TFT) at the surface of the semiconductor is very close to the Fermi level (so that the number of mobile carriers is significant). In order to move the band edge close to the Fermi level, the trap states which are energetically located in the central portion of the bandgap must be filled. The higher the concentration of these "deep states" the larger the threshold voltage and the poorer the subthreshold slope (since a larger gate-voltage swing is needed to achieve a given amount of band bending and increase in the mobile carrier concentration, for a given increase in drain current). **Therefore, V_T and S are more strongly correlated with the deep states.**

Above threshold, the drain current I_D increases with gate voltage V_G according to the equation

$$|I_D| = \frac{W}{L}\mu_{eff}C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D$$

The mobile carrier (areal) density, $C_{ox}(V_G\text{-}V_T)$, nominally increases linearly with gate voltage. However, if trap states exist in the band gap at the Fermi level (which is near the band edge, for a device operating above threshold), a portion of the carriers induced by increasing the gate voltage will be trapped, so that the mobile carrier density increases sub-linearly with gate voltage. Effectively, the carrier mobility μ_{eff} is degraded; hence the higher the density of the "tail states," the lower the effective mobility.

Leakage current in a poly-Si TFT occurs via trap-assisted tunneling (field emission and thermionic emission) of carriers (holes, in the case of an n-channel TFT; electrons, in the case of a p-channel TFT) in the channel near the drain. The traps which are located near to the band edges will provide the highest probability of tunneling, because of the small tunneling distance (for a given electric field) and/or low thermal energy required for the trapped carrier to move into the energy band. (See slide entitled "TFT Leakage Current" from Lecture #13 for reference.) The higher the density of these "tail states," the higher the leakage current.

In summary, μ_{eff} and I_{min} are more strongly correlated with the tail states.

b) As the magnitude of the gate voltage V_G increases, the total (trapped + mobile) charge induced in the channel increases. The Fermi level at the surface of the channel moves closer to the conduction band as the mobile charge there increases. The lower the density of trap states in the band gap, the "faster" the Fermi level will move toward the conduction band as the gate voltage increases.

The drain-current activation energy E_A can be taken to be equivalent to the grain-boundary barrier height, if the poly-Si channel film is modelled as a film comprising monocrystalline grains of uniform size separated by grain boundaries containing defects associated with trap states in the band gap. E_A can be taken to be equivalent to the energy barrier at the source-channel junction, if the poly-Si channel film is modelled as a uniformly defective film (as in the "effective medium" approach). In either case, the rate at which E_A decreases with increasing V_G is an indicator of the density of trap states near the Fermi level. For V_G well above threshold, the magnitude of E_A is correlated to the integrated defect density.

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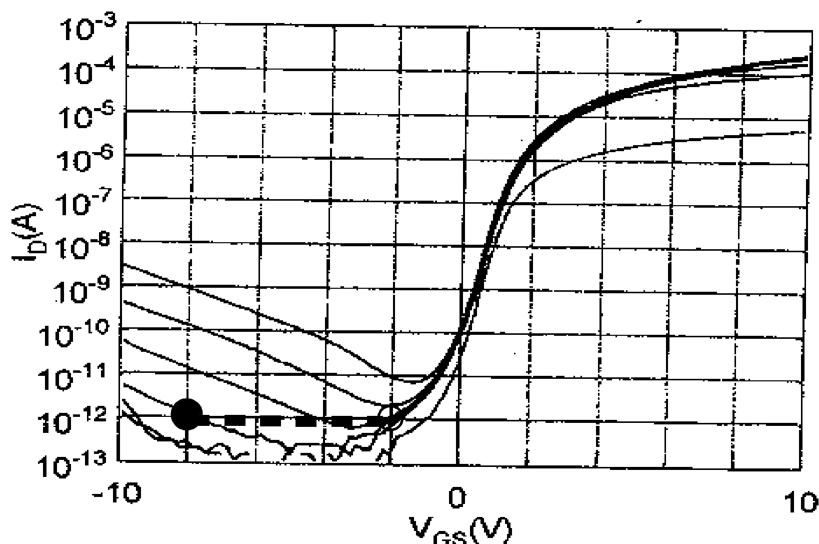
Parameter	Higher in Device A or Device B?	Brief Justification
Threshold Voltage	Device A	The “knee” in the E_A-vs.-V_G curve occurs at a higher value of V_G for Device A.
Deep State Density	Device A	V_T is correlated with deep-state density. Also, the slope of the E_A-vs.-V_G curve is less steep for Device A at higher values of E_A.
Tail State Density	Device B	The slope of the E_A-vs.-V_G curve is less steep for Device B at lower values of E_A.
Integrated Defect Density	Device B	At high values of V_G, E_A is higher for Device B.

<u>Problem 3</u>: Multiple-Gate TFT

When V_{GS} > ~ -3 V: The drain current is dominated by electron current, which increases exponentially with increasing V_{GS} and is almost independent of V_{DS} (classical subthreshold current). The lower transistor has a more positive V_{GS}; hence, the applied V_{DD} is divided such that <u>most of the applied voltage falls across the upper transistor</u> so that the two transistors have equal drain currents.

When V_{GS} < ~ -3 V: The drain current is dominated by hole current, which increases exponentially with $|V_{GS}|$ as well as with V_{DS} (Figure P3a). The upper transistor has a more negative V_{GS}; therefore, the applied V_{DD} is divided such that <u>most of the applied voltage falls across the lower transistor</u> so that the two transistors have equal drain currents.

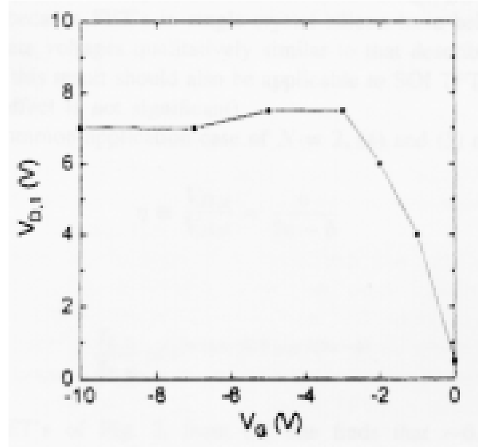
a) For each V_{GS} and V_{DD}, only one V_{D1} can be found such that the drain currents match in the two transistors. For the upper transistor, $V_{GS} = V_G - V_{D1}$ and $V_{DS} = V_{DD} - V_{D1}$; for the lower transistor, $V_{GS} = V_G$ and $V_{DS} = V_{D1}$. By judicious trial and error, the value of V_{D1} for any particular value of $V_G < 0$ can be found from the I_D-V_{GS} characteristics for an individual TFT. The graphical solution for $V_{DD} = 10$ V and $V_G = -2$ V is illustrated below.



<u>Lower TFT</u> (open circle): $V_{GS} = -2$ V; $V_{DS} = 6$ V

<u>Upper TFT</u> (filled circle): $V_{GS} = -8$ V; $V_{DS} = 4$ V

V_{D1} is plotted as a function of V_G, for V_{DD} = 10 V, below:



b) For sufficiently negative gate voltages and large drain voltages, the drain current can be empirically approximated as

$$I_D = Ce^{aV_{DS} - bV_{GS}}$$

where C is an arbitrary constant, and a and b are constants which can be found from the TFT *I-V* characteristics. (a = ln 3 V^{-1} and b = ln 2 V^{-1} for the data in Figure P3a.) Setting the drain currents for the two transistors to be equal, we obtain the following equation:

$$Ce^{a(V_{DD} - V_{D1}) - b(V_G - V_{D1})} = Ce^{a(V_{D1}) - b(V_G)}$$

Solving this equation for V_{D1}, we obtain

$$\boxed{V_{D1} = V_{DD}\left(\frac{a}{2a-b}\right)}$$

For V_{DD}=10 V, this evaluates to **~7 V**, which is in good agreement with the graphical solution.

Problem 4: Organic TFTs

a) Advantages: Organic TFTs can potentially be fabricated at much lower cost than Si-based TFTs and can be more easily fabricated on a variety of substrate materials, including plastic (for lightweight, rugged and flexible display applications) because high processing temperatures are not required.
Disadvantages: Organic TFTs generally have much poorer *I-V* characteristics (high threshold voltage, poor subthreshold swing) and hence require much higher operating voltages. Also, only p-channel devices show significant promise (effective mobility > 0.1 cm^2/Vs), so low-power CMOS circuitry cannot be implemented in an all-organic TFT technology.

b) The quality of the deposited pentacene layer significantly affects the TFT mobility, since molecular disorder, defects and chemical impurities can form trapping states which impede carrier movement from one molecule to the next. The deposition conditions must be optimized to obtain high-quality (well-ordered) pentacene films, and high-purity source material must be used, in order to achieve high mobility and low off-state current. The use of a crystalline gate-dielectric substrate (onto which the pentacene is deposited) can provide for an improved interface, resulting in an improved subthreshold slope. The use of a self-organizing monolayer (which provides an ordered template for film deposition/growth) on the substrate also improves the interface and provides low threshold voltage as well as reasonable subthreshold swing.

<u>Problem 5</u>: Phosphors

a)

Display Parameter	**Phosphor Property of Direct Impact**
Color gamut	spectral response
Brightness	brightness saturation, efficiency
Power consumption	efficiency
Operating temperature range	thermal stability
Screen size	decay time
Lifetime	coulomb aging

b) UXGA-resolution (1600 x 1280 pixels) displays operating at a frame rate of 60 Hz:

- CRT pixel dwell time = (1/60)/(1600x1280) = **8.1 ns**.
- FED pixel dwell time = (1/60)/1280 = **13 μs**.

The pixel "duty cycle" in an FED much higher than that in CRT; this has implications for phosphor life-time as well as cathode lifetime in an FED.