

HOMEWORK ASSIGNMENT #4
Due @ 5 PM on Friday, March 19

Problem 1: Amorphous-Si TFT

Do Problem 3 at the end of the chapter entitled “Thin-Film Transistors” (Handout #20). This situation is relevant for a-Si:H TFT fabrication processes which do not employ a “top nitride” layer to protect the backside of the channel film during the n+ a-Si:H etch step, so that very thick (hundreds of nm) channel films must be used. **For part (c), assume that the gate dielectric is a 300 nm-thick layer of silicon nitride, with a relative permittivity of 7.5.**

Problem 2: Poly-Si TFT

- a) In poly-Si, “deep” trap states (energetically located near the middle of the energy bandgap) arise from dangling-bond defects predominantly located in the grain-boundary regions, whereas “tail states” arise from distorted-bond defects predominantly located within the grains. The TFT performance parameters (threshold voltage V_T , subthreshold swing S , effective mobility μ_{eff} , and leakage current I_{min}) depend upon the density-of-states (DOS) distribution within the energy bandgap. More specifically, the various parameters are strongly correlated with trap states in *certain portions* of the bandgap. Would you expect V_T and S to be correlated more strongly with the deep states or with the tail states? Would you expect μ_{eff} and I_{min} to be correlated more strongly with the deep states or with the tail states? Provide brief explanations for your answers.
- b) Given the plots of drain current activation energy for two n-channel poly-Si TFTs as follows:

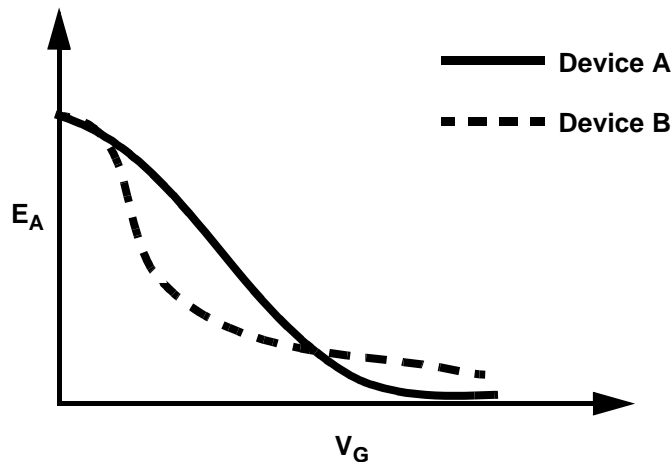


Figure P2: Drain current activation energy as a function of gate voltage, for two poly-Si TFTs.

Compare the characteristics of the two devices by filling out the table below:

Parameter	Higher in Device A or Device B?	Brief Justification
Threshold Voltage		
Deep State Density		
Tail State Density		
Integrated Defect Density		

Note: In the table above, the integrated defect density should be taken to be $\int_{E_{f0}}^{E_c} N_T(E)dE$, where E_{f0} is the Fermi level in the (undoped) channel film under zero gate bias.

Problem 3: Multiple-Gate TFT

The leakage current in a poly-Si TFT is highly dependent on V_{GS} and V_{DS} , as can be seen from the I - V characteristics shown in Figure P3a.

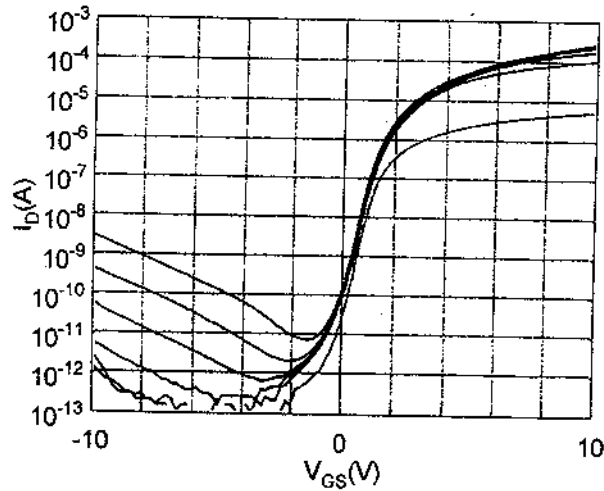


Figure P3a: Transfer characteristics of a poly-Si TFT ($W=40 \mu\text{m}$, $L=20 \mu\text{m}$; gate- SiO_2 thickness = 100 nm). V_{DS} is varied from 0.1 V to 10.1 V in 2.0 V steps.

In order to reduce the leakage current, a single transistor can be replaced with two transistors (each of channel length equal to half of that of the single transistor) in series connected to a common gate, as shown in Figure P3b.

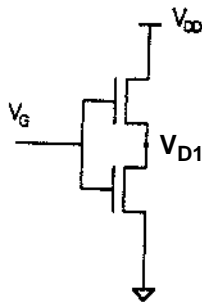


Figure P3b: Schematic diagram of two TFTs connected in series to reduce leakage current.

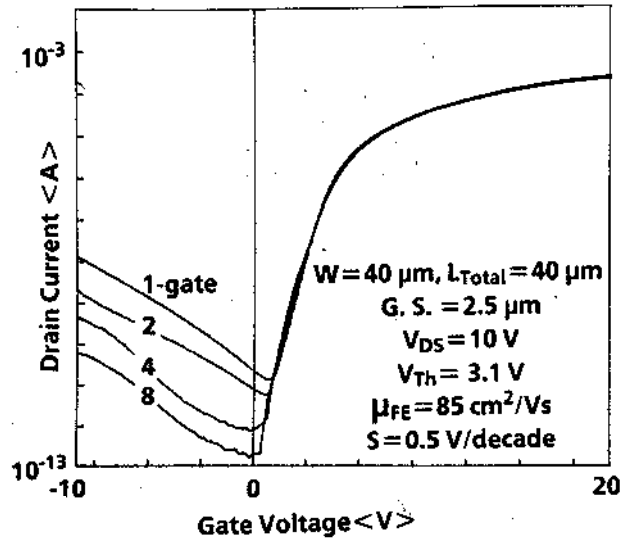


Figure P3c: Transfer characteristics of poly-Si TFTs with the same channel width and total channel length.

The I - V characteristics of poly-Si TFTs with the same channel width $W=40\ \mu\text{m}$ and total channel length $L=20\ \mu\text{m}$ are shown in Figure P3c. It can be seen that the above-threshold (ON-state) characteristics are almost identical, whereas the leakage current decreases with increasing number of gates. In a “multiple-gate” device, the peak electric field in the channel at the drain is reduced; this is why the leakage current (dominated by trap-assisted tunneling and thermionic emission from traps in the channel region near the drain) is substantially lowered. It should be noted that the individual TFTs are independent (not coupled in any way, *e.g.* by minority-carrier holes passing through common $n+$ regions from one channel to the other), and the intermediate drain voltages (*e.g.* V_{D1} in the figure above) adjust so that the drain currents of the individual transistors are equal.

- a) Consider a double-gate device comprised of two series-connected TFTs (Figure P3b), each with I - V characteristics as shown in Figure P3a. (Because there is no body contact -- and hence no “body effect” on threshold voltage to be taken into consideration -- in a TFT, the same I - V characteristics apply for each individual TFT.) The upper TFT has a V_{GS} which is more negative (because of its higher source voltage) than that of the lower transistor. Plot V_{D1} as a function of V_G for $V_{DD} = 10.1\text{V}$ and $-10\text{V} < V_G < 0\text{V}$. (For each V_{GS} and V_{DD} , only one V_{D1} can be found such that the drain currents match in the two transistors.) **Note:** You will need to extrapolate the data of Figure P3a to $V_{GS} < -10\text{V}$ to obtain the graphical solution.)

- b) For sufficiently negative gate voltages ($V_{GS} < -3\text{V}$ in Figure P3a) and large drain voltages ($V_{DS} > 1\text{V}$ in Figure P3a), the drain current is exponentially dependent on both V_{GS} and V_{DS} . We may therefore empirically approximate I_D as

$$I_D = C e^{aV_{DS} - bV_{GS}}$$

where C is an arbitrary constant, and a and b are constants which can be found from the TFT I - V characteristics. ($a = \ln 3\ \text{V}^{-1}$ and $b = \ln 2\ \text{V}^{-1}$ for the data in Figure P3a.) Derive an analytical expression for V_{D1} . Evaluate this expression and compare the result against your graphical solution in part (a).

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Problem 4: Organic TFTs

- a) What are the benefits of organic TFT technology for FPD applications as compared with Si-based TFT technologies? What are the disadvantages?
- b) Pentacene is thus far the most promising organic material for TFT application. What are the critical factors for achieving pentacene material which yields “high-performance” TFTs (field-effect mobility $> 0.5 \text{ cm}^2/\text{Vs}$, subthreshold swing $< 2 \text{ V/dec}$, threshold voltage close to 0V)?

Problem 5: Phosphors

- a) For emissive display technologies, the properties of the phosphor directly impact the performance of the display system. Indicate which properties of the phosphor impact the various display performance parameters in the table below.:

Display Parameter	Phosphor Property
Color gamut	
Brightness	
Power consumption	
Operating temperature range	
Screen size	
Lifetime	

- b) In a cathodoluminescent display, the pixel dwell time is defined to be the addressing time for an individual pixel. In a CRT, scan addressing is employed, so that the pixel dwell time $\tau = (1/f)/(m \times n)$ where f is the frame refresh rate (Hz), m is the number of columns and n is the number of rows in the display. In an FED, passive-matrix addressing is employed, so that the pixel dwell time $\tau = (1/f)/n$. Calculate the pixel dwell times for a UXGA-resolution CRT and a UXGA-resolution FED.

Current Conduction in Poly-Si

A. Grain-boundary barrier height

As derived in Lecture #12, the height E_B of the energy barrier which exists at the grain boundary in an idealized poly-Si film (with average grain size L_g and grain-boundary trap-state density D_t) is given by

$$qE_B = \frac{qN_D L_g^2}{8\epsilon_s}$$

if the doping concentration N_D is less than D_t/L_g , and

$$qE_B = \frac{qD_t^2}{8\epsilon_s N_D}$$

if the doping concentration N_D is greater than D_t/L_g . Note that in the derivation, not only is the poly-Si film assumed to consist of defect-free grains of uniform size (L_g), separated by grain boundaries of infinitesimally small lateral dimensions and fixed areal trap-state density (D_t), but also the grain-boundary trap states are assumed to be energetically located at the middle of the Si energy bandgap.

B. Conductivity of a poly-Si film

Carrier transport in a poly-Si film is limited by thermionic emission of carriers over the grain-boundary energy barriers, so that the average conductivity of a poly-Si film is exponentially dependent on the barrier height:

$$\sigma \propto \exp\left(-\frac{E_B}{kT}\right)$$

At low doping concentrations, the carriers which are contributed by the dopants (in addition to intrinsic carriers) are mostly trapped in the grain boundaries and hence the poly-Si resistivity is extremely high. As the doping concentration increases beyond D_t/L_g , the average mobile carrier concentration increases and, at the same time, the energy barrier height decreases. This is why the resistivity of poly-Si decreases so rapidly at moderate doping concentrations (10^{16} - 10^{18} cm⁻³). An “effective mobility” μ_{eff} of carriers in poly-Si can be defined as

$$\mu_{eff} = \mu_0 \exp\left(-\frac{E_B}{kT}\right)$$

where μ_0 is the carrier mobility within the (crystalline) grain. Note that μ_{eff} is a mobility in the sense that it describes the ease of carrier motion from one grain to another in the polycrystalline material. It is not the familiar microscopic mobility related to isolated scattering centers in a homogeneous piece of semiconductor.

C. I-V characteristic of a poly-Si TFT

Adapting this simple one-dimensional model of conduction to the case of an n-channel poly-Si thin-film transistor (TFT), we can write the following expression for TFT drain current I_D :

$$I_D \propto n \exp\left(-\frac{E_B}{kT}\right) = n \exp\left(-\frac{qD_t^2}{8\epsilon_s n_0 kT}\right)$$

where n_0 is the total (free + trapped) carrier density at the channel surface and n is the free-carrier (areal) density. J. Levinson *et al.* [*Journal of Applied Physics*, Vol. 53, p. 1993, 1982] approximated n_0 to be equal to $nt_s = C_{ox}(V_G - V_T)t_s$, where C_{ox} is the areal gate-oxide capacitance, V_G is the gate voltage, V_T is the threshold voltage, and t_s is the thickness of the TFT channel film. Under this approximation, the effective grain-boundary trap-state density can be determined from a plot of $\ln(\delta I_D / \delta V_G)$ vs. $1/V_G$ for low drain bias V_D (such that there is negligible distortion of the energy bands in the direction parallel to carrier conduction) -- the so-called “**Levinson’s method.**”

From the gradual channel approximation, $n = C_{ox}(V_G - V_T - \frac{V_D}{2})$ so that the TFT drain current can be expressed as

$$I_D = \frac{W}{L} \mu_n C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) V_D \exp\left(-\frac{E_B}{kT}\right) = \frac{W}{L} \mu_{neff} C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) V_D$$

where W and L are the channel width and length, respectively, and μ_n is the electron mobility within the grain. Since E_B decreases with increasing n (and hence with increasing V_G), **the effective carrier mobility in a poly-Si TFT increases with gate voltage.** (μ_{eff} will eventually begin to decrease with increasing gate voltage, at high gate voltages, when the effect of the increasing vertical electric field becomes dominant.)

Qualitatively, this conduction behavior is similar to that of a spatially uniform, defective material. (The number of free carriers which can contribute to conduction increases as defect-associated trap states become filled.) Therefore, for the purposes of modelling poly-Si TFT I - V characteristics, it is sufficient to treat the poly-Si channel material as a uniform “effective medium.” The trap density used in the model should be of the order of D_t/L_g . The effective medium approach can be used to model the TFT threshold voltage also.

From the boxed equation above, it can be seen that TFT drain current should exhibit a strong dependence on temperature, due to the exponential factor. (The carrier mobility μ_n changes with temperature -- generally decreasing with increasing temperature near room temperature -- but this effect is far weaker than that due to the grain-boundary barrier.) An “activation energy” (equivalent to E_B , for $V_G > V_T$), which varies with gate voltage, can thus be extracted from measurements of I_D vs. V_G at several (at least 2) temperatures.