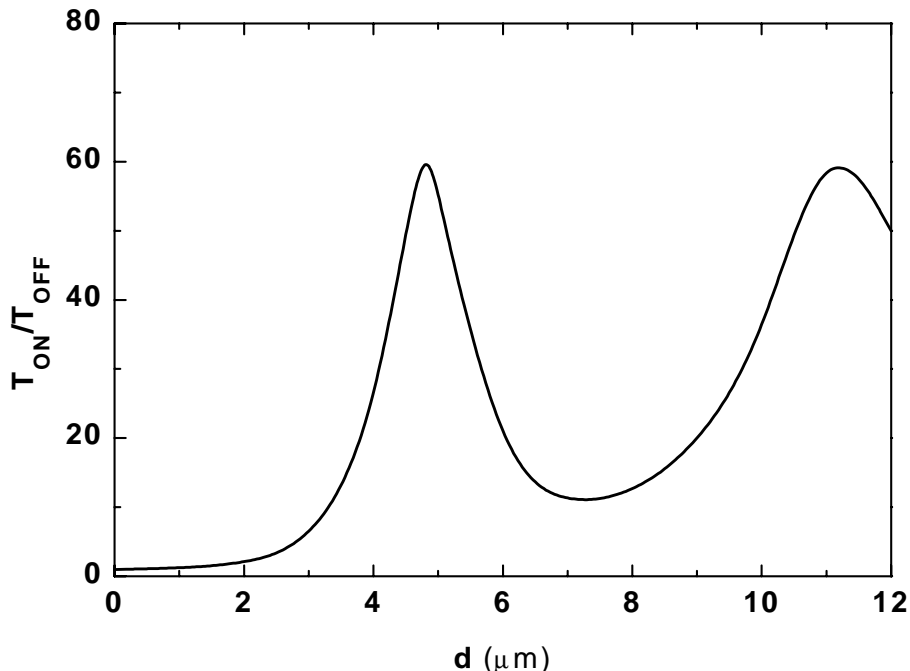


HOMEWORK ASSIGNMENT #3 SOLUTIONS

Problem 1:

- a) In order for a TN-LCD to operate as a 90° rotator, $\Gamma(\lambda) = ((\Delta n d / \lambda)^2 + 0.25)^{0.5}$ must be an integer value. In active-matrix displays, the cell gap d is chosen such that $\Gamma(\lambda_0) = 1$ where $\lambda_0 = 550$ nm. In this case, $d = \lambda(1-0.25)^{0.5} / \Delta n = 4.76$ μm .
- b) In a normally-black TN-LCD, the polarization directions of the polarizers are parallel, so that light passes through the cell when the LC twist is destroyed by application of an electric field. From Figure 4 of Handout #19, we can infer (from the transmittance values for zero cell gap) that the transmittances of Red, Green, and Blue in the ON (driven) state are each equal to 1, so that $T_{\text{ON}} = 3$. T_{OFF} is found by adding the three transmittances. The resulting display contrast ratio $T_{\text{ON}}/T_{\text{OFF}}$ is plotted below.



- c) From part (b), it is clear that the **contrast ratio is a very sensitive function of cell gap** for a normally-black TN-LCD. In addition, **small variations in T_{OFF} resulting from slight misalignment of the polarizers also translate into large variations in contrast ratio**. These characteristics are undesirable because of the tighter tolerances required in manufacturing.

Problem 2:

- a) Full-color images can be rendered **either by stacking reflective LC displays** (each of which reflects one of Red, Green, Blue wavelengths) **or by employing a mosaic color filter in front of a single (white-reflective) LC display**. **The stacking method results in a brighter display**, but is more expensive to implement (3X LCD cost). **The color filter method is less costly**, but results in lower display brightness (~3X lower brightness, since at least 2/3 of the light is filtered out at each sub-pixel).
- b) Bistable LCDs do not require standby power to maintain an image; their main advantage is **ultra-low-power operation**. Because of their bistable characteristics, they have **no inherent analog greyscale**

capability. Greyscale images must be achieved by spatial or temporal dithering (sequential modulation), which require higher sub-pixel density or higher data and LC switching rates, respectively.

Problem 3:

a) Representative parameter values are provided in the table below.:

Parameter	PMLCD	>, <, or =	AMLCD	Brief Justification
Contrast Ratio	15:1	<	100:1	Pixels are electrically isolated from each other and hence can be independently addressed in an AMLCD, so that they can be driven from the fully OFF state to the fully ON state (<i>i.e.</i> the $\langle V_{on} \rangle_{rms} / \langle V_{off} \rangle_{rms}$ ratio is not dictated by the Alt-Pleshko “iron law”).
Viewing Angle (CR>5)	H: +/-30° V: +/-25°	<	H: +/-60° V: +45°, -30°	Because of the higher degree of LC twist in a STN-LCD, changes in the midlayer LC tilt angle with viewing angle will be larger, so that the viewing cone (for a given minimum contrast ratio) will be more restricted.
Response Time	100 ms	>	30 ms	In PMLCDs which employ standard multiplexed addressing (as opposed to active addressing), the LC must respond to the rms voltage averaged over a frame time in order to avoid the “frame response” problem and hence it generally has a longer response time. Faster responding LC material can be employed in AMLCDs, since the pixel voltage is held constant over a frame time.
# Gray Levels	16	<	256	The electro-optic characteristics of a STN-LCD are much steeper, and the rms drive voltage is limited to a small range due to the Alt-Pleshko “iron law.” Thus, it is much more difficult to achieve many bits of gray scale in a PMLCD.
Aperture Ratio		>		In an AMLCD, the pixel-switching element occupies some area in the pixel which must be made opaque (to shield the active device from light). This reduces the active area of the pixel.
Cost		<		Active-matrix fabrication involves a complicated, expensive process (in comparison with passive-matrix stripe-electrode fabrication). In addition, column driver ICs are generally more expensive for AMLCDs because of the many output voltage levels required.

b) Over the period of a frame time (16.7 ms), the LC must not leak an amount of charge which is enough to change the pixel voltage by more than 20 mV. This amount of charge is equal to $20 \text{ mV} \times C_{\text{pixel}} = 2 \times 10^{14} \text{ C}$. This means that the LC leakage current cannot exceed $2 \times 10^{14} \text{ C} / 16.7 \text{ ms} = 1.2 \text{ pA}$. Assuming a typical maximum LC voltage of 5 V, the resistance of the LC must exceed $5 \text{ V} / 1.2 \text{ pA} = 4.2 \times 10^{12} \Omega$. The mini-

imum required LC resistivity is $(4.2 \times 10^{12} \Omega)(6 \times 10^{-4} \text{ cm}^2)/(5 \times 10^{-4} \text{ cm}) = \mathbf{5 \times 10^{12} \Omega\text{-cm}}$.

Problem 4:

- a) In a video-rate (60 Hz refresh rate) VGA (640 x 480 pixels) display, the line time is $16.7 \text{ ms}/480 = 35 \mu\text{s}$. Thus, the $R_{\text{ON}}C_{\text{pixel}}$ time constant associated with the pixel should be less than $3.5 \mu\text{s}$. For $C_{\text{pixel}} = 1 \text{ pF}$, this means that R_{ON} must be less than $3.5 \text{ M}\Omega$. The resistance of the TFT in the ON state can be approximated as given by Equation (4) from the paper entitled “Transistor sizing for AMLCD integrated TFT drive circuits” (Handout #25). From this equation, the minimum W/L ratio is $(2/\mu_{\text{eff}})/[(C_{\text{ox}})(V_{\text{GS}} - V_{\text{T}})(R_{\text{ONmax}})] = (2/0.7)/[(2.5 \times 10^{-8})(20-2.5)(3.5 \times 10^6)] = \mathbf{1.87}$.
- b) For a poly-Si TFT with gate SiO_2 thickness 100 nm, $C_{\text{ox}} = (3.9)(8.854 \times 10^{-14})/(100 \times 10^{-7}) = 3.45 \times 10^{-8} \text{ F/cm}^2$. The minimum W/L ratio is $(2/\mu_{\text{eff}})/[(C_{\text{ox}})(V_{\text{GS}} - V_{\text{T}})(R_{\text{ONmax}})] = (2/50)/[(3.45 \times 10^{-8})(20-2)(3.5 \times 10^6)] = \mathbf{0.018}$ -- 100 times smaller than that required for an a-Si TFT. Thus, a poly-Si TFT-AMLCD will have a larger aperture ratio than an a-Si TFT-AMLCD, for a given display size and resolution.
- c) From Figure 3 in the paper entitled “Transistor sizing for AMLCD integrated TFT drive circuits” (Handout #25), the required TFT ON-resistance is $18 \text{ k}\Omega$. The required W/L ratio is $(2/\mu_{\text{eff}})/[(C_{\text{ox}})(V_{\text{GS}} - V_{\text{T}})(R_{\text{ON}})] = (2/50)/[(3.45 \times 10^{-8})(20-2)(18,000)] = \mathbf{3.6}$ (very reasonable!). Scan-line driver circuitry can be easily implemented “on-board” using poly-Si TFTs.