UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE290D — Handout #24
Spring 1999 — T.-J. King

HOMEWORK ASSIGNMENT #3
Due Thursday, March 11 (in class)

Problem 1: Liquid-Crystal Cell Design

a) Calculate the optimum cell gap (d) for an active-matrix TN-LCD employing a liquid crystal material with $\Delta n=0.1$. (Use $\lambda_o=550$ nm.)

b) Consider the transmittance characteristics of a normally-black TN-LCD shown in Figure 4 of Handout #19. Plot the display contrast ratio (T_{ON}/T_{OFF}) as a function of cell gap, for $0 < d < 12$ μm. You should assume that the transmission (T) of the display is equal to the sum of the Red, Green, and Blue transmissions.

c) Why is the normally-white mode used in almost all commercial AMLCDs?

Problem 2: Reflective LCD Technology

a) What are the two methods by which full-color images can be rendered with reflective LC displays? What is the advantage of each method?

b) What is the main advantage of bistable LCDs? What is the main disadvantage of bistable LCDs?

Problem 3: Active Matrix vs. Passive Matrix LCDs

a) Compare the characteristics of a passive-matrix STN-LCD against those of an active-matrix TN-LCD, by filling out the 3rd and 5th columns in the following table:

Parameter	PMLCD	>, <, or =	AMLCD	Brief Justification
Contrast Ratio				
Viewing Angle				
Response Time				
# Gray Levels				
Aperture Ratio				
Cost				

b) In an active-matrix LCD, the liquid-crystal material must have very high resistivity in order for grayscale images to be displayed. Calculate the minimum required LC resistivity for an SVGA display (60 Hz frame rate) with a cell gap of 5 μm, a pixel ITO area of $6x10^4$ μm^2, a pixel capacitance ($C_{LC} + C_{storage}$) of 1 pF, if the maximum allowable change in pixel voltage during a frame time is 20 mV.

Problem 4: TFT sizing in AMLCDs

A pixel TFT in an active-matrix circuit operates in the linear region. Pixels are usually addressed using a scan-line voltage of 20V (to sequentially turn on each row of TFTs, and a pixel TFT is usually sized to allow the pixel capacitance to be charged to the data-line voltage within one-tenth of the line time. The maximum difference in pixel voltage from frame to frame is 10 V (corresponding to a fully driven pixel).

a) Typical amorphous-Si TFT performance parameters are μ_{eff}=0.7 cm^2/Vs and V_T=2.5V. **Estimate** the minimum W/L ratio required for an a-Si pixel TFT in a video-rate VGA display. (Assume gate-dielectric areal capacitance = $2.5x10^{-8}$ F/cm^2, and pixel capacitance = 1 pF.)

b) Typical "low-temperature" poly-Si n-channel TFT performance parameters are μ_{eff}=50 cm^2/Vs and V_T=2.0V. **Estimate** the minimum W/L ratio required for a poly-Si pixel TFT in a video-rate VGA display. (Assume gate SiO_2 thickness = 100 nm, and pixel capacitance = 1 pF.)

c) Following the methodology described in the paper entitled "Transistor sizing for AMLCD integrated TFT drive circuits" (Handout #25), estimate the W/L ratio required for a poly-Si buffer TFT of a single-ended scan-line driver for a video-rate VGA display.