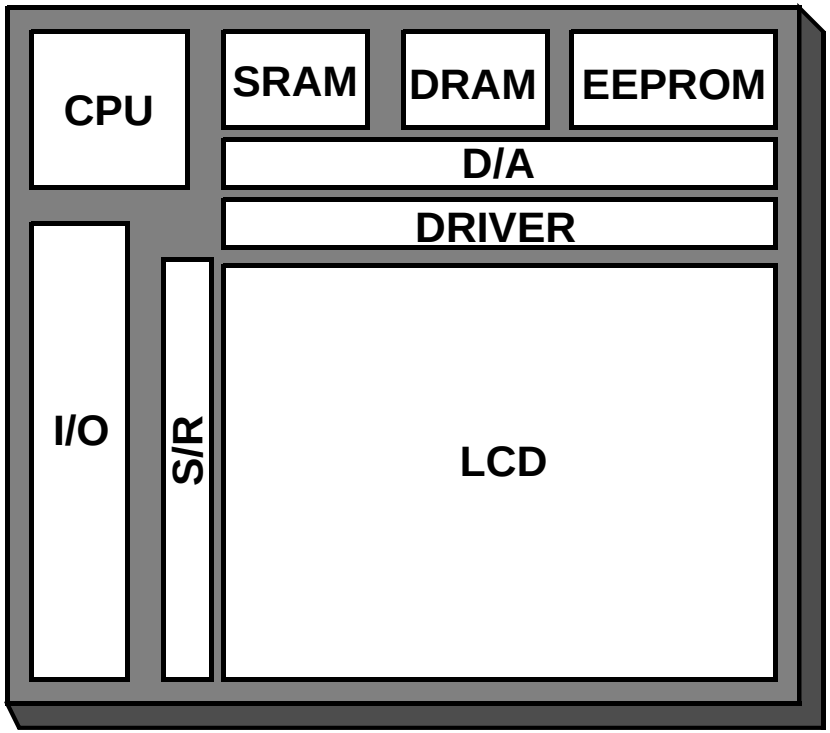
LSI ON GLASS SUBSTRATES

OUTLINE

- Introduction: Why “System on Glass”?
- MOSFET Technology
- Low-Temperature Poly-Si TFT Technology
- System-on-Glass Technology Issues
- Conclusion

System on Glass



COMPONENTS:
- signal-processing/computation
- data storage
- communication
- human-machine interface

ADVANTAGES:
- compact
- lightweight
- higher performance (?)
- lower cost (?)

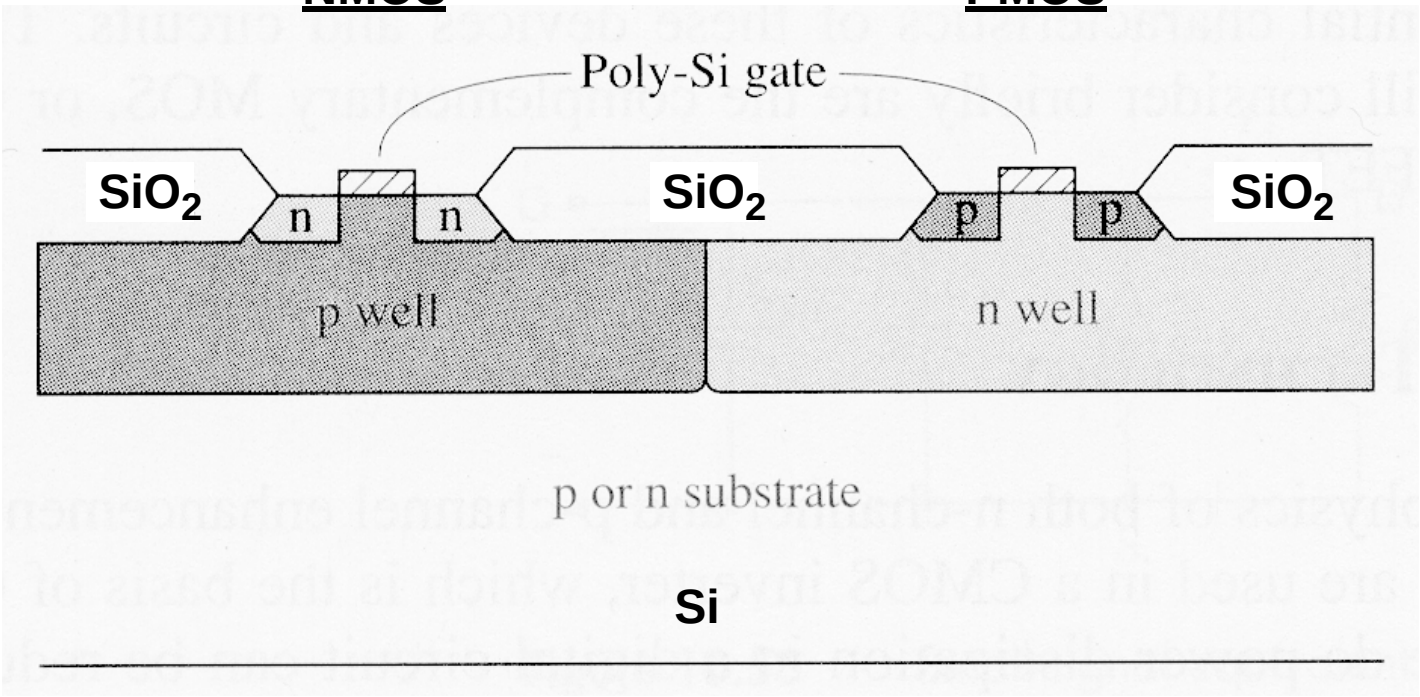
POTENTIAL APPLICATION: Electronic Books

Substrate Comparison: Glass vs. Si

PROPERTY:	GLASS* SHEET	SILICON WAFER
OPTICAL TRANSPARENCY	transparent	opaque
THERMAL CONDUCTIVITY	< 0.001 W/cm/K	1.5 W/cm/K
ELECTRICAL CONDUCTIVITY	insulator	semiconductor
CRYSTALLINITY	amorphous	monocrystalline
MAXIMUM TEMPERATURE	~500^{o}C	1100^{o}C

*** non-alkali borosilicate or aluminosilicate glass**

MOSFET Technology

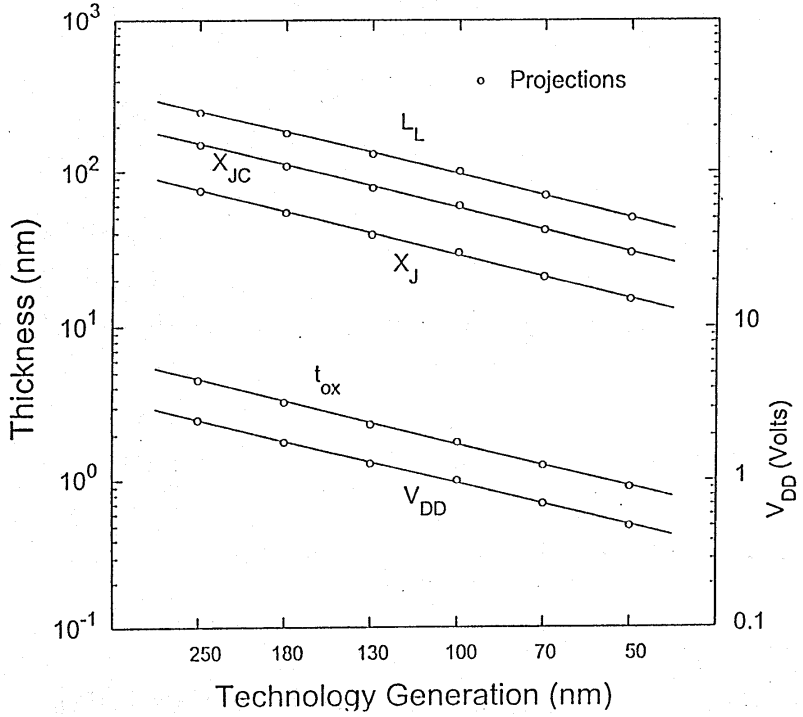


- ☹ **Separate “well” regions required**
- ☹ **Complicated device isolation process**
- ☺ **V_T adjustment by ion implantation**
- ☺ **Thin, high-quality gate SiO_2**

MOSFET Technology Scaling

MOSFET size reductions => improved performance, reduced cost

SIA National Technology Roadmap for Semiconductors



Constant E-field scaling:

=> reductions in

- power-supply voltage
- gate-dielectric thickness
- S/D junction depth

MOSFET Technology: State of the Art

Minimum channel length (drawn)**: 0.25 μm**
Gate-SiO_2 thickness: 5 nm

Power-supply voltage: 2.5 V

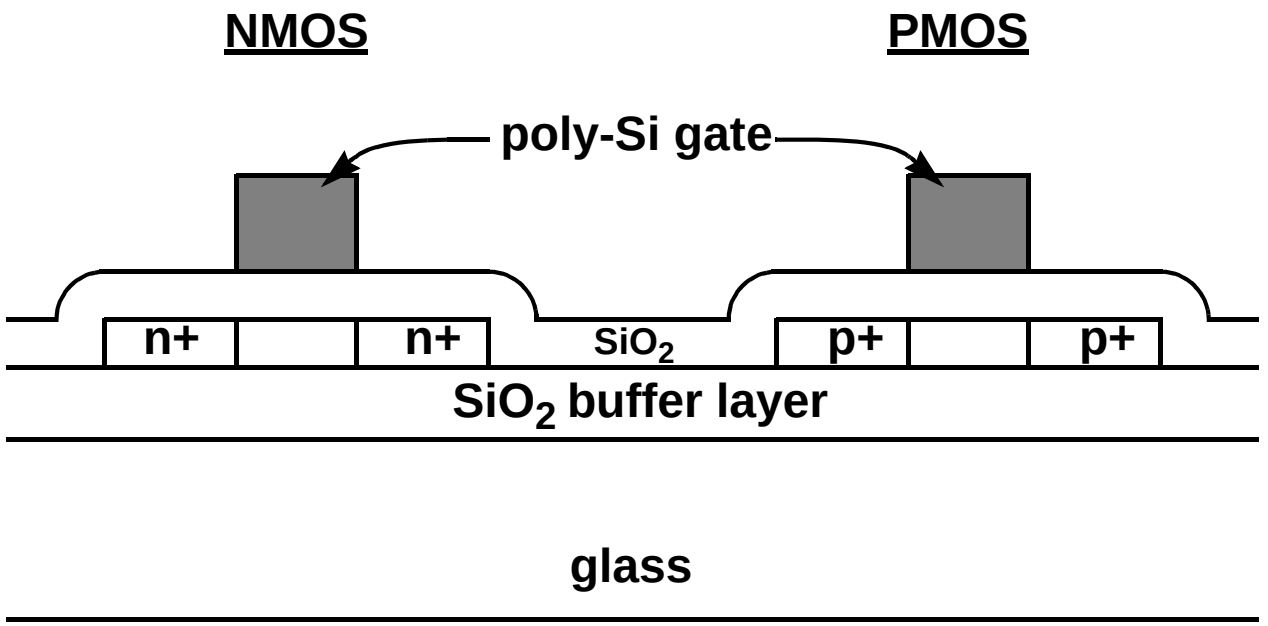
Drive current: > 600 μA/μm
Leakage current: < 1 nA/μm

CV/I circuit-delay metric: < 20 ps

<u>Key factors for performance</u>:

- **High-purity, monocrystalline channel material**
- **High-quality gate-SiO_2 (bulk and interface)**
- **Low-resistance S/D contacts**

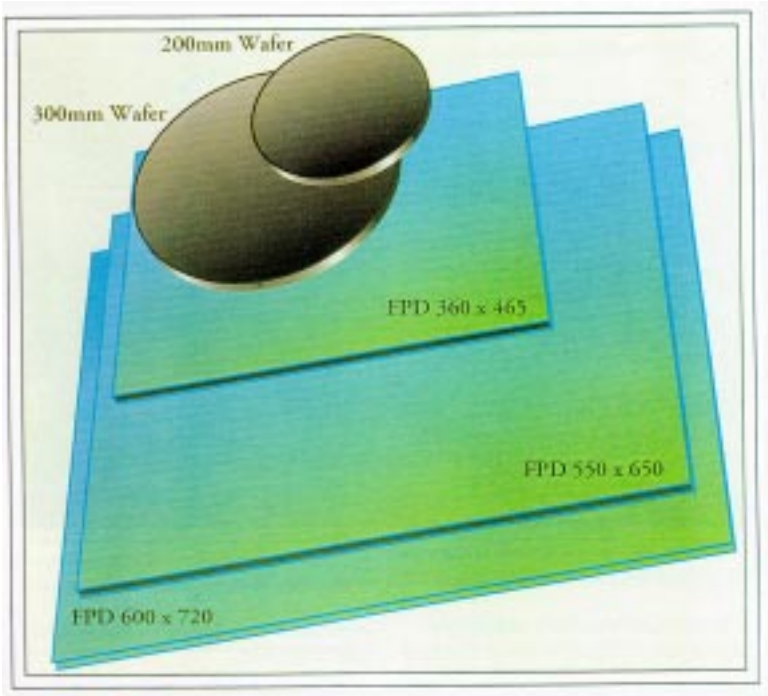
Low-Temperature Poly-Si TFT Technology



- ☺ Simple device isolation process
- ☹ Impurities & defects in channel film
- ☹ V_T adjustment (channel doping) difficult
  => severe short-channel effects
- ☹ Deposited gate SiO_2
  => inferior device performance

Poly-Si TFT Technology Scaling

Substrate size increases => reduced cost



TREND IN GLASS SUBSTRATE SIZE:

- **increase area**
  - 360 mm x 465 mm
    - 550 mm x 650 mm
      - 650 mm x 830 mm
- **decrease thickness**
  - 1.1 mm
    - 0.7 mm
      - 0.5 mm

-> No scaling of TFT dimensions for improved performance!

LT Poly-Si TFT Technology: State of the Art

Minimum channel length (drawn)**: 2 μm**
Gate-SiO_2 thickness: 100 nm

Power-supply voltage: 20 V

Drive current: > 10 μA/μm
Leakage current: < 1 nA/μm

CV/I circuit-delay metric: > 1 ns

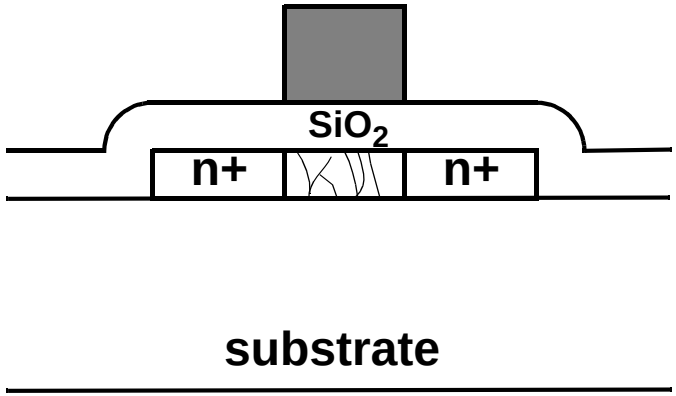
<u>Key contributors to inferior performance</u>:

- **Defects in channel region**
- **Inferior-quality gate-SiO_2**
- **Larger transistor dimensions**

System on Glass Technology Issues

ISSUE #1: TFT performance variation

- due to statistical variation in number, size, and location of grain boundaries in the channel:



- increases as TFT size is reduced

- problematic for circuit design

System on Glass Technology Issues (II)

ISSUE #2: High power consumption of TFT circuitry

- more problematic because glass is a poor thermal conductor

=> need to reduce power-supply voltage for non-display-related circuitry

- but high V_T limits TFT drive current

=> employ thinner gate-SiO_2 in these areas (added process complexity)

System on Glass Technology Issues (III)

ISSUE #3: Low manufacturing yield

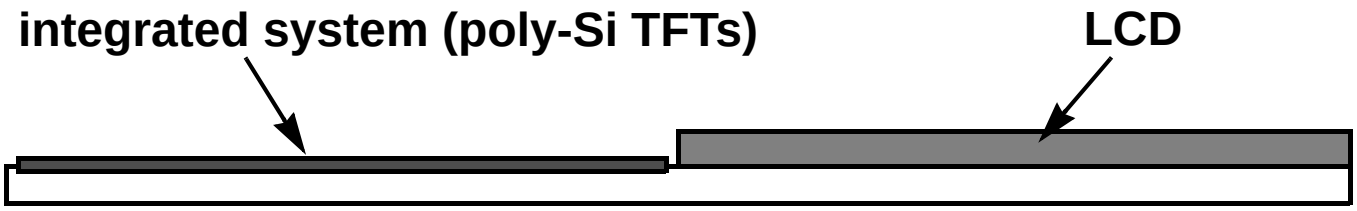
high degree of integration:

=> large critical area for defects

=> reduced yield

=> higher manufacturing cost

Chip-in-Glass Technology



System on Glass Technology

Chip-on-Glass Technology:

Near-term solution for

- **lower cost**
- **higher performance**
- **compact and lightweight systems**

CONCLUSION

- Poly-Si can provide System-on-Glass capability
- Important differences between MOSFETs & TFTs

-> Difficult to implement high-performance circuitry in poly-Si with high yield

=> Hybrid integration is best approach