Lecture #9: Active-Matrix LCDs

OUTLINE

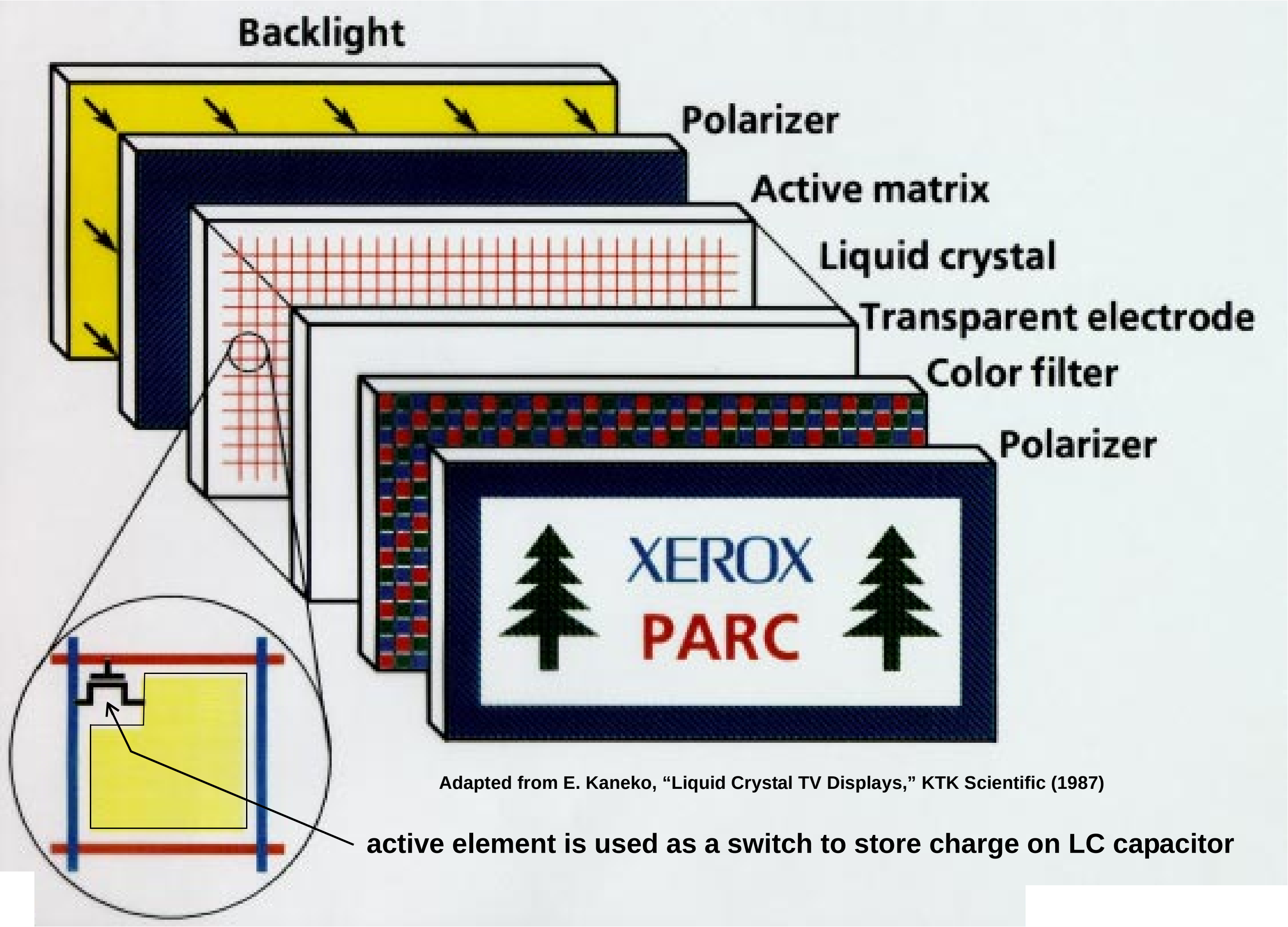
- **Introduction**
  - Active-matrix switching elements
  - TFT performance requirements
  - Active matrix processing constraints

- **Amorphous silicon (a-Si) TFT technology**
  - TFT fabrication process
  - Development trends and future requirements

- **Polycrystalline silicon (poly-Si) TFT technology**
  - TFT fabrication process
  - Development trends and future requirements

- **Summary**

Components of a TFT-AMLCD

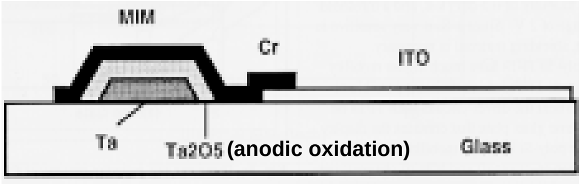


Adapted from E. Kaneko, “Liquid Crystal TV Displays,” KTK Scientific (1987)

active element is used as a switch to store charge on LC capacitor

Switching Elements for Active Matrices

- **Diodes**
  - **Metal-Insulator-Metal (MIM)**
  - **Amorphous Si**



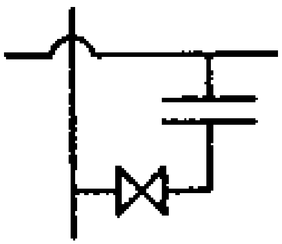
- **Transistors**
  - **MOSFET**
  - **Thin-Film Transistor (TFT)**
    - **CdSe**
    - **Amorphous Si**
    - **Polycrystalline Si**
    - **Single-crystal Si**

- **CdSe TFT (T. P. Brody *et al.*, 1973) - first**

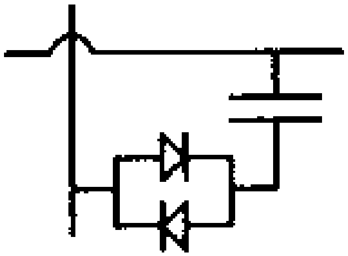
- **MIM**
  - ☺ **simpler fabrication process -> lower cost**
  - ☺ **excellent electrical properties, uniformity**
  - ☹ **parasitic capacitance -> capacitive voltage divider effect**
  - ☹ **asymmetrical current characteristic -> image retention problem**

- **a-Si TFT (P. G. LeComber *et al.*, late 1970's) - primarily used in AMLCDs today**
  - ☺ **stability advantage compared to CdSe**
  - ☺ **cost advantage compared to poly-Si, X-Si**

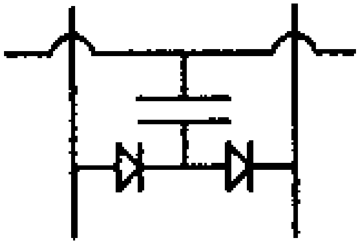
Two-Terminal Devices for AMLCDs



MIM



a-Si pin

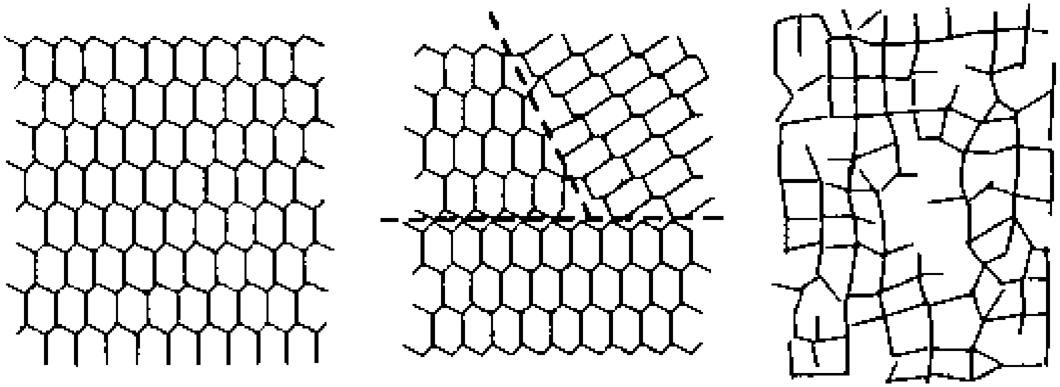


D^2R

- Simpler fabrication (MIM : 3 mask process)
- No cross-overs

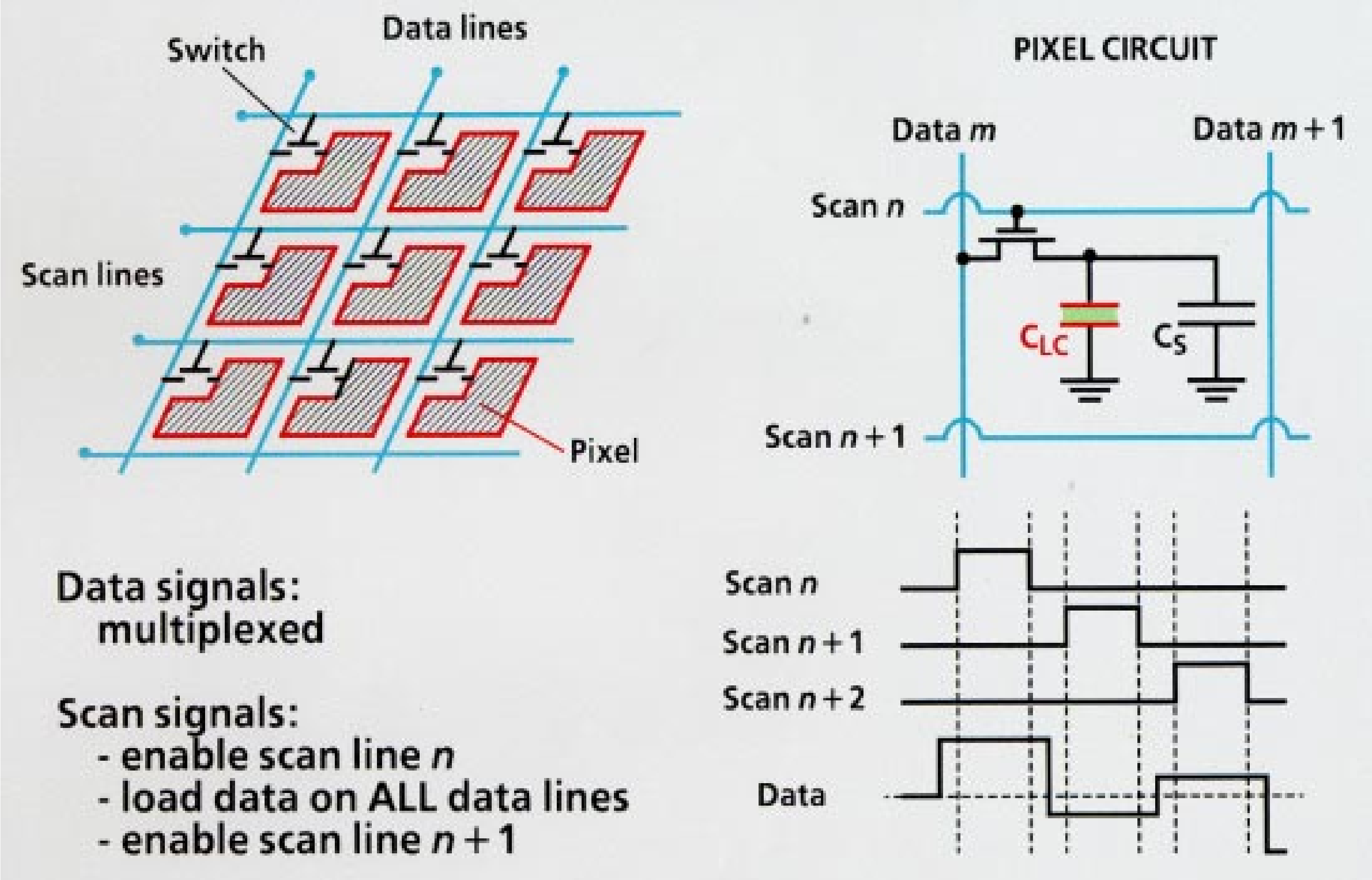
- Uniformity of diode characteristics
- No storage capacitors
- Patterning of backplane ITO required

What is Amorphous Silicon?



	c-Si	p-Si	a-Si
Mobility (Speed/Current)	500	50	0.5
Process Temp	>900C	600-900C	250-350C
Substrate	Single Crystal Si 4" - 8"	Quartz/Glass 4" - 8"	Glass 14" x 18". . .

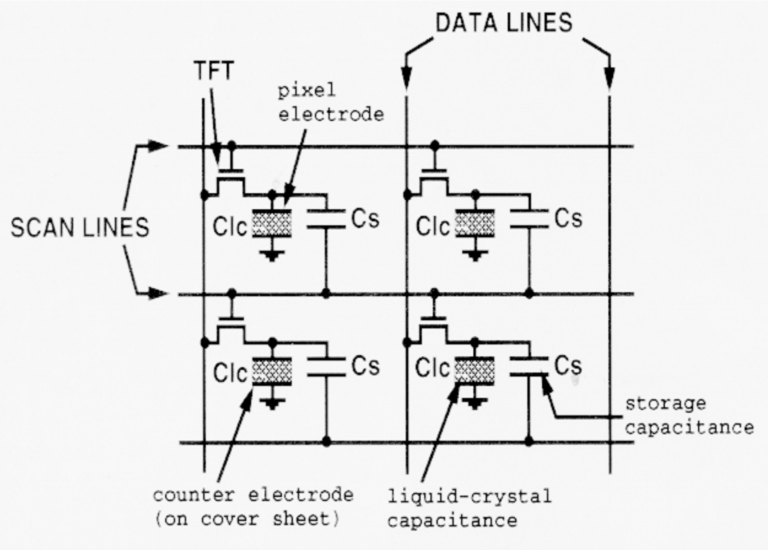
TFT Active Matrix Operation



Data signals:
multiplexed

Scan signals:
- enable scan line *n*
- load data on ALL data lines
- enable scan line *n* + 1

Pixel TFT Performance Requirements



- **Ability to deliver +/- 5 Volts to pixel**

  -> V_{DS} **= 10 V**

  V_{GS} **= 20 to 30 V**

- **Performance (gray-scale AMLCDs):**

  ΔV_{pixel} **= 20 mV** (frame time τ = 16 ms)

$$I_{leakage} < \frac{C_{pixel}\Delta V_{pixel}}{\tau}$$

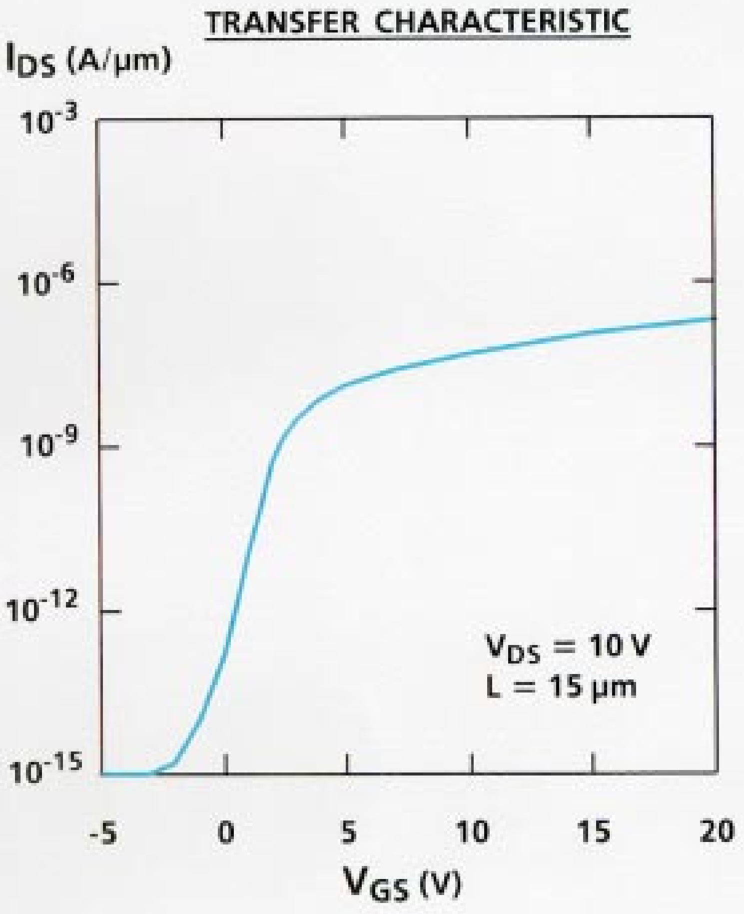
	VGA	EWS
charge (line time)	32 µs	13 µs
pixel capacitance	1 pF	0.5 pF
drive current	~1 µA	~1 µA
leakage current	< 1 pA	< 0.5 pA

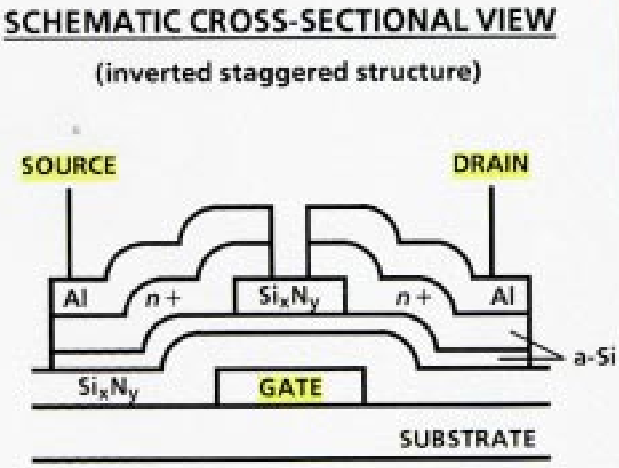
Substrate Comparison: Glass vs. Si

PROPERTY:	GLASS* SHEET	SILICON WAFER
OPTICAL	transparent	opaque
ELECTRICAL CONDUCTIVITY	insulator	semiconductor
THERMAL CONDUCTIVITY	< 0.001 W/cm/K	1.5 W/cm/K
MAXIMUM TEMPERATURE	~500°C	1100°C

* non-alkali borosilicate or aluminosilicate glass

Amorphous-Si Thin-Film Transistor


TRANSFER CHARACTERISTIC


SCHEMATIC CROSS-SECTIONAL VIEW

(inverted staggered structure)

A-Si TFT Fabrication Process (I)

Gate metal deposition (RF sputter)

Gate mask

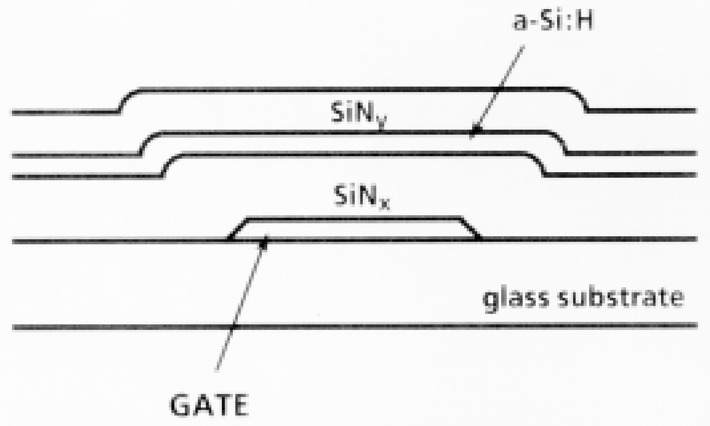
Gate metal etch (wet)

“NSN” deposition (PECVD)

- **gate nitride deposition**
  gases: NH_3, SiH_4 (N_2 or He dilution)
  temperature: 300-350^{o}C
  thickness: ~300 nm
  rate: ~120 nm/min for in-line system
  ~200 nm/min for cluster tool

- **a-Si:H deposition**
  gases: SiH_4, H_2
  temperature: 250-300^{o}C
  thickness: 50 nm
  rate: ~25 nm/min for in-line system
  ~100 nm/min for cluster tool

- **top nitride deposition**
  gases: NH_3, SiH_4, (N_2 or He dilution)
  temperature: 250^{o}C
  thickness: ~150 nm

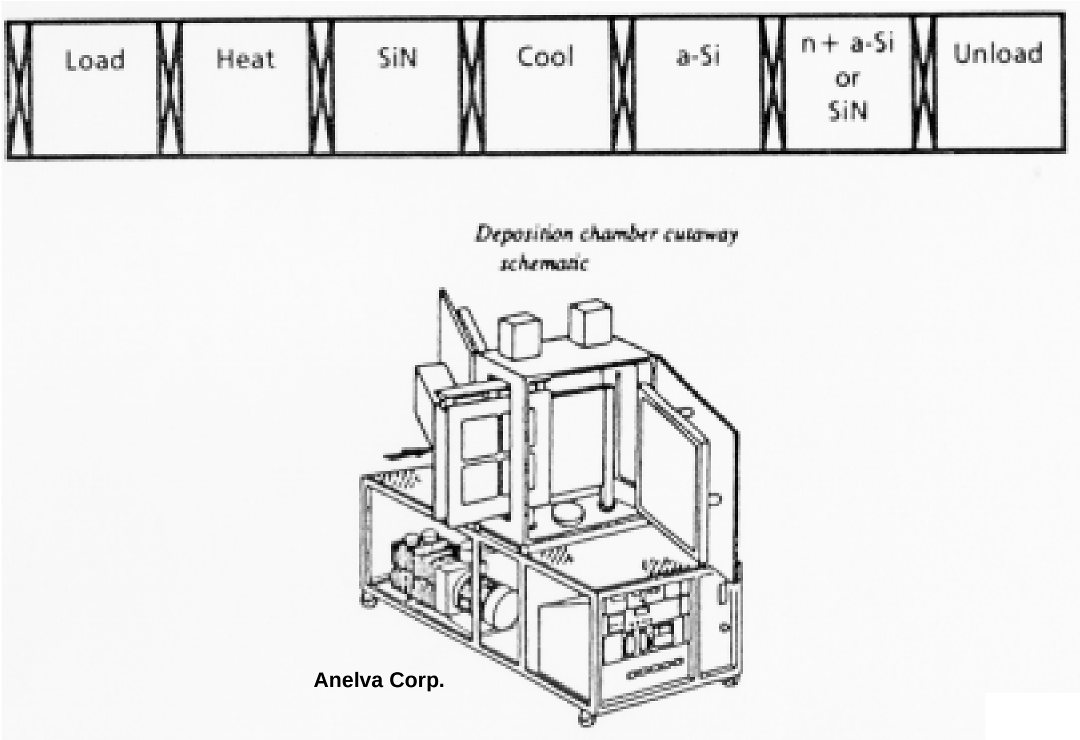


Schematic cross-sectional view of a-Si TFT structure after NSN deposition

PECVD Systems for Large-Area Substrates (I)

IN-LINE SYSTEM:

- historical -- solar battery a-Si deposition (Japan)
- low throughput (< 10 plates/hour)
- slow CF_4+O_2 in-situ dry cleaning
- large clean-room footprint

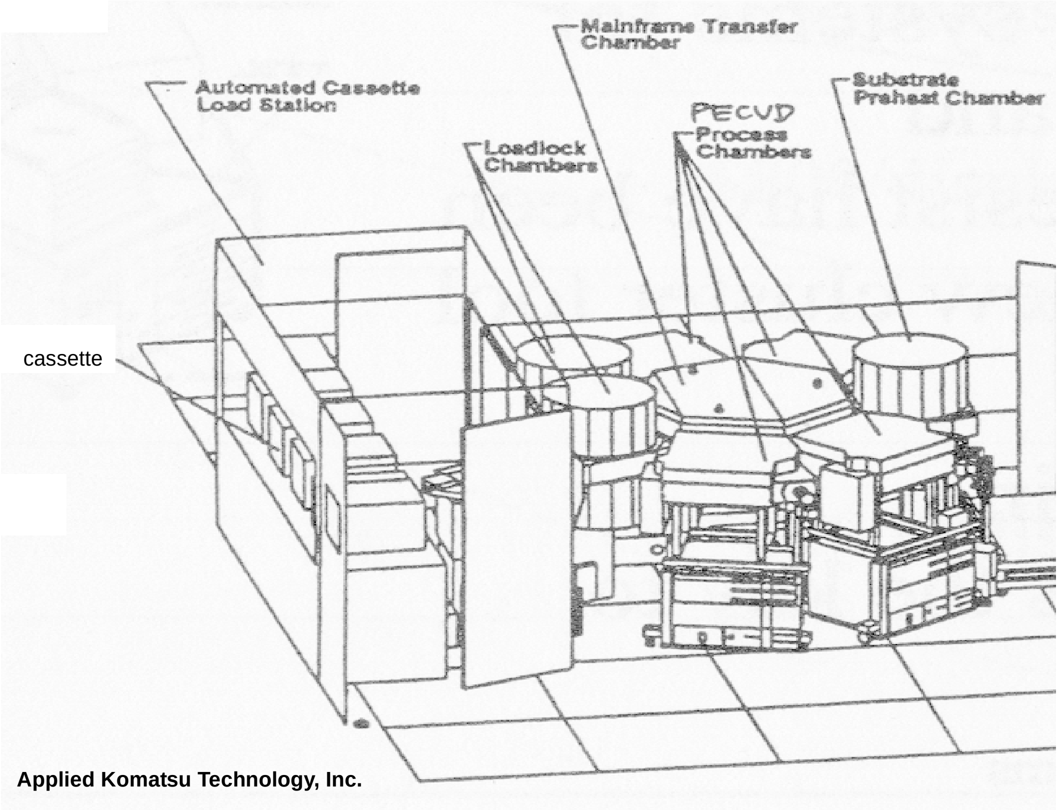


Anelva Corp.

PECVD Systems for Large-Area Substrates (II)

CLUSTER TOOL (e.g. AKT-1600):

- single-substrate processing units (reduced thermal mass)
- designed for higher throughput (30 plates/hour) and easier maintenance
- fast NF_3-based in-situ dry cleaning
- can be installed through-the-wall (bulkheaded)



Applied Komatsu Technology, Inc.

PECVD Systems for Large-Area Substrates (III)

PROCESS ISSUES:

- **Deposition uniformity**
  - **- presently sufficient** (better than +/- 7%)

- **Throughput**
  - **Major challenge** (need > 60 plates/hour)
    - **-> increase film-deposition rates**
    - **-> improve robot handling speed**

- **Yield loss:**
  - **particles** --> improvements in gas-flow, in-situ cleaning
  - **electrostatic discharge** --> improvements in design
  - **breakage** --> improvements in robot handling

Large-Area Processing

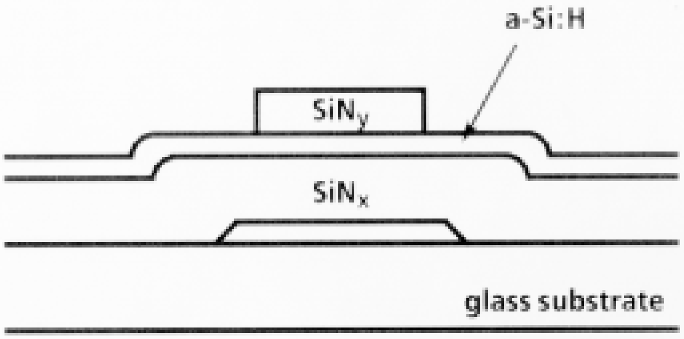
PHOTOLITHOGRAPHY:

- **Stepper exposure systems**
  - ~10 cm diameter field
  - < 1 μm stitching accuracy
  - ~2 μm resolution
  - > 60 plates/hour throughput
- **Integrated "track" systems for coating, baking, and developing photoresist**
- **Defect control is key to higher yields**

SPUTTER DEPOSITION (for metals, ITO):

- **In-line systems are most widely used**
- **New cluster tools allow floorspace reduction, greater process flexibility**
- **Improved heating uniformity is required, especially for achieving uniformly low ITO resistivity**

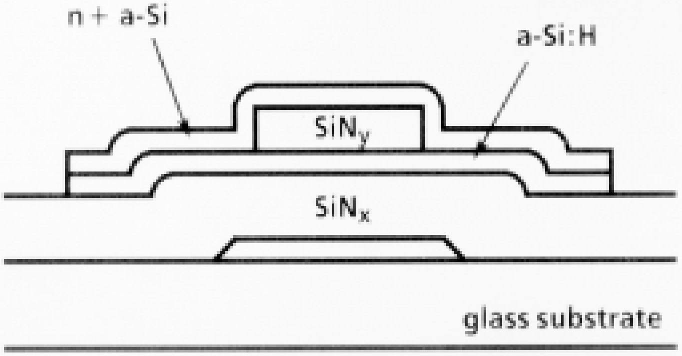
A-Si TFT Fabrication Process (II)



Schematic cross-sectional view of
a-Si TFT structure after top nitride etch

Backside flood exposure

Top nitride etch (wet)



Schematic cross-sectional view of
a-Si TFT structure after n + etch

n+ a-Si:H deposition (PECVD)

gases: SiH_4, PH_3, H_2
temperature: < 250^oC
thickness: 100 nm
rate: ~25 nm/min for in-line system
~200 nm/min for cluster tool

n+ mask

a-Si etch (RIE)

gases: SF_6, $CFCl_3$
pressure: 100 mT
rate: 100 nm/min

A-Si TFT Fabrication Process (III)

S/D metal deposition (RF sputter)

Top metal mask

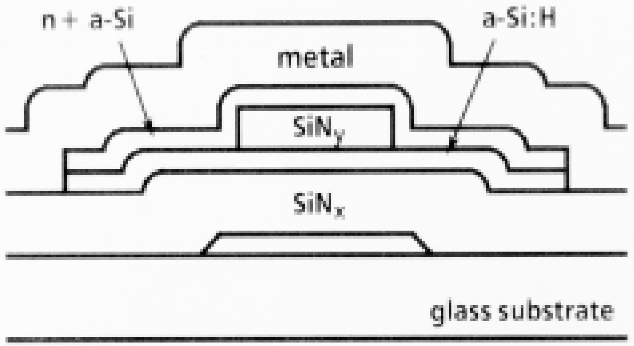
Top metal etch (wet)

“slot” mask

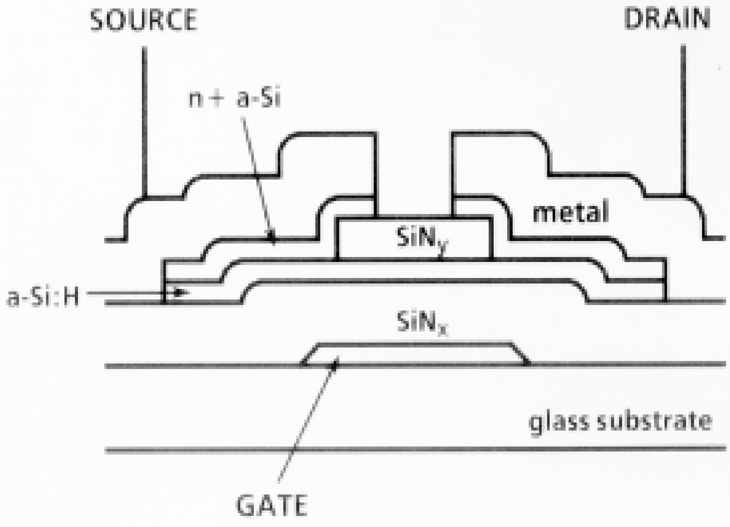
Top metal etch (wet)

n+ etch (RIE)
- gases: SF_6, $CFCl_3$
- pressure: 100 mT
- rate: 100 nm/min

Passivation SiO_xN_y deposition (PECVD)
- gases: SiH_4, NH_3, N_2O, He
- temperature: < 200°C
- thickness: ~600 nm
- rate: ~120 nm/min for in-line system
  ~200 nm/min for cluster tool



Schematic cross-sectional view of
a-Si TFT structure after top metal deposition

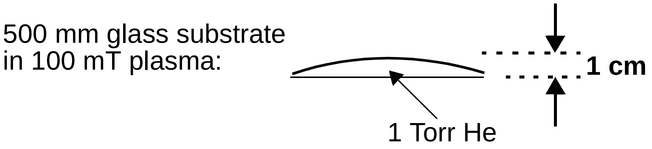


Plasma Etch Issues for Large-Area Substrates

Parallel-plate RIE tools are used to etch Si and SiN_x films (e.g. TEL cluster tool)

MAJOR CHALLENGES:

- **Improvement of throughput/etch-rate** (typically 15 plates/hour)
  --> new high-density-plasma etch tools
- **Improvement of uniformity** (typically +/- 20%)
- **Cooling of substrate**
  (no mechanical clamping, due to substrate bowing issues)



Note: Without cooling, 0.5 W/cm^2 --> burned photoresist

--> electrostatic clamping (e.g. Lam Research Corp.)

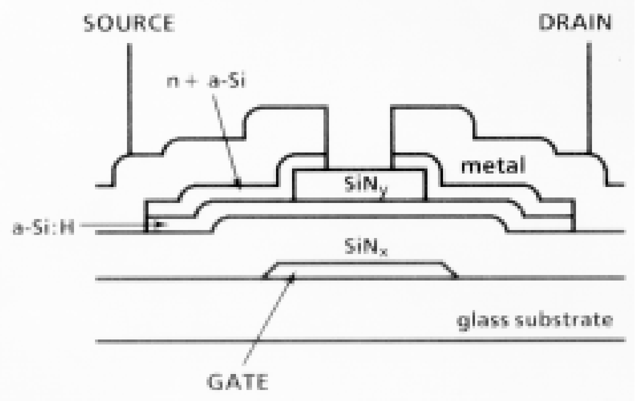
- **Development of etch processes for SiO_2 and metal films**
  e.g. AKT cluster RIE tool for etching Al (Cl_2 chemistry)
  (Note: Conventional RIE SiO_2 etch process would require > 10 kW)

NON-CONCERNS:

- **plasma damage** (thick dielectrics, insulating substrate)
- **anisotropy of etch** (large feature sizes, thin films)

Source: W. Yao, dpiX, a Xerox company

Future A-Si Technology Requirements/Trends



- **Process simplification (reduced number of photomasks)**
- **TFT performance improvement**
- **Self-aligned doping process** (ion shower doping)
- **Low sheet-resistivity gate line process** (Al, Cu)
- **Improved gate-nitride step coverage:**
  - development of gate-metal RIE process for better taper control
  - development of lower-stress nitride (maintain low trap density)
- **Dual layer SiO_2/SiN_x gate dielectric for:**
  lower defect density (improved yield)
  higher process throughput (e.g. APCVD SiO_2 deposition: SiH_4 & O_2; 430°C; ~1 µm/min)

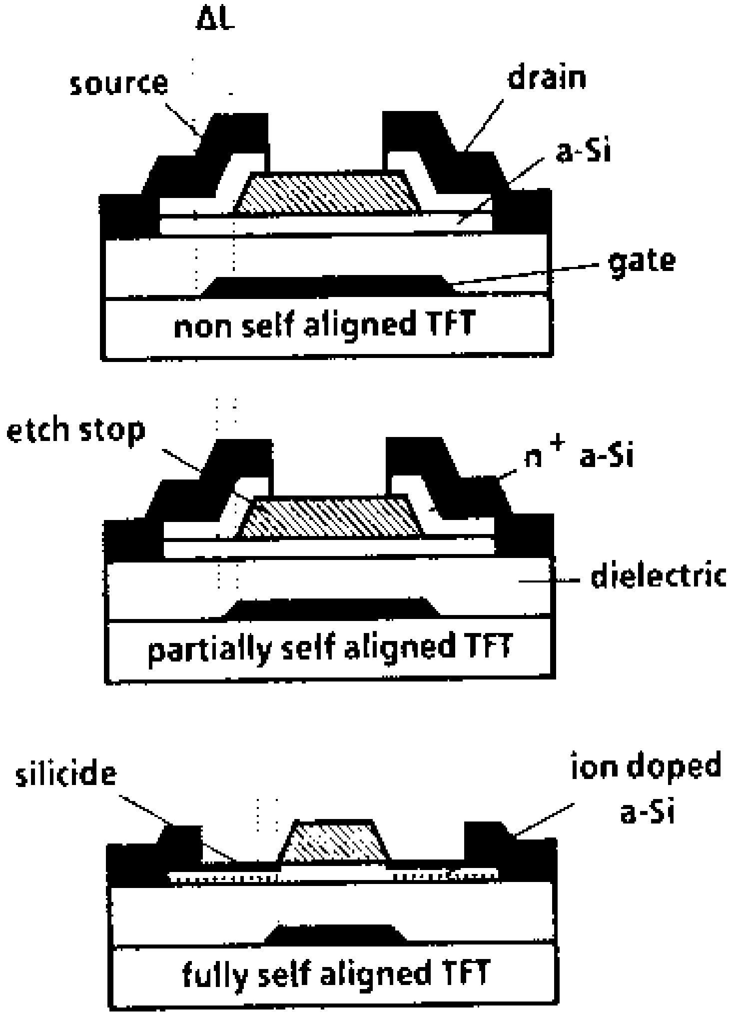
Self-Aligned a-Si TFT Structure

Goals :

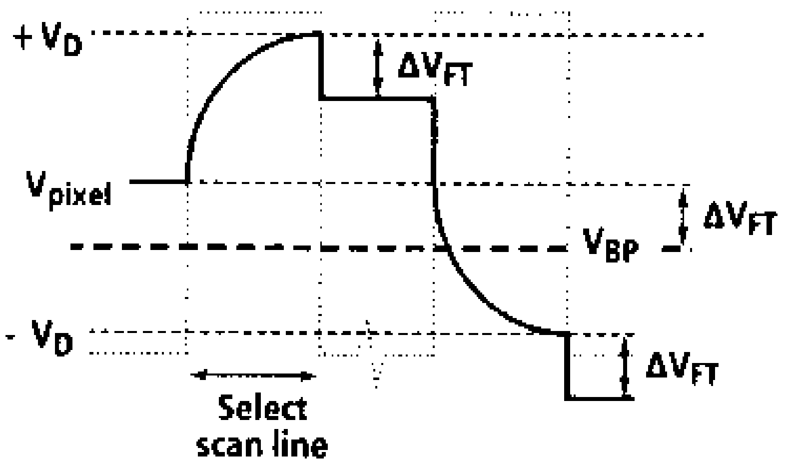
- reduce gate / source overlap
- reduce overlap variation
- reduce TFT size

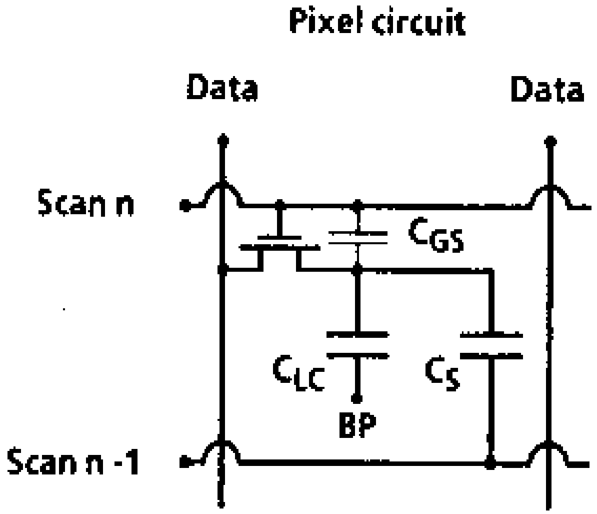
Challenges:

- ion doping
- light shielding



TFT Feedthrough Issue





$$\Delta V_{FT} = \Delta Vg \,.\, C_{GS} / (C_{LC} + C_S + C_{GS})$$

- TFT feedthrough due to TFT gate to source capacitance
- Adjust backplane voltage to zero net liquid crystal voltage
- Requires TFT feedthrough to be uniform across display

Ion Doping Systems for Large-Area Substrates

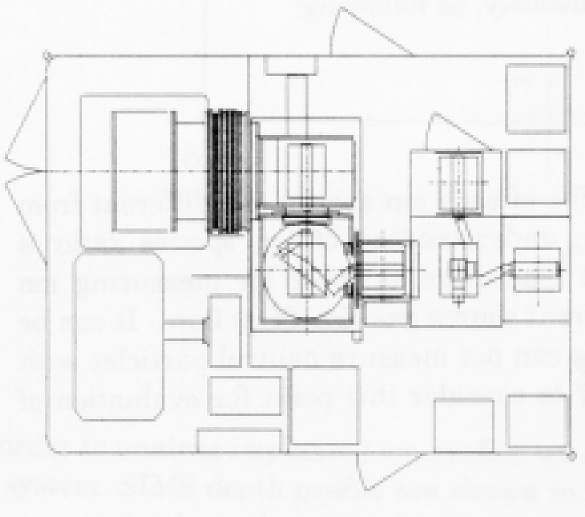


Fig. 1 Ion shower doping system.

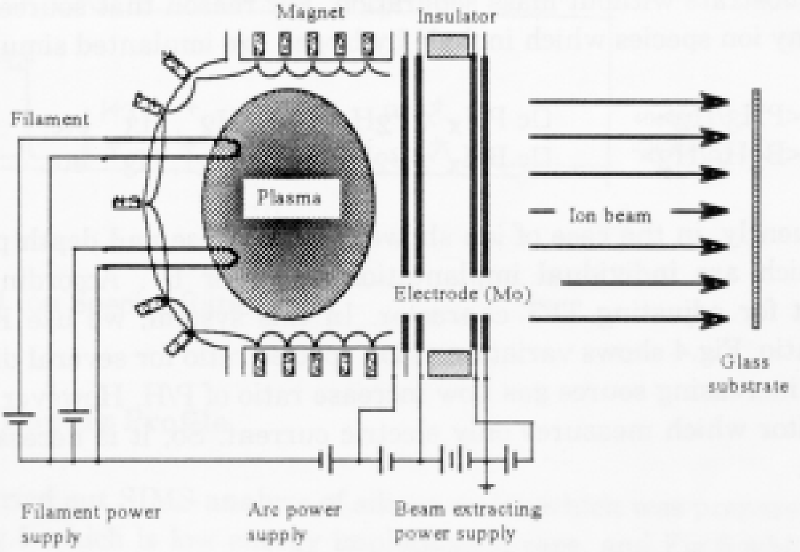


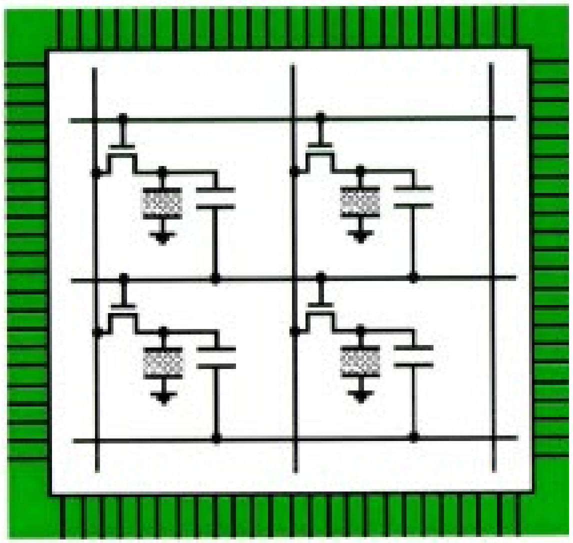
Fig. 2 Schematic diagram of ion source.

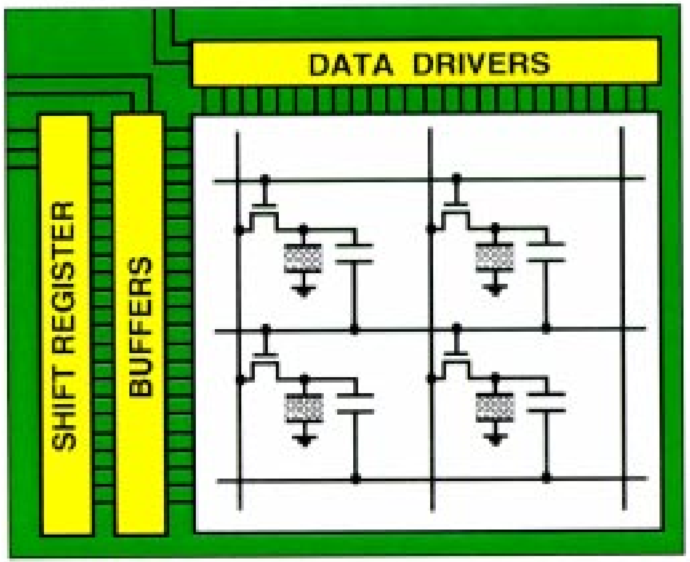
I. Nakamoto et al. (Ishikawajima-Harima Heavy Industries Co., Ltd.), February 1997

- **Ion source with 5% PH_3 or B_2H_6 in H_2**
  --> H^+, H_2^+, H_3^+, PH_x^+ or BH_x^+, etc.
- **Extraction electrodes (grids)**
  20 $\mu A/cm^2$ at 100 keV (--> $1x10^{16}$ cm^{-2} in 80s); 100 $\mu A/cm^2$ at 30 keV
  => Substantial heating of substrate (> 200^oC)

◆ **Magnetic filter for mass separation under development**

TFT Technology Comparison





AMORPHOUS SILICON	**POLYCRYSTALLINE SILICON**
● low TFT mobility (<1 cm^2/Vs) -> separate LSI drivers needed ● low-temperature (<350^{o}C) process -> glass substrates	● higher TFT mobility (μ_n, μ_p > 30 cm^2/Vs) -> smaller pixel TFTs (higher aperture ratio) -> integration of driver circuitry ◆ fewer external connections -> improved reliability ◆ reduced system cost ● high-temperature (>450^{o}C) process -> high strain-point glass or quartz substrates

Integrated Drivers for AMLCDs

Why?

- Limitations of packaging technologies
- Compact packaging
- Cost savings for small, high-resolution displays
- Custom drivers

Applications:

- Viewfinder displays
- Head-mounted displays
- Projection displays

Materials used:

- Polycrystalline silicon
- Crystalline silicon (transparent or Si substrates)

Production of Poly-Si TFT-AMLCDs

ANNOUNCED LARGE-AREA POLY-SI TFT-AMLCD FABS

(2”- to 6”-diagonal displays)

Sony and Sanyo:	1996 (300 x 400 mm)
Sharp:	1997 (400 x 500 mm)
Fujitsu,Matsushita:	1997
LG Electronics:	1997
Samsung:	1997
DTI:	1997 (12”-diagonal displays)
NEC:	1998
Hitachi:	1998

Source: *The DisplaySearch Monitor*, June 13, 1996, DisplaySearch, Austin, TX

INITIAL APPLICATIONS:

(high-pixel-density displays)

- digital video camcorders
- digital still cameras

Production of Poly-Si TFT-AMLCDs (II)

First commercial product incorporating low-temp. poly-Si TFT-AMLCD:

JVC’s DVM-1 digital video camera
2.5”-D display (Sony):
- 800 x 225 pixels
- 8-bit gray scale
- 56% aperture ratio
- integrated driver electronics

Future markets:

- small and medium-sized direct view displays
- LCD panels for front and rear projectors
- notebook PC displays
- LCD monitors

Most of TFT-AMLCD fab capital spending in 1998 was dedicated to adding poly-Si AMLCD production capacity*

- ~10X capacity growth rate as compared with a-Si AMLCD production, in 1998 & 1999

*Source: *The DisplaySearch Monitor*, March 23, 1998, DisplaySearch, Austin, TX

TFT Requirements for Integrated Drivers

- **CMOS** (reduced power consumption)
- **High-frequency operation**
  - high mobilities (> 30 cm^2/Vs)
  - low V_{th} (< 3 V)
  - low source/drain series resistances (< 1 kΩ/☐)
- **High hot-carrier immunity**
  - lightly doped drain structure (NMOS)

AMLCD Substrate Materials

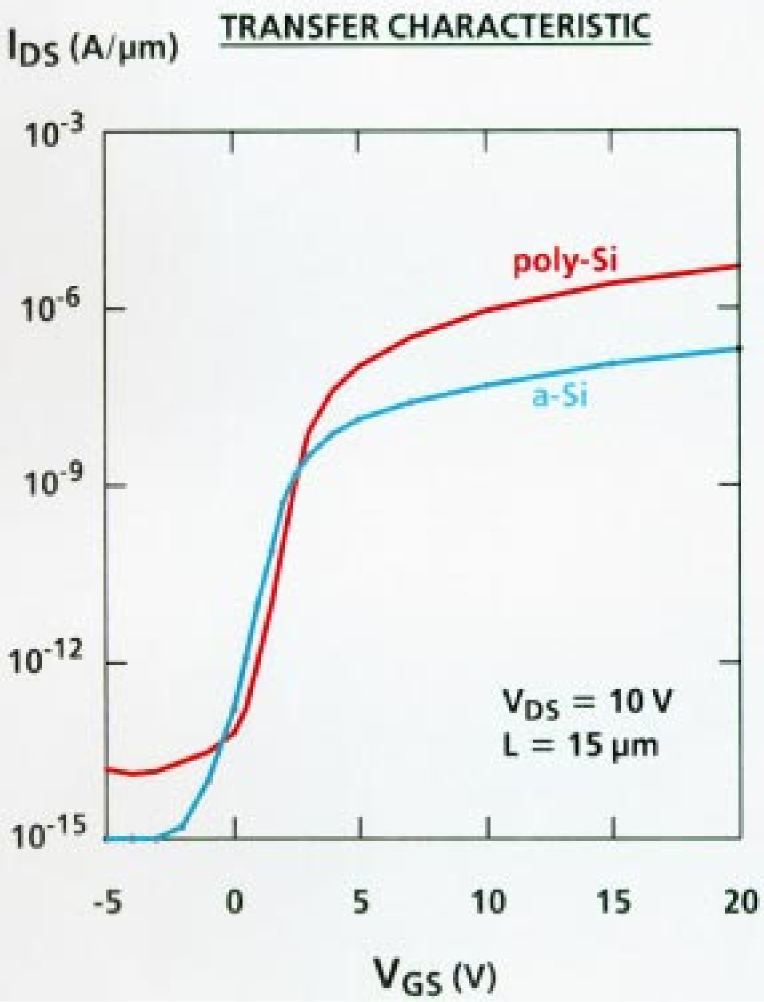
MATERIAL	MAXIMUM TEMPERATURE
Silicon	1100°C
Glass*	~600°C
Plastic:	
Polyimide	250°C
Polyethersulfone	200°C
Polyester	100°C

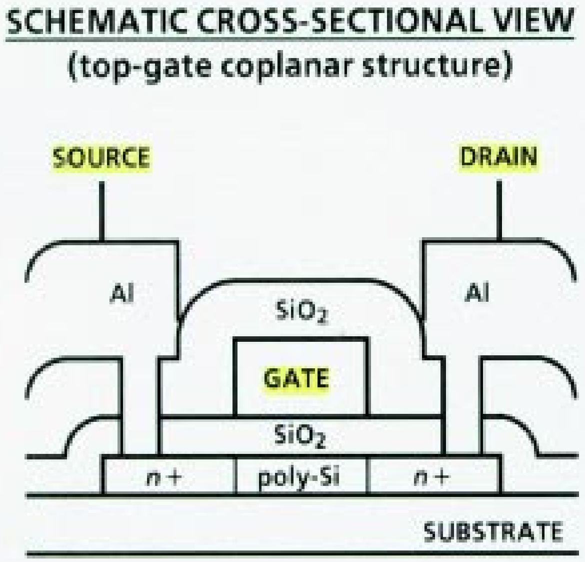
*** non-alkali borosilicate or aluminosilicate glass**

PLASTIC SUBSTRATES:

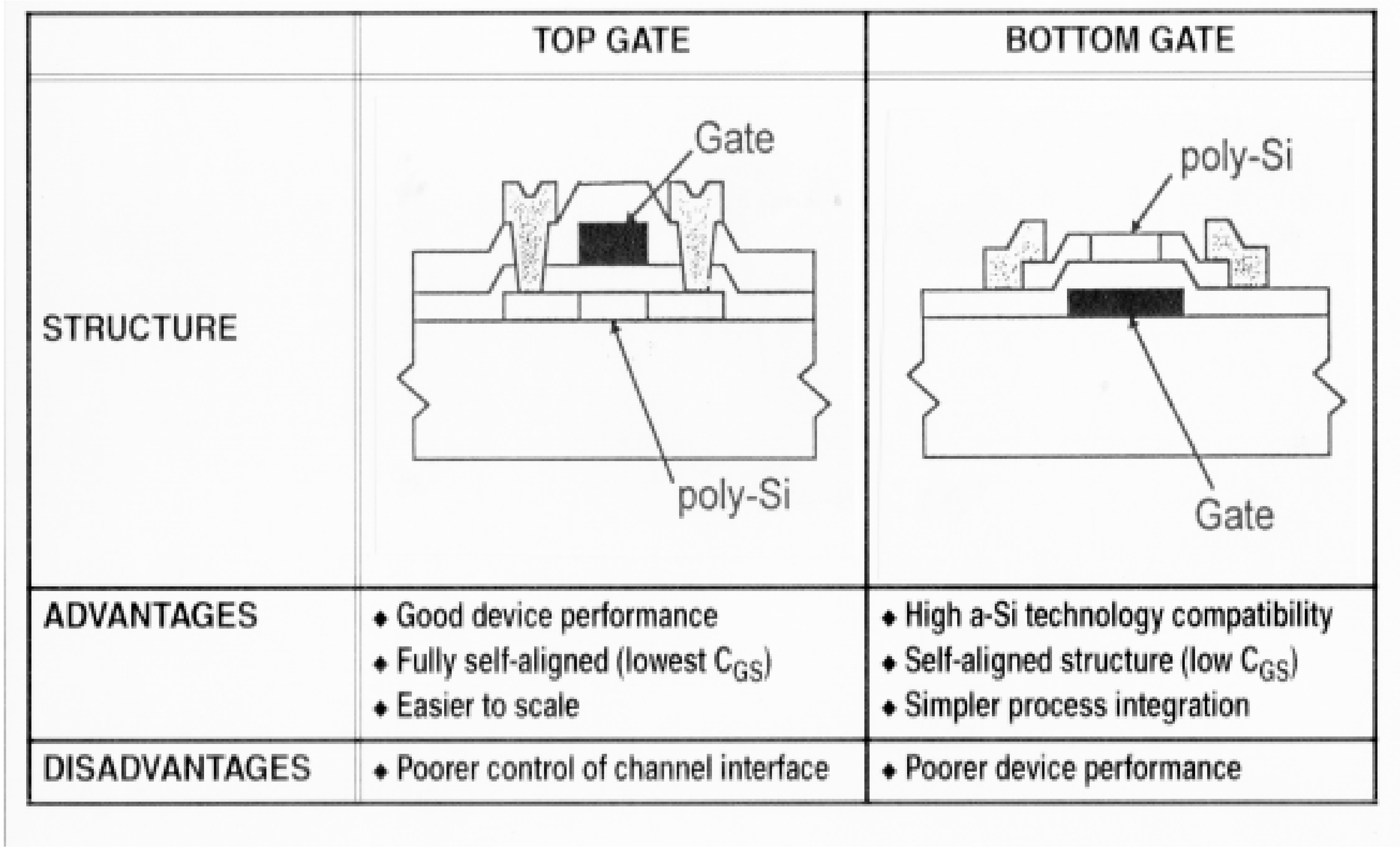
- lightweight, rugged displays
- ultra-low TFT processing temperatures
- reliability issues
  --> poly-Si TFT technology advantageous

Polycrystalline-Si Thin-Film Transistor





Poly-Si TFT Architecture Considerations



	TOP GATE	BOTTOM GATE
STRUCTURE		
ADVANTAGES	◆ Good device performance ◆ Fully self-aligned (lowest C_{GS}) ◆ Easier to scale	◆ High a-Si technology compatibility ◆ Self-aligned structure (low C_{GS}) ◆ Simpler process integration
DISADVANTAGES	◆ Poorer control of channel interface	◆ Poorer device performance

Poly-Si TFT Fabrication Process (I)

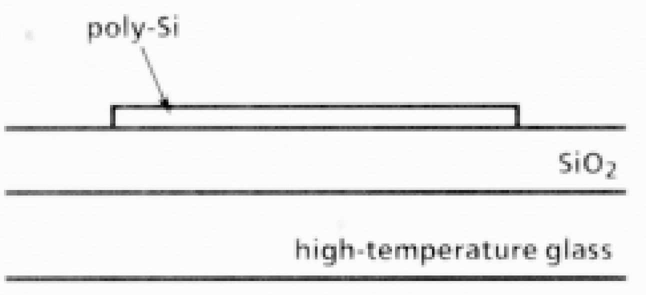
Buffer-layer SiO_2 deposition (LPCVD, APCVD or PECVD)
gases: SiH_4 or TEOS, O_2
temperature: 300-400°C
thickness: ~500 nm

Active Si layer deposition (LPCVD or PECVD)
gases: SiH_4 or Si_2H_6
temperature: 350-550°C
thickness: 50-100 nm

Si crystallization
- **Furnace** (500-600°C)
- **Rapid thermal annealer**
- **Laser**

Island mask

Poly-Si island etch (RIE)
SF_6 chemistry
rate: ~200 nm/min



Schematic cross-sectional view of poly-Si TFT structure after island etch

Poly-Si TFT Channel-Layer Deposition

COMPARISON OF a-Si DEPOSITION TECHNIQUES

	LPCVD (~450^{o}C)	**PECVD** (<350^{o}C)	**PVD** (<100^{o}C)
Hydrogen content (atomic %)	**< 1**	**> 10**	**< 1**
Thickness uniformity (+/- %)	**5**	**> 5**	**< 5**

- **PECVD & PVD techniques compatible with plastic substrates**
- **PVD films comparable to LPCVD films, for TFT performance**
  - trace metallic contamination may be an issue

(Y.-J. Tung *et al.*, presented at the 56th Annual Device Research Conference)

- **PECVD films have high H content**
  - extra dehydrogenation step required
  - poorer TFT performance
- **Thickness uniformity is an issue for PECVD films**

Crystallization of Amorphous Silicon Thin Films

COMPARISON OF CRYSTALLIZATION TECHNIQUES

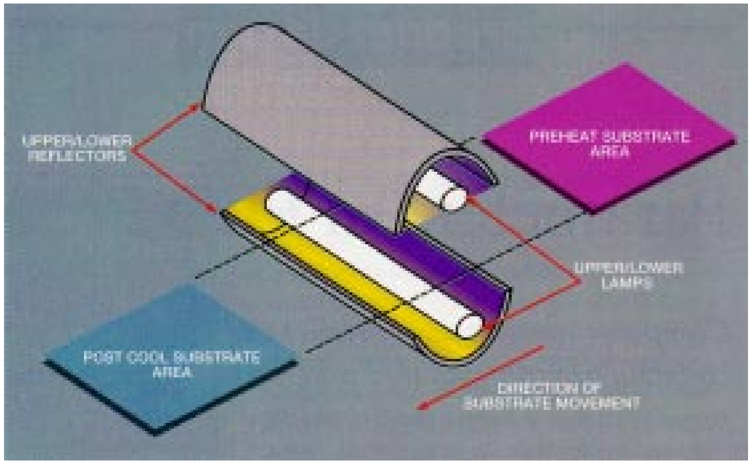
	Furnace	RTP	Laser
Substrate Temperature	**> 500^{o}C**	**> 700^{o}C**	**R.T.**
Throughput (plates/hr)	**15**	**> 60**	**20**
Uniformity	**good**	**good**	**fair**

- **Only laser annealing compatible with plastic substrates**
  Buffer layer protects substrate; surface temperature is above softening point for <100 ms (P. G. Carey *et al.*, 1997 IDRC)

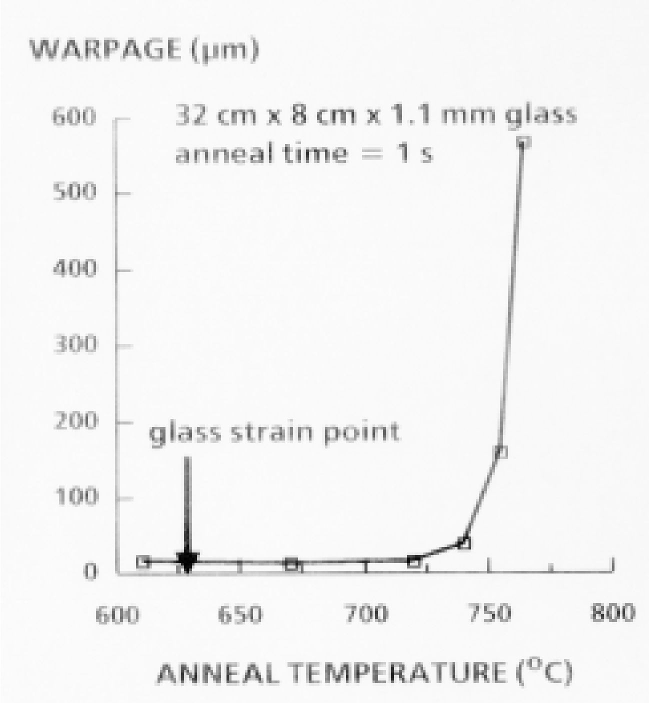
- **Challenges:**
  - **poor uniformity --> poor TFT performance**
  - **low throughput --> bottleneck in TFT process**

Large-Area Rapid Thermal Annealer

- **Xe arc lamp system -- light focused to 15 mm width**
- **Substrate scanned under the beam**
- **Typical crystallization process** (for 100 nm-thick LPCVD a-Si)**:**
  ~550^{o}C preheat, ~1 s residence time, >700^{o}C peak temperature
- **High throughput** (> 60 plates/hr)**, good uniformity -- but warpage is an issue**
- Equipment supplier: Intevac, Inc.



Intevac Rapid Thermal Annealing System

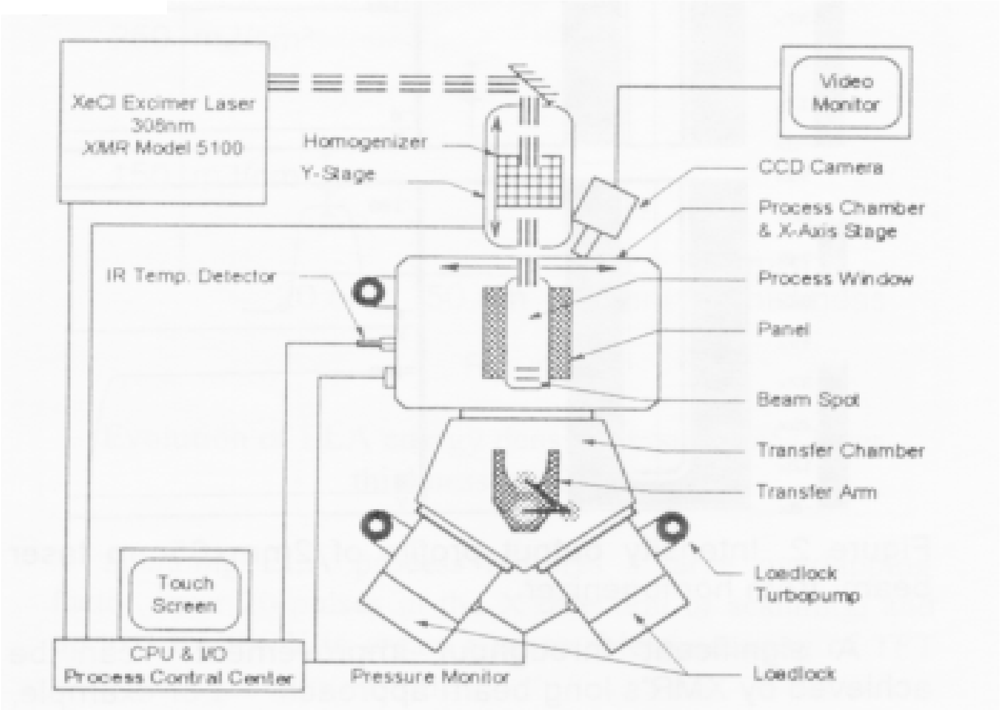


Large-Area Laser Annealing Systems

- **Fast pulsed** (~40 ns) **XeCl** (308 nm) **excimer laser beam**
- **Small beam spot** (100 mm^2) **raster-scanned across substrate** (at up to 200 mm/s)
- **Typical crystallization process** (for 100 nm-thick LPCVD a-Si)**:**
  ~400 mJ/cm^2, 300 Hz, 90% overlap (in fast-scan direction)

◆ **Uniformity is an issue -- tradeoff with process throughput**
  - can be improved with substrate heating, increased beam overlap

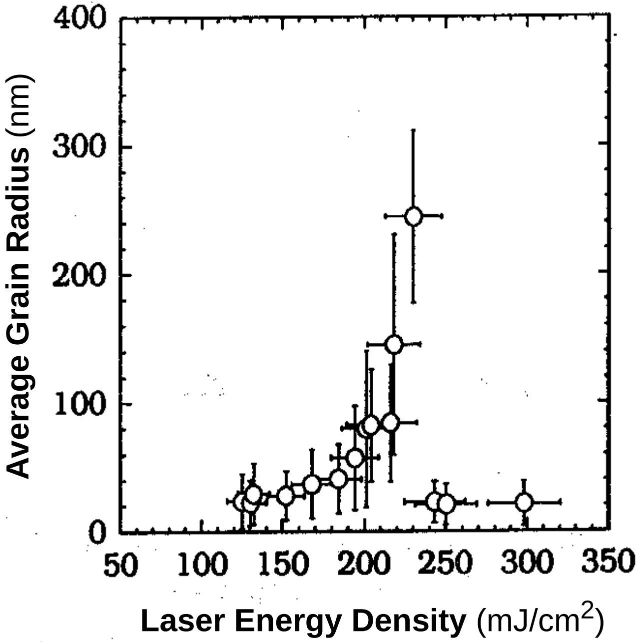
- Equipment suppliers: Lambda Physik, XMR, SOPRA



XMR's ELA system

Laser Crystallization of a-Si Films

Poly-Si grain size dependence on laser energy density:



- **surface roughness also increases with grain size**

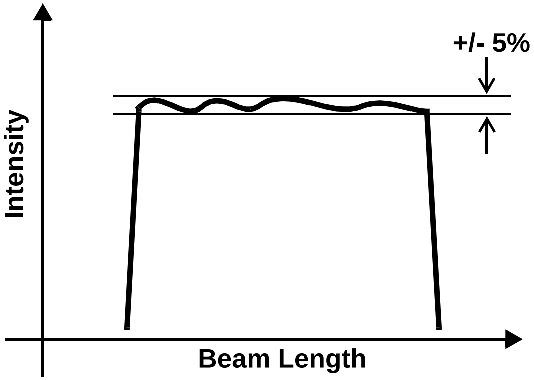
J. Im *et al.*, *Appl. Phys. Lett.*, **63**, 1969 (1993)

- **Peak location dependent on film thickness**
- **Direct correlation between grain size, TFT performance**
- **Narrow process window** (large-grained films)

Laser Crystallization Issues

- **Stability of high-power laser systems**
  - **- pulse-to-pulse variations in beam energy**
    - ~15% variation; 1.7% std. dev. (K. Yoneda, 1997 IDRC)

- **Beam homogeneity** (+/- 2% required for mass production)
  - - critical for achieving uniformly crystalline film



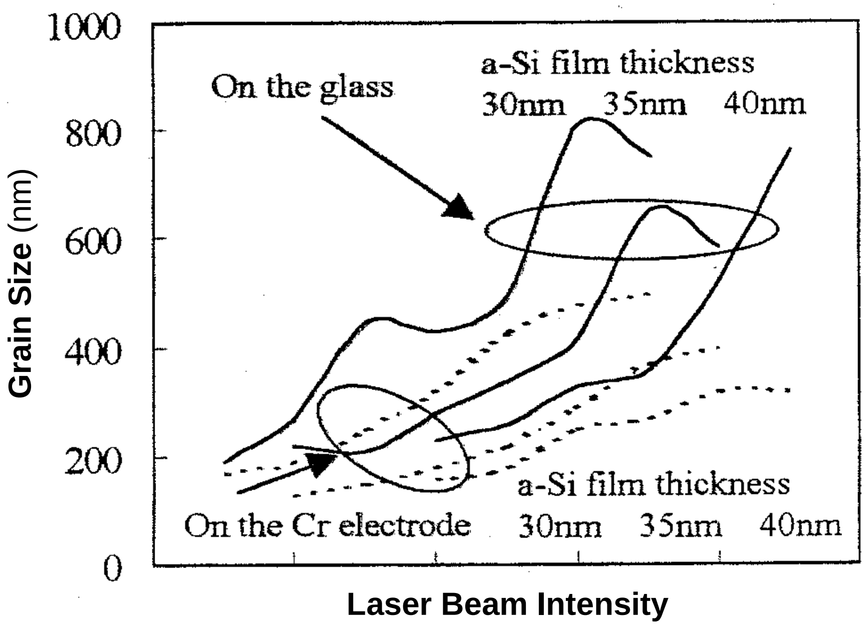
Process uniformity can be improved by:

- ◆ heating substrate and/or
- ◆ increasing beam overlap

--> trade-off with process throughput

Laser Crystallization Issues (continued)

Poly-Si grain size dependence on Si film thickness:



K. Yoneda, 1997 IDRC

- **Thickness uniformity must be better than +/- 5%**
- **Smaller grains are obtained with patterned bottom gate** (heat sink effect)

Poly-Si TFT Fabrication Process (II)

Gate SiO_2 deposition (LPCVD or PECVD)

gases: SiH_4 or TEOS, O_2

temperature: ~400°C

thickness: 100 nm

Gate SiO_2 anneal (600°C)

Gate Si deposition (LPCVD or PECVD)

gas: SiH_4 or Si_2H_6

temperature: 350-550°C

thickness: ~350 nm

Gate mask

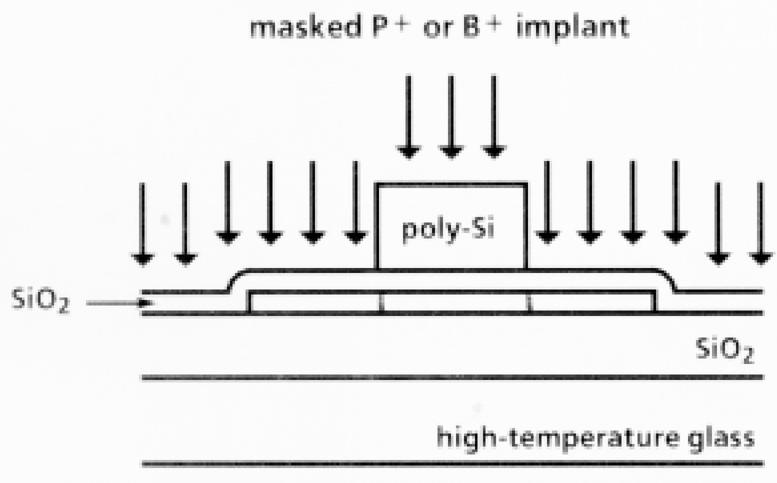
Poly-Si gate etch (RIE)

SF_6 chemistry

rate: ~200 nm/min

n+ mask; phosphorus implant

p+ mask; boron implant



Schematic cross-sectional view of poly-Si TFT structure after gate etch

SiO_2 Deposition

COMPARISON OF METHODS FOR LARGE-AREA SUBSTRATES

	LPCVD 400°C	**APCVD** 300-500°C	**PECVD** 300-500°C	**ECR** R.T. to 400°C
Film quality	**excellent**	**good**	**excellent**	**excellent**
Step coverage	**excellent**	**excellent**	**fair**	**poor**
Thickness uniformity (+/- %)	**> 10**	**2**	**5**	**< 5**
Throughput (100 nm) (plates/hr)	**10**	**60**	**30**	**10**

SiO_2 Deposition (II)

COMPARISON OF LOW-TEMP. OXIDE DEPOSITION TECHNIQUES

	PECVD 100°C	**ECR** 100°C	**PVD** R.T.
Film quality	**good**	**excellent**	**good**
Step coverage	**fair**	**poor**	**poor**
Thickness uniformity (+/- %)	**5**	**< 5**	**< 5**

- **Requirements for gate oxide:** (H. J. Kim, 1997 IDRC)
  - $D_{it} < 5 \times 10^{10}$ cm^{-2}
  - $\mathcal{E}_{bd} > 8$ MV/cm
  - ΔV_{th} (BTS) < 0.1 V
- **Several techniques are compatible with plastic substrates**
- **Oxygen plasma treatment can improve Si/SiO_2 interface quality**

Source/Drain Doping for Poly-Si TFTs

DOPING REQUIREMENTS:

- **Implant dose: 1 - 5 x 10^{15} cm^{-2} P^+ or B^+**
  (ρ_s < 1 kΩ/square)
- **Implant energy: 10 - 100 keV**
- **Uniformity: better than 10%**
- **Minimal damage**
- **Minimal introduction of contaminants**
- **High throughput**
  --> Ion shower doping
  - throughput limited by:
    - substrate heating and charging
    - robotic handling
  - proton co-implantation --> low ρ_s
  - post-implant annealing --> lower ρ_s

Poly-Si TFT Fabrication Process (III)

Passivation SiO_2 deposition (LPCVD or PECVD)
gases: SiH_4 or TEOS, O_2
temperature: ~400°C
thickness: 700 nm

Dopant-activation anneal
- **Furnace** (550-600°C)
- **Rapid thermal annealer** (~700°C)
- **Laser** (~200 mJ/cm^2)

Hydrogenation (plasma)
300-350°C

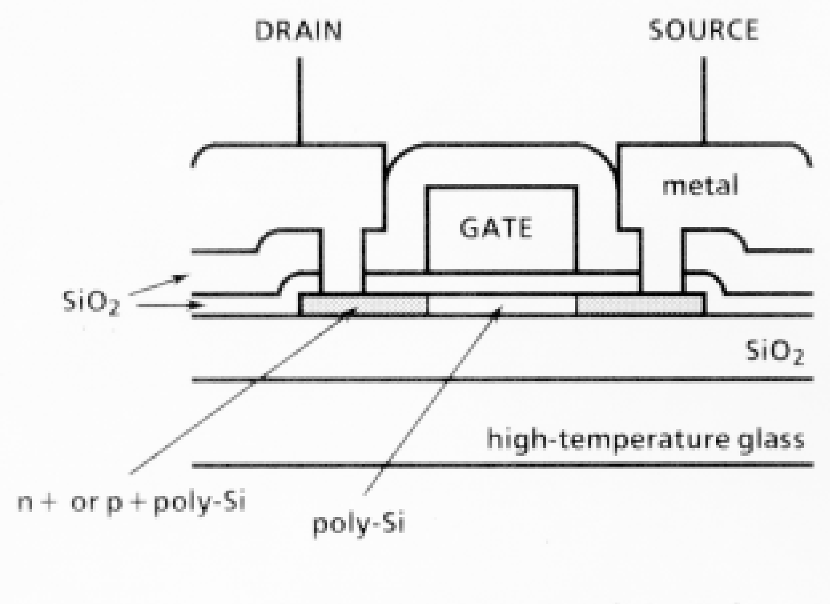
Contact mask

Contact etch (wet)

Metal deposition (RF sputter)

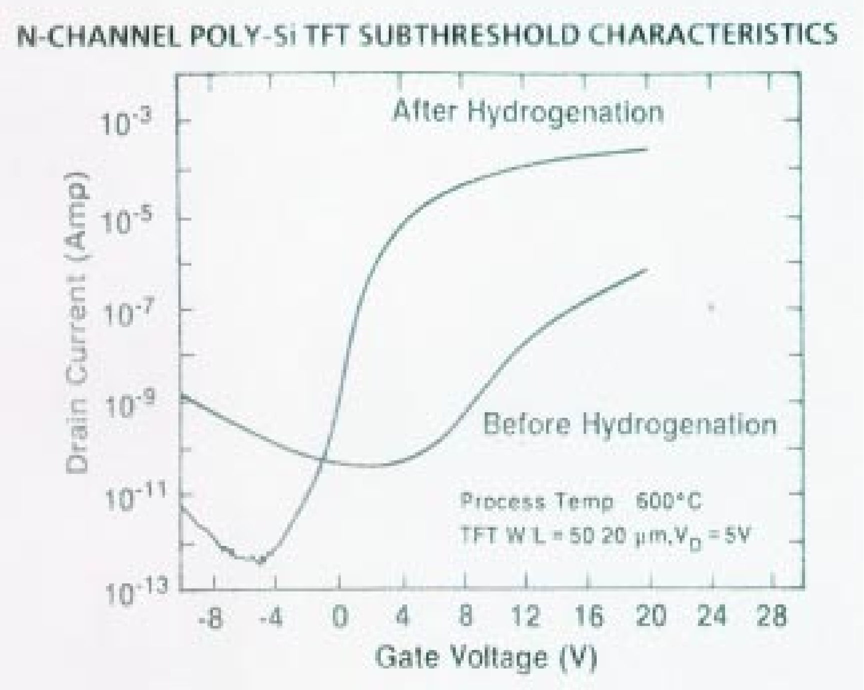
Metal mask

Metal etch (wet)



Schematic cross-sectional view of completed poly-Si TFT structure

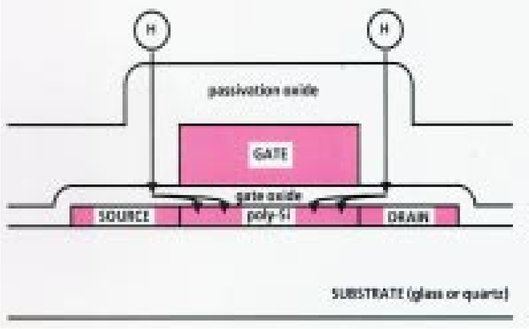
Defect Passivation in Poly-Si TFTs



PLASMA HYDROGENATION:

- Conventional diode reactor
- Substrate heated to ~350^{o}C, immersed in hydrogen plasma

◆ Process time: many hours



N-CHANNEL TFT * PERFORMANCE	μ_{eff} (cm^2/Vs)	V_{TH} (V)	I_{min} (pA)	S_{th} (V/dec)
BEFORE HYDROGENATION	5	14	150	2.1
AFTER HYDROGENATION	40	2	1	0.55

* W = 50 μm; L = 20 μm

Effect of Hydrogenation on Device Uniformity

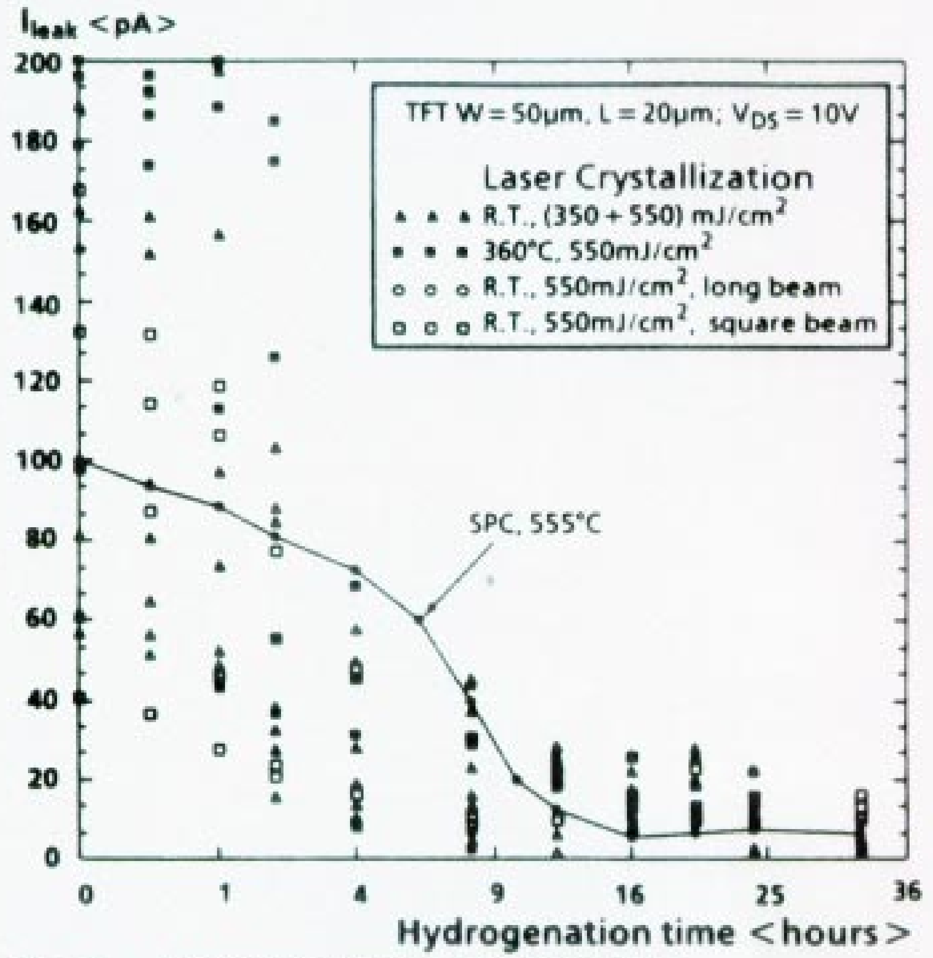


Fig. 5. Leakage current of p-Si TFTs vs. hydrogenation time for various laser crystallization treatments and SPC.

I-W. Wu, AM-LCD '95

- Hydrogenation necessary for uniform TFT performance

Alternative Hydrogenation Methods

◆ **HIGH-DENSITY PLASMA (ECR, ICP, or Helicon)**

- heated substrate
- H_2 plasma exposure: ion densities > 10^{11} cm^{-3}

◆ **SOLID-SOURCE DIFFUSION**

- PECVD Si_xN_y deposition (~150 nm, compressive)
- Thermal anneal: 450°C, 10 minutes

◆ **H^+ ION IMPLANTATION + ANNEAL**

- Dose: ~1 x 10^{16} cm^{-2}
- Energy: > 100 keV
- Thermal anneal: 250-400°C, 10-60 minutes

COMPARISON OF HYDROGENATION METHODS

	plasma exposure	solid-source diffusion	ion implantation
TFT performance	excellent	good	good
TFT reliability	good*	good	poor
Process uniformity	good	good	poor
Process throughput	low	high	medium
Equipment cost	moderate	moderate	high

* conventional RF, or ICP or Helicon plasma source

Effects of Device and Process Architectures

HYDROGENATION PROCESS THROUGHPUT CAN BE IMPROVED BY:

- **Reducing TFT channel length** (4X improvement)
- **Adopting bottom-gate TFT architecture** (10X improvement)
- **Performing hydrogenation earlier in process**
  -requires low-temperature source/drain formation process

HYDROGENATION STEP CAN BE <u>ELIMINATED</u> FOR

- **High-quality (low-defect-density) poly-Si films**
  e.g. films obtained by metal-induced lateral crystallization
  (S.-W. Lee *et al.*, *IEEE Electron Device Letters*, **17**, p.160, 1996)
- **Single-crystalline Si films**
  e.g. films obtained by sequential lateral solidification
  (J. S. Im *et al.*, *Applied Physics Letters*, **70**, p. 3434, 1997)

Ultra-Low-Temp. Poly-Si TFT Technology Issues

High temperatures (>250^{o}C) **required for hydrogenation**
- cannot be used in ultra-low-temp. TFT process

=> TFT performance uniformity will be an issue!

- **Low-defect-density poly-Si films must be achieved by channel formation process**

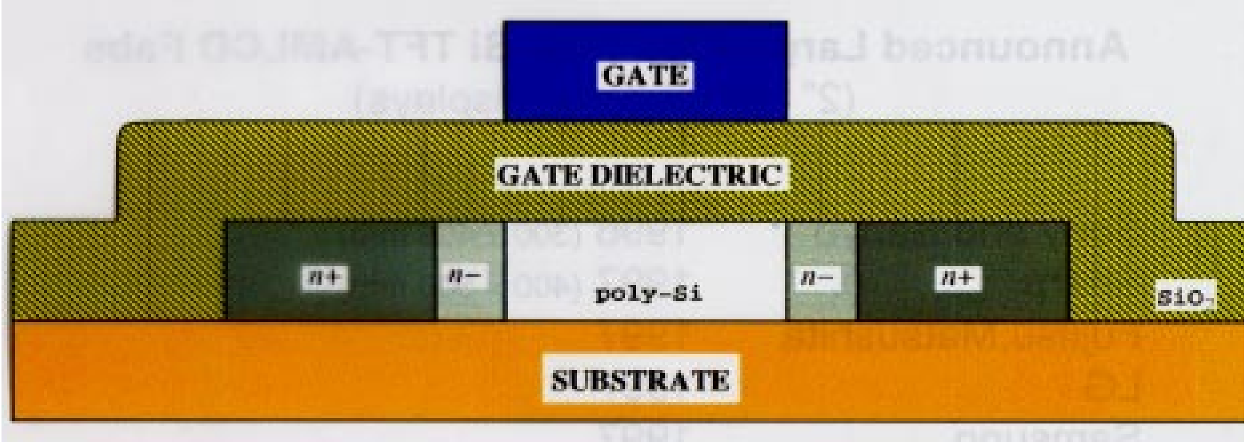
- **TFTs should exhibit improved reliability...**

Poly-Si TFT Reliability

ON-state stress (saturation region)
--> increase in bulk and interface trap densities
--> V_{th} increase
- related to hydrogen in channel film

◆ Issue for driver circuitry

=> Offset-drain or LDD structures required



Future Poly-Si Technology Requirements/Trends

- **DEVICE FABRICATION:**
  - **Reduced thermal-processing budget**
    (channel formation, dopant activation)
  - **Improved defect-passivation throughput**

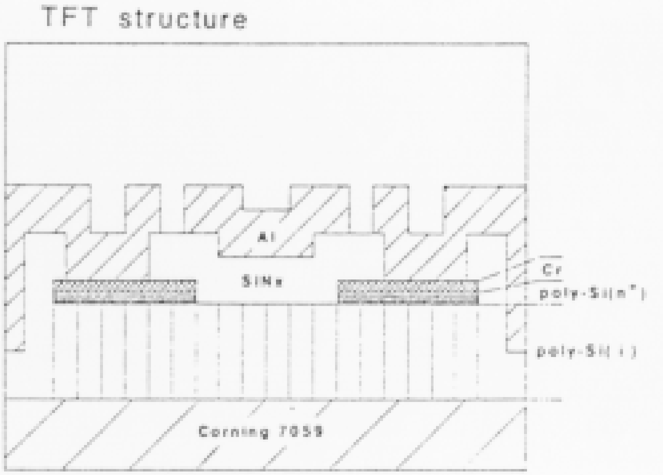
- **DEVICE PERFORMANCE:**
  - **Improved uniformity**
  - **Reduced leakage current**
  - **Improved reliability**

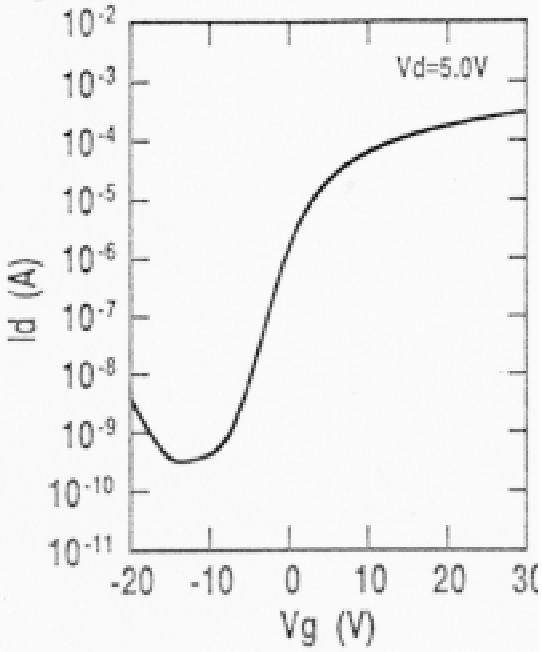
=> NEW PROCESSING TECHNIQUES

New Poly-Si Deposition Technique

PLASMA CHEMICAL VAPOR DEPOSITION:

- ◆ **SiF_4/SiH_4 gas mixture**
- ◆ **$T_{growth} < 450^oC$**
- ◆ **grain sizes up to 250 nm**
- ◆ **n-channel TFT mobility > 40 cm^2/Vs**



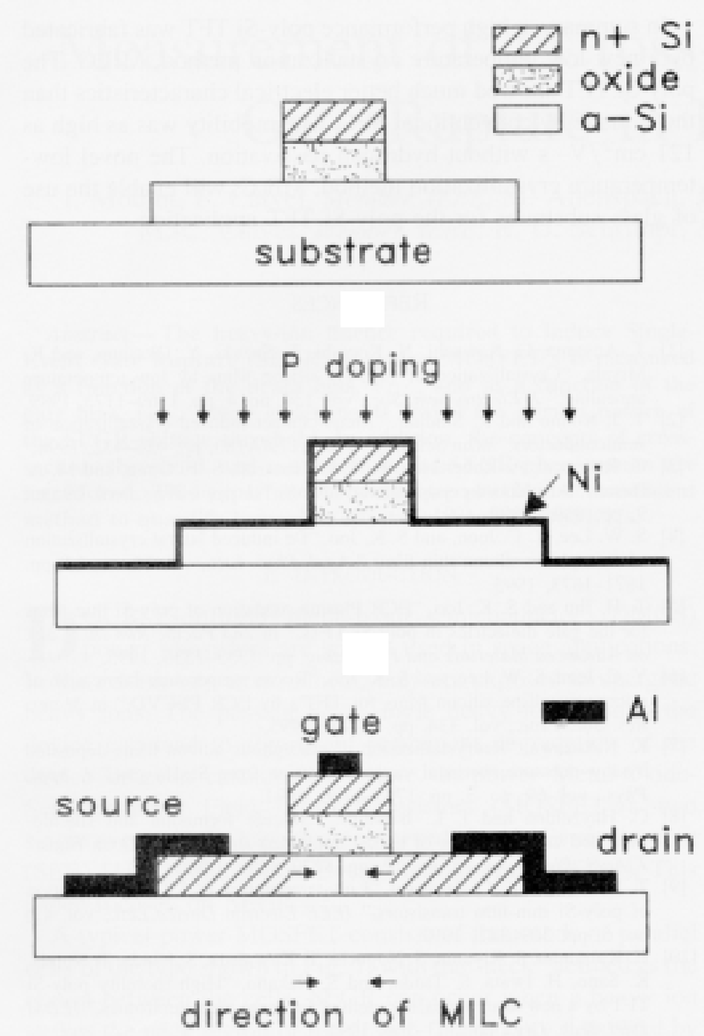


Nagahara et al., Jpn. J. Appl. Phys. Vol. 31 (1992) pp. 4555-4558

- **thick films** (~700 nm) **required**
- **low deposition rates** (~5 nm/min)

New Crystallization Technique

METAL-INDUCED LATERAL CRYSTALLIZATION



- 100 nm LPCVD a-Si channel
- 100 nm ECR CVD gate oxide
- PECVD poly-Si gate

◆ **0.5 nm PVD Ni after gate etch**

- **500^oC crystallization**
  (1.6 μm/hr lateral growth rate)
- **NO HYDROGENATION NEEDED**

TFT parameter	**N-channel** *****	**P-channel** ******
mobility (cm^2/Vs)	**121**	**90**
threshold (V)	**1.2**	**-1.7**
subth. slope (V/dec)	**0.56**	**0.71**
leakage (pA/μm)	**0.36**	**~0.5**

* S.-W. Lee and S.-K. Joo, IEEE Electron Device Letters, Vol. 17, No. 4, pp. 160-162, 1996.

** S.-W. Lee et al., IEEE Electron Device Letters, Vol. 17, No. 8, pp. 407-409, 1996.

New Crystallization Technique (cont'd)

Announcement in January 1998 by
Sharp Corporation & Semiconductor Energy Laboratory:

- "Continuous grain silicon" technology (MILC) for highly integrated display systems
- Products to incorporate CGS technology in FY98
  - video projectors
- > 500 patents applied for (!)

Summary: TFT Technologies for AMLCDs

FUTURE TRENDS

A-Si technology:

- ◆ **Improved performance**
  - scale-down of device dimensions
  - self-aligned doping of source/drain contacts
  - development of low sheet-resistivity-gate process
- ◆ **Lowered cost**
  - simplification of process

Poly-Si technology:

- ◆ **Lowered cost**
  - reduction in thermal processing budget
  - improvement in process module throughput