EE290D   Handout #10
Spring 1999   T.-J. King

HOMEWORK ASSIGNMENT #1 SOLUTIONS

Problem 1:

Let D = panel diagonal, H_p = panel height + border widths = $(3D/5) + 2$, W_p = panel width + border widths = $(4D/5) + 2$, H_s=substrate height, W_s=substrate width:

D (in)	D (cm)	H_p (cm)	W_p (cm)	H_s (cm)	W_s (cm)	*H_s/H_p	*W_s/W_p	^W_s/H_p	^H_s/W_p
12.1	30.73	20.44	26.59	36	46.5	1.76	1.75	2.27	1.35
12.1	30.73	20.44	26.59	55	65	2.69	2.44	3.18	2.07
12.1	30.73	20.44	26.59	65	83	3.18	3.12	4.06	2.44
13	33.02	21.81	28.42	65	83	2.98	2.92	3.81	2.29
14	35.56	23.34	30.45	65	83	2.79	2.73	3.56	2.13
15	38.10	24.86	32.48	65	83	2.61	2.56	3.34	2.00
16	40.64	26.38	34.51	65	83	2.46	2.40	3.15	1.88
17	43.18	27.91	36.54	65	83	2.33	2.27	2.97	1.78
18	45.72	29.43	38.58	65	83	2.21	2.15	2.82	1.68
19	48.26	30.96	40.61	65	83	2.10	2.04	2.68	1.60
20	50.80	32.48	42.64	65	83	2.00	1.95	2.56	1.52
21	53.34	34.00	44.67	65	83	1.91	1.86	2.44	1.46

*panels oriented in same direction as substrate (long sides of panels parallel to long sides of substrate)
^panels oriented in orthogonal direction to substrate (long sides of panels parallel to short sides of substrate)

a) Considering that only an integral number of display panels can be fabricated on a single substrate:
    i) 2 panels can be fabricated on a single substrate for a Generation II fab.
    ii) 6 panels can be fabricated on a single substrate for a Generation III fab.
    iii) 9 panels can be fabricated on a single substrate for a Generation III.5 fab.

b) From the above table, it can be seen that a single 65 cm x 83 cm substrate can accommodate six 14"D panels, six 15"D panels, four 16"D panels, four 17"D panels, four18"D panels, four 19"D panels, or two 20"D panels. The manufacturing cost per display panel will increase significantly if the number of panels per substrate decreases significantly, i.e. **at 16"D, and then at 20"D**. Conversely, the cost of manufacturing a 15"D display is not significantly larger than the cost of manufacturing a 14"D display. For this reason, some manufacturers have discontinued production of 14"D LCD desktop monitors (produc-

ing 15"D products instead)!

Problem 2:
a) Let D = panel diagonal, C = number of columns, R = number of rows.

Pixel size = (4D/5)/C = (3D/5)/R:

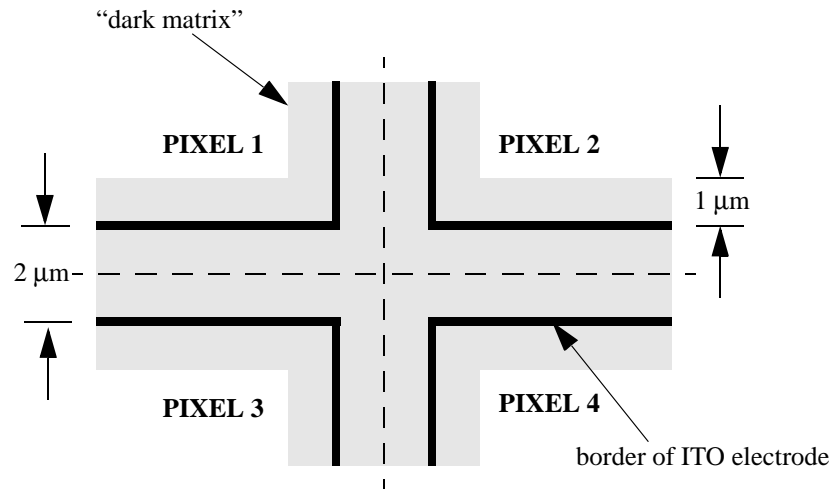**i)** 10"D VGA display: C = 640, R = 480; pixel size = **317.5 μm**

ii) 12.1"D SVGA display: C = 800, R = 600; pixel size = **307.3 μm**

iii) 15"D SXGA display: Aspect ratio = 5:4! C = 1280, R = 1024; pixel size = **232.4 μm**

iv) 42"D VGA display: C = 640, R = 480; pixel size = **1333.5 μm**

b) The intersection of 4 pixels on the STN-LCD in the ideal case (perfect layer-to-layer alignment) is sketched below:

The ITO-to-ITO spacing is 2 μm, and the dark matrix overlaps the ITO electrode by 1 μm. The active pixel area is $(P - 4 \mu m)^2$ where P = pixel size = 317.5 μm from part a). Hence, the maximum pixel aperture ratio is $(P - 4 \mu m)/P^2$ = **97.5%**. Note that the aperture ratio is significantly higher in passive-matrix displays as compared with active-matrix displays.

Problem 3:
a) For a dual-scan VGA display, the number of matrixed rows M = 240. From the plot on the left-hand side, L_{off} = 0.33 and L_{on} = 0.25. PCR = $(L_{on}/L_{off})/M + (M-1)/M$ = **1.001**.

b) From the plot on the right-hand side, L_{off} = 0.45 and L_{on} = 0.03. PCR = $(L_{on}/L_{off})/M + (M-1)/M$ = **1.06**.

c) For a dual-scan SVGA display, M = 300. From the Alt-Pleshko formula, $<V_{off}>/<V_{on}>$≥1.06. Choose V_{off} = 2.59 V and V_{on} = 2.75V. From the plot on the right-hand side, L_{off} = 0.43 and L_{on} = 0.03. PCR = $(L_{on}/L_{off})/M + (M-1)/M$ = **1.04**. The higher resolution display has poorer contrast, as expected (but not poor as a passive-matrix TN display).

Problem 4:
a) For a 6-bit color display, each sub-pixel must be able to display 64 distinct levels of gray. For the TN electro-optic characteristic given, the difference in transmitted luminance between two adjacent levels of gray is 0.5/64=0.0078. The maximum slope of this characteristic is ~0.3/0.8V=0.375/V; therefore, the minimum change in applied voltage between two levels of gray is 0.0078/0.375=**21 mV**. This is the maximum allowable change in pixel voltage during a frame time.

b) During a frame time, the voltage on a pixel electrode must not change by more than ΔV_{pixel}=21 mV. The charge which is leaked through the TFT is equal to $I_{leak}\tau$ where I_{leak} is the average TFT leakage current and τ is the frame time (~16.7 ms, assuming a display refresh rate of 60 Hz). This charge must not

exceed $C_{pixel}\Delta V_{pixel}$. Thus, the maximum TFT leakage current is $C_{pixel}\Delta V_{pixel}/\tau$=**1.26 pA**.

Problem 5:

a) A reflective LCD does not require a backlight and hence it consumes much less power and can be much more lightweight than transmissive LCDs. Also, the brightness of a reflective display naturally adjusts to the ambient lighting.

b) Because the electro-optic characteristics of PDLC are not highly non-linear (ref. Lecture #2 notes), active-matrix addressing is needed in order to achieve good contrast and gray scale performance in high-resolution PDLC displays.