Czochralski Crystal Growth

Crystal Pulling

Crystal Ingots

Shaping and Polishing

300 mm wafer

Seed
Single Silicon Crystal
Quartz Crucible
Water Cooled Chamber
Heat Shield
Carbon Heater
Graphite Crucible
Crucible Support
Spill Tray
Electrode

Professor N Cheung, U.C. Berkeley
Advantage of larger diameter wafers

Chip area larger

Wafer area larger

Chips per Wafer

DRAM generation

1M 4M 16M 64M 256M 1G 4G 16G

100mm 150mm 200mm 300mm 400mm
Large-Diameter Wafer Handling

La Vals Fab

Production Fab

300mm wafer vs pizza

Overhead rail transport of wafer cassette

• Lateral uniformity of processing effects across the WHOLE wafer is key consideration for microfabrication design
Microstructure of Electronic Materials

Amorphous materials

Single-Crystal Material

Polycrystalline Material

Lines show lattice orientation

Grain boundary

Silicide

Nitride spacer

Poly Si

Substrate Si

50nm
Photolithography

Positive Resist

Part exposed to light will be dissolved in development solution.

Processing Temperature *Ambient*
Etching

Pattern resist mask

Etching thin film

Etching completed

Remove resist mask

Anisotropic (e.g. Reactive Ion Etching)

Isotropic (e.g. Wet Etching)

Processing Temperature

Ambient
Etching Selectivity

Example: HF solution etches SiO$_2$ but not Si

* A high etching selectivity is usually desired
"Anisotropic " Wet Etching of Si Crystals

Etchants: KOH or EDP (Ethylene-Diamine_Pyrocatechol)

Top view

Cross-section

Effect of different mask opening

V-pit etched into Si wafer by KOH
Thermal Oxidation

Processing Temperature

\[ 900-1100 \, ^\circ\text{C} \]

\[ \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \]

\[ \text{Si} + 2 \, \text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \]

- \( \text{O}_2 \) (or \( \text{H}_2\text{O} \)) diffuses through \( \text{SiO}_2 \) and reacts with \( \text{Si} \) at the interface to form more \( \text{SiO}_2 \).
- 1\( \mu \)m of \( \text{SiO}_2 \) formed consumes 0.44 \( \mu \)m of \( \text{Si} \) substrate.
- Thin oxide growth (e.g. gate oxide) - use \( \text{O}_2 \). Dry oxidation
- Thick oxide growth (e.g. field oxide) - use \( \text{H}_2\text{O} \). Wet oxidation
Uneven surface topography with window oxidation

Realistic topography with 2-dimensional effect

Note uneven Si surface after window oxidation

Pattern oxide window by litho and etch
Local Oxidation

pad oxide ~100 Å

silicon nitride

Si

Thermal Oxidization

“LOCOS Process”

SiO₂

nitride

Professor N Cheung, U.C. Berkeley
Ion Implantation

typically used to introduce dopants into semiconductors

Ion Energy
~1 keV to 200 keV

Processing Temperature
Room temp during implantation.

After implantation, a 900°C-1000°C anneal step is needed to:
1) activate dopants
2) restore Si crystallinity
Diffusion

- To introduce dopants into semiconductors [Predeposition]
- To spread out the dopant profile [Drive-in]

\[ D = D_0 \cdot e^{-\frac{Q}{kT}} \]

- \( D \): Diffusion Constant
- \( Q \): Activation Energy
- \( T \): Temp in K (\( D \uparrow \) as \( T \uparrow \))

Processing Temperature 950-1200 °C
Predeposition

- Si surface concentration maintained at constant $C_s$ (solid-solubility) during predep.

- Dose of dopant incorporation

$$= \frac{C_s \cdot 2\sqrt{Dt}}{\sqrt{\pi}}$$
Predeposition and Drive-in

• Half-gaussian depth profile after long drive-in.

• Dopant dose \textit{conserved} during drive-in.

• Diffusion distance

\[
\left( \approx \sqrt{Dt} \right)
\]
Physical Vapor Deposition (1)

**Evaporation Deposition**

- **Si Substrate**
- **Substrate at ~ room temp**
- **Deposited Al film (polycrystalline)**
- **evaporation Al charge**

\[(T_{\text{source}} \gg T_{\text{boiling of Al, 700}^\circ\text{C}})\]
**Physical Vapor Deposition (2)**

**Sputtering Deposition**

- **Si Substrate**
- **Ar+**
- **Ar ions with ~ keV kinetic energy**
- **Al target**
- **Substrate at ~ room temp**
- **Deposited Al film (polycrystalline)**
- **Al atoms ejected due to Ar ion bombardment**

Professor N Cheung, U.C. Berkeley
Chemical Vapor Deposition (CVD)

CVD, eg. of Si$_3$N$_4$

Processing Temperature
300-600$^\circ$C

SiCl$_2$H$_2$(v) + NH$_3$(v) $\rightarrow$ Si$_3$N$_4$ + effluent(v)

Si$_3$N$_4$ film

Si Substrate

Solid films are formed by chemical reactions taking place at the surface.
Epitaxial Growth

- Requires an ultra-clean Si surface prior to epi growth.
- Requires deposition of Si at very high temperature for perfect crystallinity.

Processing Temperature
950-1150°C
Epitaxial Growth

Typically used when we need a lightly doped single-crystal Si layer on top of heavily doped substrate.

Example

\[ n^- \text{ Si} \quad \uparrow \quad 10^{15}/\text{cm}^3 \]

\[ n^+ \text{ Si} \quad \text{e.g. } 10^{20}/\text{cm}^3 \]
Cost of Silicon Real Estate

200mm Si wafer 200mm Epi wafer 1812 sq/ft House

Menlo Park, CA

$80 $140 $944,492

$0.25 /cm² $0.44 /cm² $0.56 /cm²
Chemical Mechanical Polishing (CMP)

Wafer is polished using a slurry containing
  • silica abrasives (10-90 nm particle size)
  • etching agents (e.g. dilute HF)

• Backing film provides elasticity between carrier and wafer

• Polishing pad made of polyurethane, with 1 µm perforations
  – rough surface to hold slurry
Metal Plating

Figure 18-7. An electrolytic cell used for copper plating.

~ ambient temp
List of Conventional Microfabrication Modules

- Lithography
- Thermal Oxidation
- Etching (Chemical, Plasma)
- Ion Implantation
- Diffusion
- Physical Vapor Deposition PVD
- Chemical Vapor Deposition CVD and Epitaxial Growth
- Chemical Mechanical Polishing CMP
- Metal Plating
Processing Temperature and Material Failure Temperature

- Si Melting Point (1412°C)
- Al-Si Eutectic (560°C)

Process Temperature in °C

- Resist Exposure
- Resist Spin-on
- Resist Bake
- Evaporation Deposition
- Sputtering Deposition
- CVD
- Ion Implantation
- Post Implantation Anneal
- Thermal Oxidation
- Dopant Diffusion
- Epi

Resist Reflow

- Al-Si Eutectic (560°C)

Processing Temperature and Material Failure Temperature

Professor N. Cheung, U.C. Berkeley 25
Interesting Facts about Chip Manufacturing

• A typical 2-gram silicon chip requires 1.6 kilograms of fossil fuel, 72 grams of chemicals and 32 kilograms of water to manufacture.

• To make the high-grade silicon needed for the chips requires 160 times the energy used to produce raw silicon. This accounts for about half of the total energy used by the chip. Only a quarter is consumed during its processing life.

• Because a chip's components are so tiny and precisely engineered, far more materials, such as fuels and solvents, are needed for their manufacture than for more traditional goods.

• The mass of these secondary materials outweighs the product by a factor of 600. In contrast, making a typical car requires only about twice its weight in fossil fuels.