EE143 General Information

Instructor: Prof. Nathan Cheung, Cory 513, 642-1615, cheung@eecs.berkeley.edu
Lecture Hours and Place: Tu & Th, 9:40-11:00am, Etcheverry 3106
Office Hours: Tu 12-2pm, W 1-2pm, and by appointment via e-mail

Required Text:
1) R.C. Jaeger "Introduction To Microelectronics Fabrication “, 2nd Edition
2) EE143 Reader (if you have S2005 version, no need to buy the F2005 version)

Homework: Weekly homework assignments due on Thursdays.

Grading: Midterm1 15%, Midterm2 15%, Final 30%, Homework 10%, Lab 30%
(undergrad and grad will be graded as two separate groups)

***Browse last semester's course content for lecture notes, homework, and exams. http://www-inst.eecs.berkeley.edu/~ee143/sp05index.html
Lab Sign-up required for ALL students
6 Lab Sections : M2-5pm, W 9-12am, W 2-5pm,
Th 2-5pm, Fri 9-12am, Fri 2-5pm

• Sign-up sheets will be posted outside Cory 218 after 11am (8/31, Tue) .You have to sign up personally at Cory 218 before 5pm (9/1, Thur) even you are enrolled by Telebear. If you do not do so, your name will be removed from the class list
• Final lab assignment will be posted outside Cory 218 and on class webpage on 9/2 (Friday).
• Assignment priority : (1) Telebear enrolled, (2) Telebear waitlist , (3) No Telebear enrollment. Order of sign-up not important.
• NO Lab Meeting the week of 8/29
Week of 9/5

Mandatory Lab attendance required.

• You will have lab orientation and have to pass a safety quiz.

• Because of Labor Day Holiday, there will be no Monday afternoon lab section. Students assigned to that section can attend any of the other 5 sections (only for this week).
Lectures, HW, Lab Info, and News (check regularly)
http://www-inst.eecs.berkeley.edu/~ee143/

Other Websites for EE143 Overview

Device Physics/ Process Visualization – Highly recommended
(Change the device parameters and watch the resultant
space charge, energy bands , I-V , C-V etc)
http://jas.eng.buffalo.edu/

MEMS operation  (Good collection of  photos and movies)

SIA Roadmap (Trend and Challenge)
http://public.itrs.net/

EE Basics (E40 course material)
http://www-inst.eecs.berkeley.edu/~ee40/

Trends and forecast
www.icknowledge/com
What is EE143 all about?

- Microfabrication Principles for IC and MEMS
- Hands-on Fabrication and Testing of IC and MEMS Devices
Principle of Monolithic Process Integration

* A sequence of **Additive** and **Subtractive** steps with **lateral patterning**

Example: CMOS Integrated Circuit
A Process Module has many sub-steps!

Example: Deep UV Photolithography

1) Surface Prime
- Dispense a controlled amount of photoresist
- Allow the photoresist to spread across the wafer
- Rapidly ramp-up the coater spin speed throwing off excess photoresist
- Spin at high speed to form a thin dry film of photoresist

2) Coat

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4) Expose
3) Pre-bake
5) Post Exposure Bake
7) Hard Bake

6) Develop

Dispense a puddle of developer and allow it to sit.
Dispense a rinse solution while slowly spinning the wafer.
Ramp up to high speed and spin the wafer dry.
SEM Micrographs of EE143 Chip
EE143 Chip Characterization

17-stage Ring Oscillator

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Process Simulation

* 3D Topography and Dopant Distribution

After resist patterning on nitride/pad oxide

After Local Oxidation

After Poly-Si Gate Patterning

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1 μm = 10^{-4} \text{ cm} = 10^{-6} \text{ m} = 1000 \text{ nm}

State-of-the-art Mass Production IC

Diameter of human hair ~50 μm

~ 200 Transistors
Advantages of Technology Scaling

- More dies per wafer, lower cost
- Higher-speed devices and circuits (electrical signals travel shorter distances)

<table>
<thead>
<tr>
<th>Generation:</th>
<th>1.5µ</th>
<th>1.0µ</th>
<th>0.8µ</th>
<th>0.6µ</th>
<th>0.35µ</th>
<th>0.25µ</th>
</tr>
</thead>
</table>
The beauty of silicon

For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by

1. Scaling device dimensions downward

2. Scaling wafer diameter upward

<table>
<thead>
<tr>
<th></th>
<th>1990</th>
<th>1995</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAMs</td>
<td>4 MB</td>
<td>64 MB</td>
<td>1 GB</td>
</tr>
<tr>
<td>Feature size</td>
<td>0.8 μm</td>
<td>0.35 μm</td>
<td>0.15 μm</td>
</tr>
<tr>
<td>Wafer diameter</td>
<td>6”</td>
<td>8”</td>
<td>12”</td>
</tr>
<tr>
<td>Cost per Megabit</td>
<td>$6.50</td>
<td>$3.14</td>
<td>$0.10</td>
</tr>
</tbody>
</table>
Transistor Per Integrated Circuit Trends

Moore’s law: "The complexity for minimum component cost has increased at a rate of roughly a factor of two per year" [5], later amended to doubling every 18 to 24 months.

Another Perspective on Moore’s Law

… we are already producing $10^{18}$ transistors per year. Enough to supply every ant on the planet with ten transistors.

Twenty years from now, if the trend continues, there will be more transistors than there will be cells in the total number of human bodies on Earth.
5nm-Gate Nanowire FinFET

2004 Symposium on VLSI Technology, p.196

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# SIA roadmap

[http://public.itrs.net/](http://public.itrs.net/)

## Memory and Logic Technology Requirements

<table>
<thead>
<tr>
<th>Year of First Product Shipment Technology Generation</th>
<th>1999 180nm</th>
<th>2001 150nm</th>
<th>2003 130nm</th>
<th>2006 100nm</th>
<th>2009 70nm</th>
<th>2012 50nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. Logic $V_{dd}$ ($V$)</td>
<td>1.8-1.5</td>
<td>1.5-1.2</td>
<td>1.5-1.2</td>
<td>1.2-0.9</td>
<td>0.9-0.6</td>
<td>0.6-0.5</td>
</tr>
<tr>
<td>$T_{ox}$ Equivalent (nm)</td>
<td>3-4</td>
<td>2-3</td>
<td>2-3</td>
<td>1.5-2</td>
<td>&lt;1.5</td>
<td>&lt;1.0</td>
</tr>
<tr>
<td>Equivalent Maximum E-field (MV/cm)</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>&gt;5</td>
<td>&gt;5</td>
<td>&gt;5</td>
</tr>
<tr>
<td>Nominal $I_{on}$ @ 25°C ($\mu$A/$\mu$m) (NMOS/PMOS)</td>
<td>600/280</td>
<td>600/280</td>
<td>600/280</td>
<td>600/280</td>
<td>600/280</td>
<td>600/280</td>
</tr>
<tr>
<td>$S/D$ Extension Junction Depth, Nominal (nm)</td>
<td>36-72</td>
<td>30-60</td>
<td>26-52</td>
<td>20-40</td>
<td>15-30</td>
<td>10-20</td>
</tr>
</tbody>
</table>
Chip Power consumption is a big concern !!!!

Source: Intel Developer Forum 2002
MEMS: Pressure Transducer

**Bulk Micromachining**

![Bulk Micromachining Diagram]

**Surface Micromachining**

![Surface Micromachining Diagram]

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MEMS Actuators

Gear Speed Reduction Unit

Movable Mirror

Responsive Drug Delivery Valve

Turbine engine

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Commercial MEMS Products

- Optomechanical Displays (TI, 1996)
- Accelerometer (Analog Devices)
MEMS-IC Integration
(Sandia National Lab)

- MEMS fabricated in 12µm-deep trench
  - Filled with SiO₂ and planarized using CMP

SNL Integrated Micromechanical / CMOS
Silicon-COMPATIBLE OPToelectronics (SCOOP)

Si-BASED WAVEGUIDES

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‘Snail' neuron grown atop an Infineon Technologies CMOS device that measures the neuron's electrical activity, linking chips and living cells.

Source: Max Planck Institute
Artificial Silicon Retina™ (ASR)

2mm, 1/1000” thick

http://www.optobionics.com/index.htm
Heterogeneous Integration of Microsystems
Professor Nathan Cheung, EECS

Si-Ge high mobility electronics

Encapsulated battery with switch/LED

Encapsulated Power source

InGaN LEDs on Si

Si microfluidic channels

GeOI

BioMEMS Emitters /Filter/Detectors

Green LED
Blue LED

Optical Modulator

MOS IC

Micro pump

LED display

Laser Emitter Arrays

Micro-fluidic channels

5mm

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Extension of Si Technology

Si circuits on plastic

Si Laser (Intel)
(i) Co-axial heterostructure nanowire (COHN); (ii) longitudinal heterostructure nanowire (LOHN).