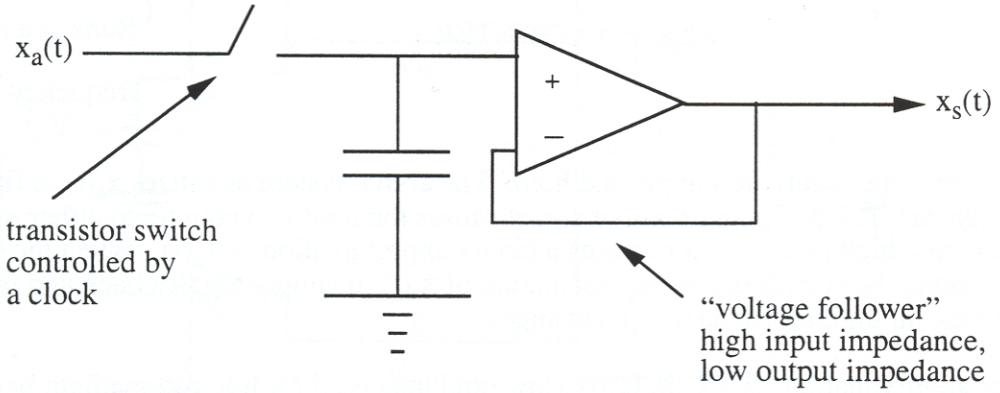
A/D and D/A Circuits

A/D consists of sample and hold followed by a quantizer.

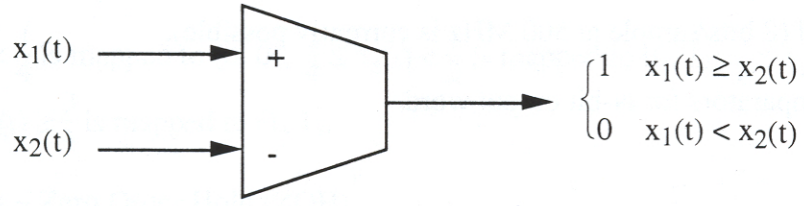
In catalogs, just the quantizer is called an A/D (unless A/D is referred to as a "sampling A/D"). As we shall see, the sample and hold is very simple, whereas the quantizer is much more complicated.

Sample and Hold:



A/D (Quantizer)

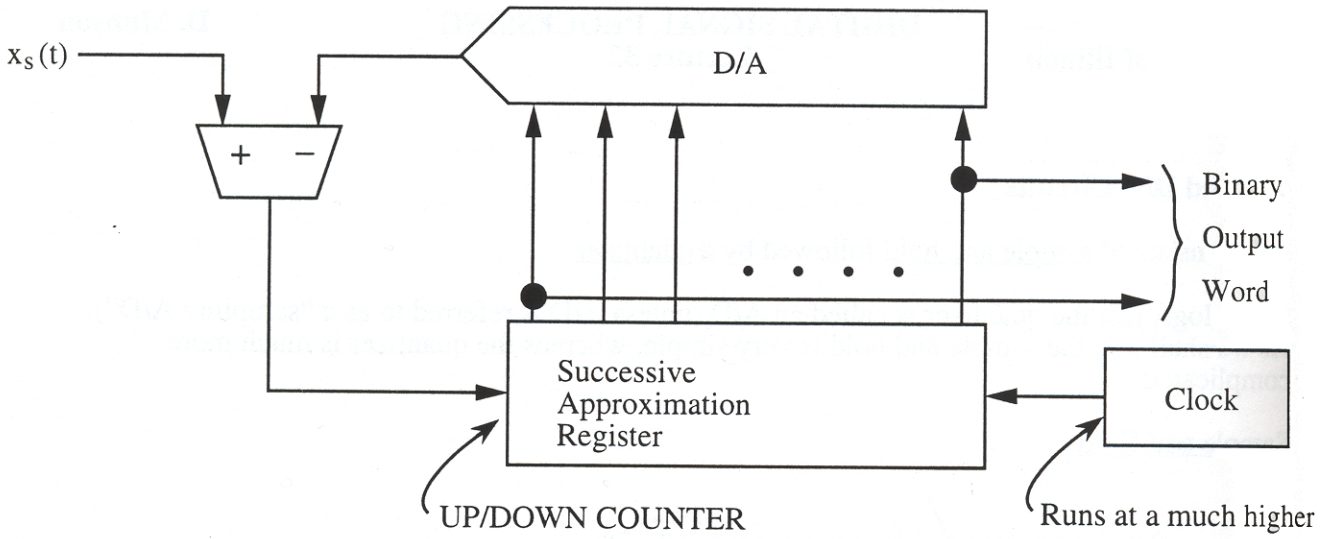
Uses comparators:



Two popular types of A/D's:

a) Successive Approximation

~ for low and medium sampling rates; uses a D/A!



Here, $x_s(t)$ is the input from the sample and hold. The above system quantizes $x_s(t)$ to fit into a computer register. The comparator output signal causes the up-down counter to either increment or decrement, at a high rate, until it contains a binary approximation of $x_s(t)$. When the counter has settled around the correct digital representation of $x_s(t)$, it simply toggles back and forth in its least significant bit until the value of $x_s(t)$ changes.

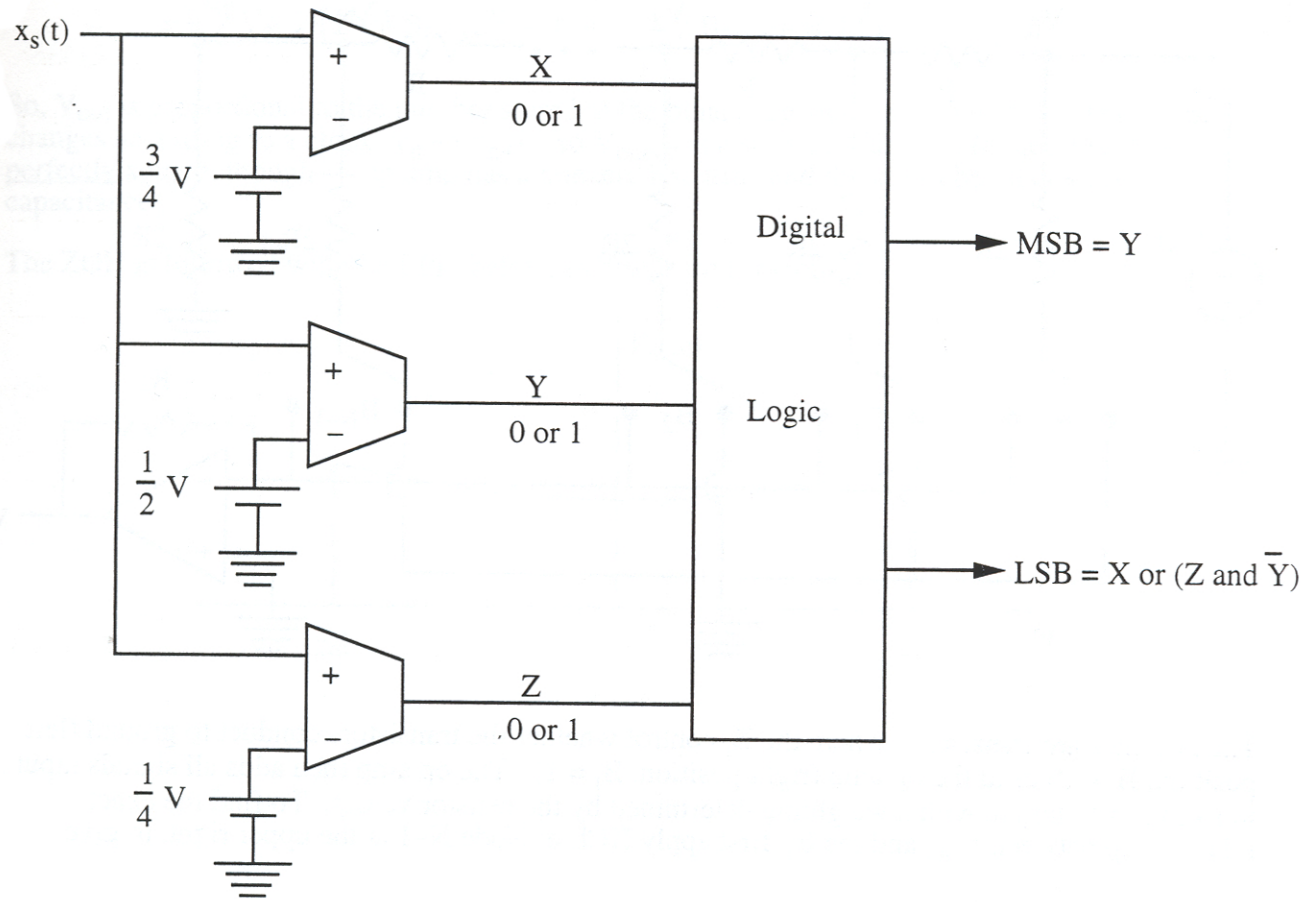
Succcessive approximation A/D's are fairly slow (and thus used for low and medium bandwidth applications) because it may take several clock cycles for the counter to settle on a new value of $x_s(t)$.

b) Parallel or Flash A/D

For high speed (8 bits/sample at 500 MHz is currently possible).

Uses 2^N-1 comparators for N-bit output word.

Example 2 bit quantizer:

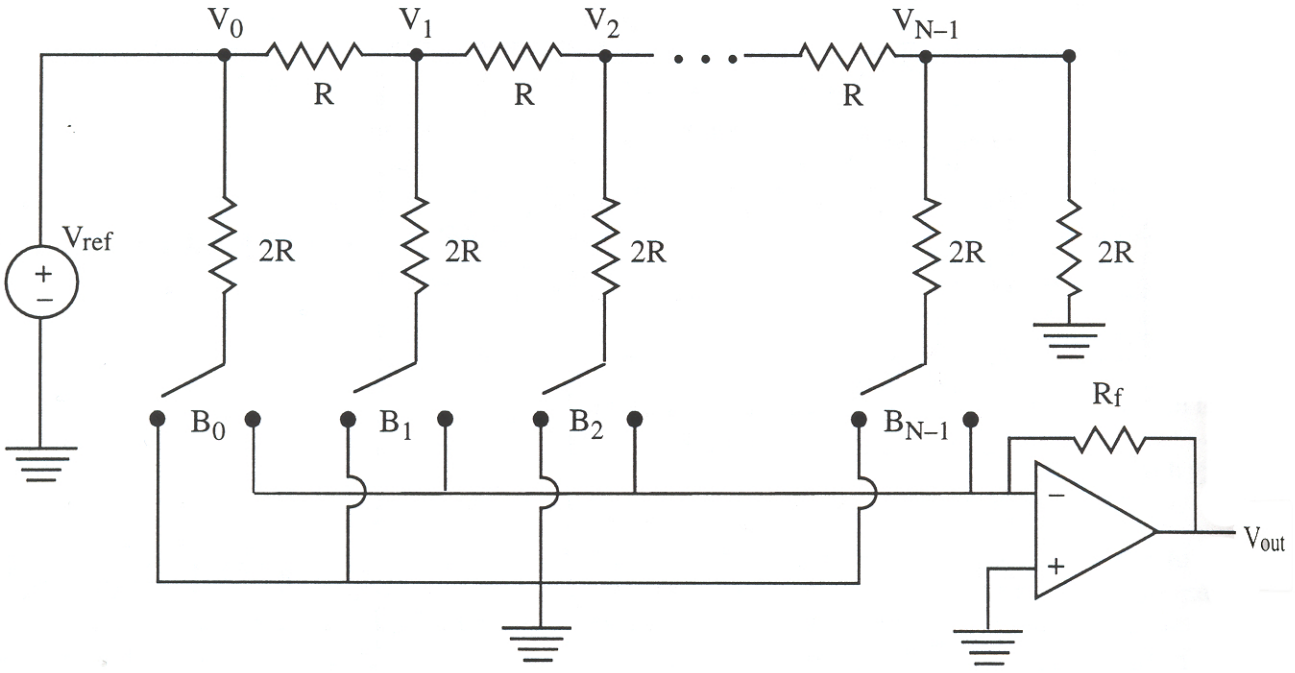


Here, $0 \le x_s(t) < \frac{1}{4}$ is mapped to (0, 0), $\frac{1}{4} \le x_s(t) < \frac{1}{2}$ is mapped to (0, 1), $\frac{1}{2} \le x_s(t) < \frac{3}{4}$ is mapped to (1, 0), and $x_s(t) \ge \frac{3}{4}$ is mapped to (1, 1).

D/A Converters ~ Zero Order Hold (ZOH)

The contents of a binary register containing y_n are the input to a D/A.. Let $[B_0, B_1, B_2, \ldots, B_{N-1}]$ be the binary representation of y_n. The B_i change with period T as y_{n+1} replaces y_n in the D/A input register.

One popular type of D/A uses a resistor ladder (can also use a capacitor ladder):



The switches are transistors, where the B_i control whether the transistors conduct to ground (left position, $B_i = 0$) or to the op amp (right position, $B_i = 1$). The op amp then adds all signals input to its minus terminal, with a weighting determined by the resistor values. To find the exact relationship between V_{out} and the B_i, first apply KCL at Node N–1 at the upper right, to give:

$$\frac{V_{N-1}}{2R} + \frac{V_{N-1}}{2R} + \frac{V_{N-1} - V_{N-2}}{R} = 0$$

$$\Rightarrow V_{N-1} + V_{N-1} - V_{N-2} = 0 \Rightarrow V_{N-2} = 2\,V_{N-1}$$

Similarly: $V_{n-1} = 2V_n \quad n = 1, 2, \ldots, N-2$

$$\Rightarrow V_n = V_{N-1}\,2^{N-1-n}$$

Using KCL at the minus terminal of the op amp gives:

$$\frac{1}{2R} \sum_{i=0}^{N-1} B_i\,V_i = \frac{0 - V_{out}}{R_f}$$

where each B_i is 0 or 1.

$$\Rightarrow \quad V_{out} = \frac{-R_f}{2R} \sum_{i=0}^{N-1} B_i \, V_{N-1} \, 2^{N-1-i}$$

$$= \frac{-R_f}{2R} V_{N-1} \left[2^{N-1} B_0 + 2^{N-2} B_1 + \ldots + 2 B_{N-2} + B_{N-1} \right]$$

So, V_{out} is proportional to the number stored in the binary register representing y_n. This number changes according to a clock ($y_n \rightarrow y_{n+1}$), so $V_{out}(t)$ is a staircase function (edges won't be perfectly square, though — op amp has a nonzero rise time and there will be other stray capacitance).

The ZOH is followed with the LPF, below, as discussed previously.