# CS250
# VLSI Systems Design

# Lecture 5: Physical Realities: Beneath the Digital Abstraction, Part 2: Power & Energy

Spring 2016

John Wawrzynek
with
Chris Yarp (GSI)

**Thanks to John Lazaro for the slides**

The Watt: Unit of power. A rate of energy (J/s). A gas pump hose delivers 6 MW.
The Joule: Unit of energy. A 1 Gallon gas container holds 130 MJ of energy.
120 KW: The power delivered by a Tesla Supercharger. Tesla Model S has a 306 MJ battery (good for 265 miles).
1 J = 1 W * s 1 W = 1 J/s.
RANGE ROVER

**Sad fact:** Computers turn electrical energy into heat. Computation is a byproduct.

# Energy and Performance

Air or water carries heat away, or chip melts.

UC Regents Spring 2016 © UCB

The Joule: Unit of energy. Can also be expressed as Watt-Seconds. Burning 1 Watt for 100 seconds uses 100 Watt-Seconds of energy.

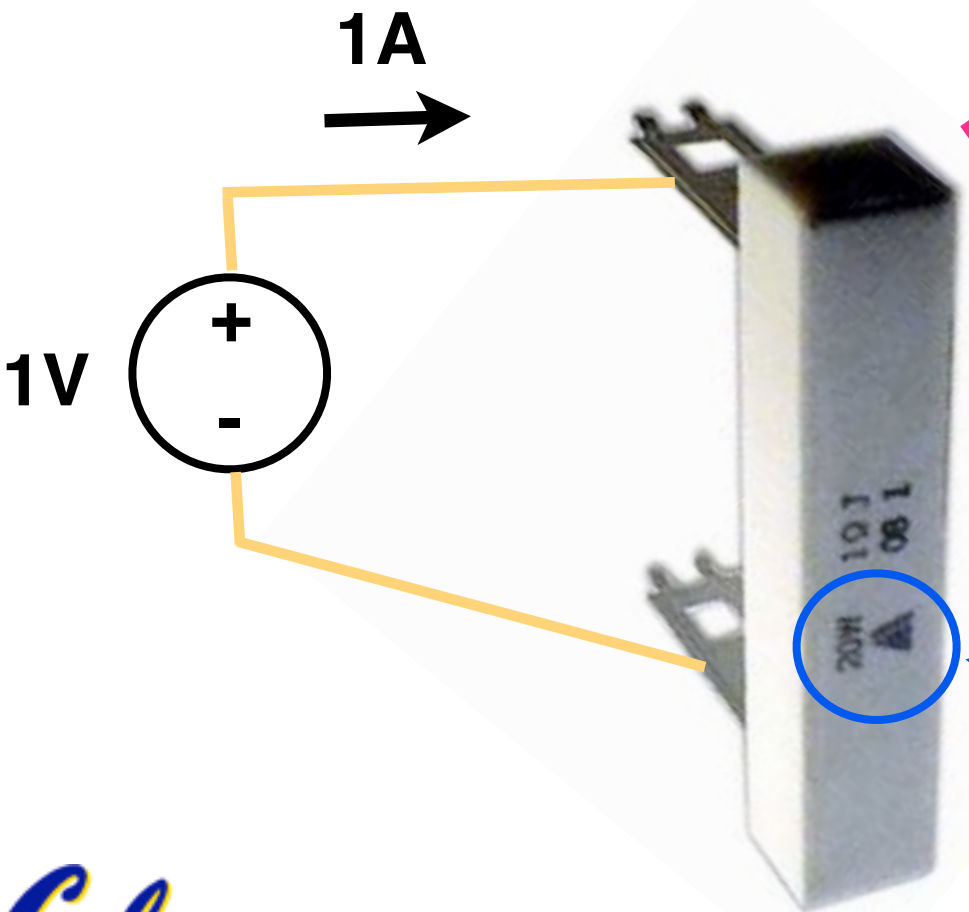
This is how electric tea pots work ...

1 Joule heats 1 gram of water 0.24 degree C

1 Joule of Heat Energy per Second

1 Watt

The Watt: Unit of power. The amount of energy burned in the resistor in 1 second.




1 Ohm Resistor

20 W rating: Maximum power the package is able to transfer to the air. Exceed rating and resistor burns.



UC Regents Spring 2016 © UCB

# Cooling an iPod nano ...

**Like resistor on last slide, iPod relies on passive transfer of heat from case to the air.**

Why? Users don't want fans in their pocket ...

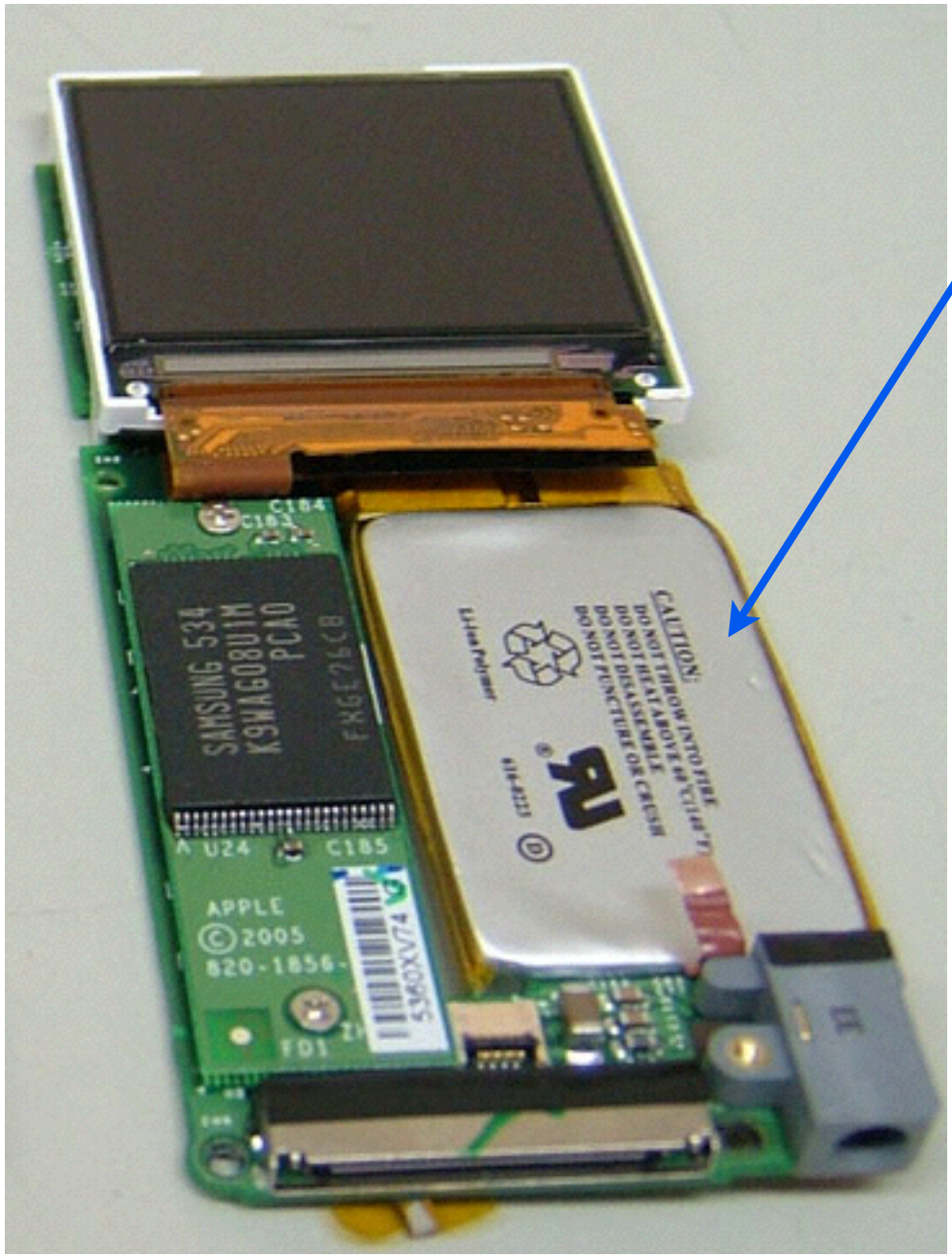
**To stay "cool to the touch" via passive cooling, power budget of 5 W.**

If iPod nano used 5W all the time, its battery would last 15 minutes ...



UC Regents Spring 2016 © UCB

# Powering an iPod nano (2005 edition)




1.2 W-hour battery:
Can supply 1.2 watts
of power for 1 hour.

1.2 W-hr / 5 W ≈ 15 minutes.

More W-hours require bigger battery
and thus bigger "form factor" --
it wouldn't be "nano" anymore :-).

**Real specs for iPod nano :**

**14 hours for music,**
**4 hours for slide shows.**

85 mW for music.
300 mW for slides.



UC Regents Spring 2016 © UCB

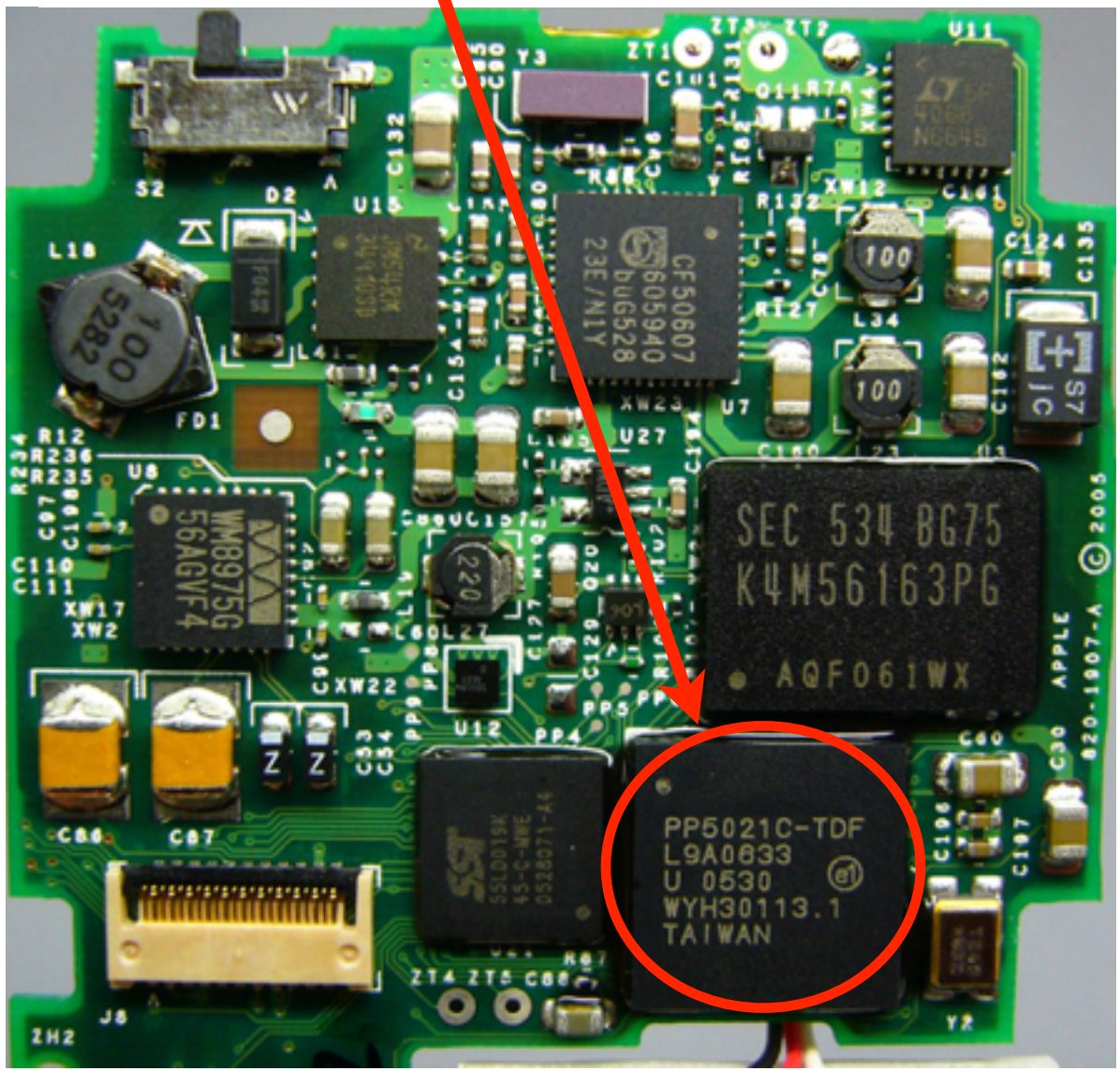
# Finding the (2005) iPod nano CPU ...

portalplayer™

A close relative ...

**PP5020**

digital media management system-on-chip




Two 80 MHz CPUs. One CPU used for audio, one for slides.

Low-power ARM roughly 1mW per MHz ... variable clock, sleep modes.

85 mW system power realistic ...



UC Regents Spring 2016 © UCB

# What's happened since 2005?

2010 nano

**0.74 ounces (50% of 2005 Nano)**

**0.39 W Hr (33% of 2005 Nano)**

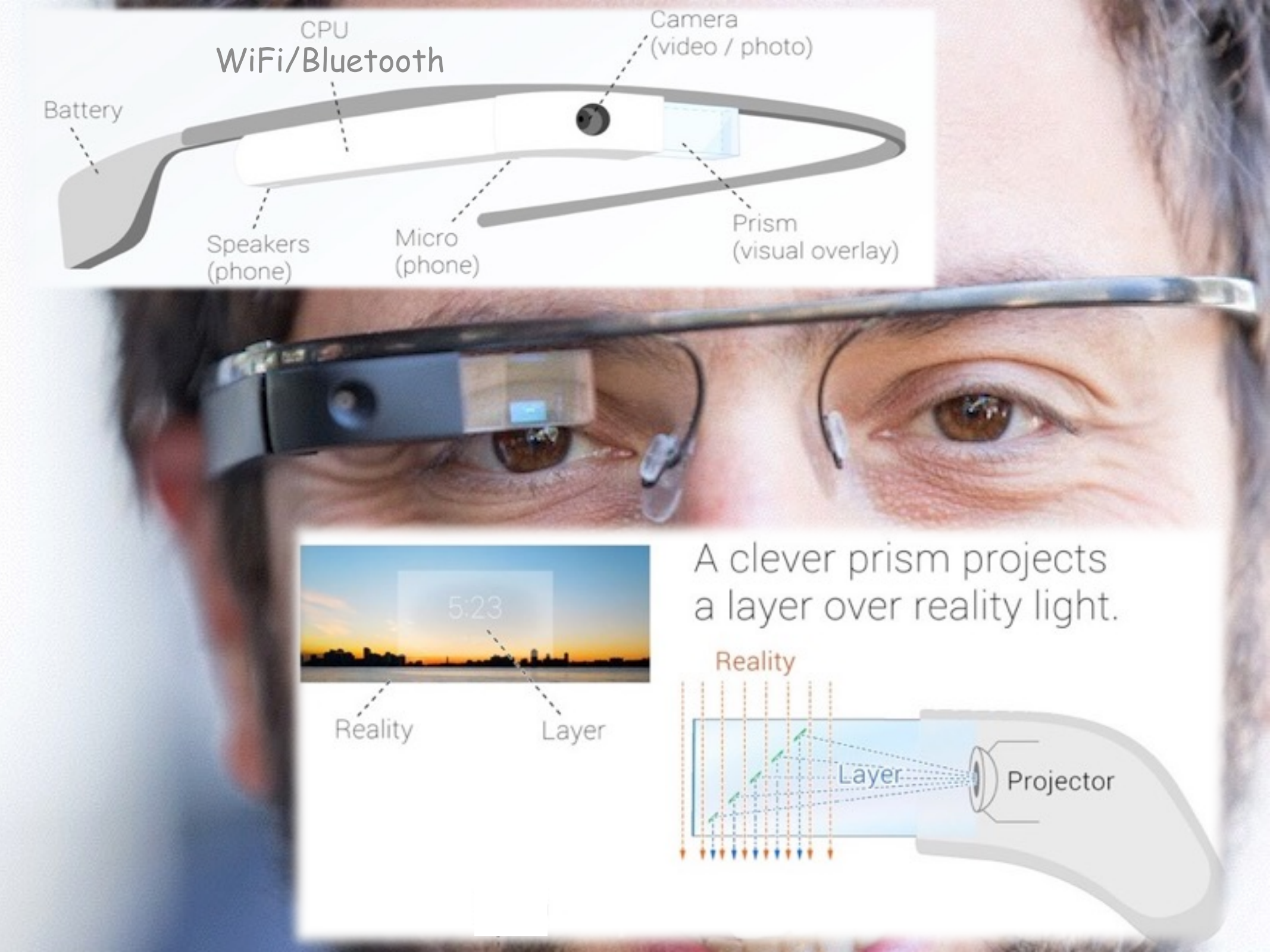
"Up to" 24 hours audio playback.

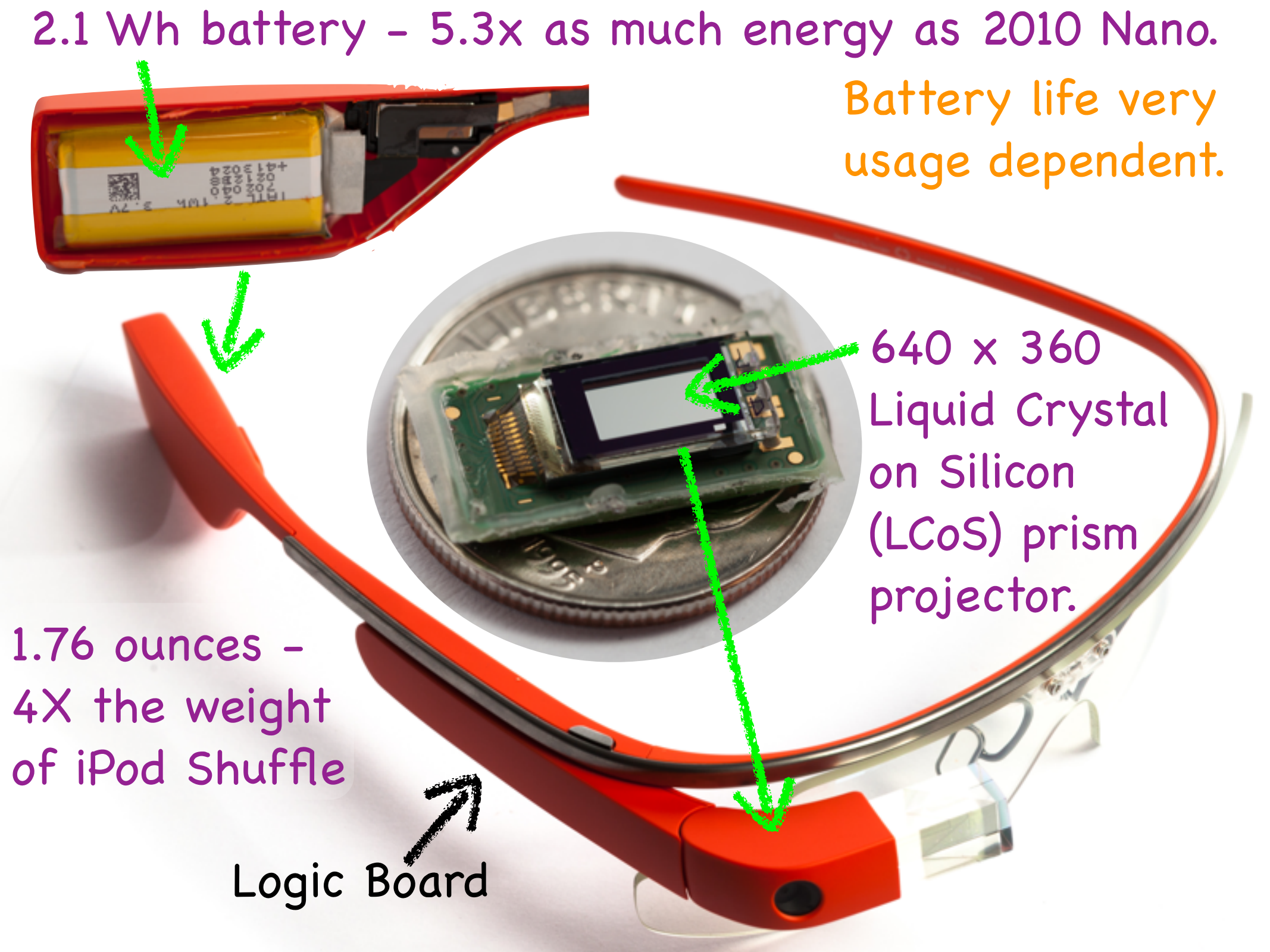
70% improvement from 2005 nano.

2015

# Apple Watch

**3.8 V, 0.78 Wh lithium-ion battery on 38mm model. Apple claims the 205 mAh battery should provide up to 18 hours of use (which translates to 6.5 hours of audio playback, 3 hours of talk time, or 72 hours of Power Reserve mode.)**


CPU
WiFi/Bluetooth
Camera
(video / photo)
Battery
Speakers
(phone)
Micro
(phone)
Prism
(visual overlay)
5:23
Reality
Layer
A clever prism projects
a layer over reality light.
Reality
Layer
Projector


2.1 Wh battery - 5.3x as much energy as 2010 Nano.
Battery life very usage dependent.
640 x 360 Liquid Crystal on Silicon (LCoS) prism projector.
1.76 ounces - 4X the weight of iPod Shuffle
Logic Board

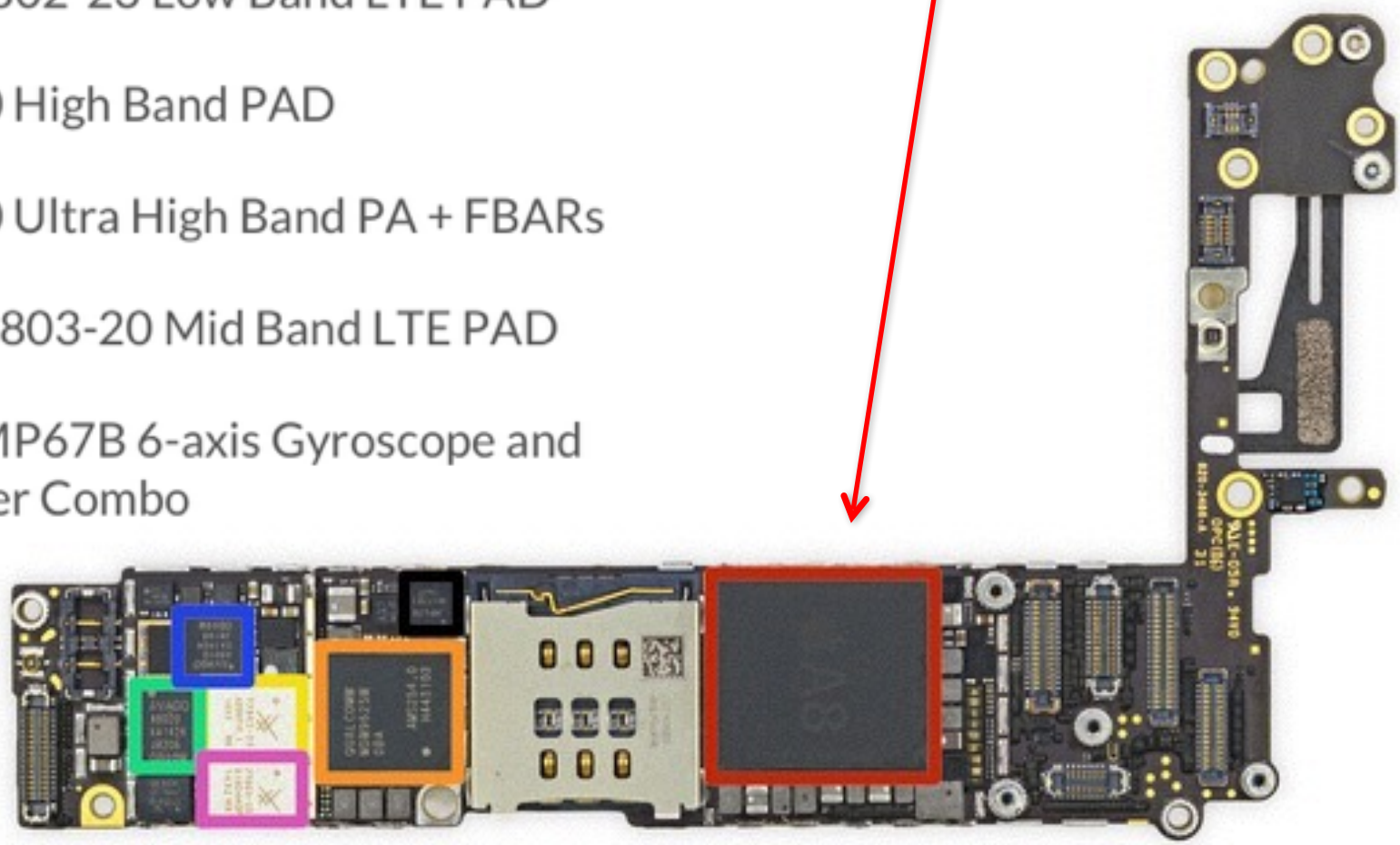
# iPhone6

## 4.7 inch iPhone6: 1,810mAh battery

## iPhone 5s: 1570mAh

- The front side of the logic board:
  - Apple A8 APL1011 SoC + SK Hynix RAM as denoted by the markings H9CKNNN8KTMRWR-NTH (we presume it is 1 GB LPDDR3 RAM, the same as in the iPhone 6 Plus)
  - Qualcomm MDM9625M LTE Modem
  - Skyworks 77802-23 Low Band LTE PAD
  - Avago A8020 High Band PAD
  - Avago A8010 Ultra High Band PA + FBARs
  - SkyWorks 77803-20 Mid Band LTE PAD
  - InvenSense MP67B 6-axis Gyroscope and Accelerometer Combo

The A8 is manufactured on a 20 nm process by TSMC. It contains 2 billion transistors. Its physical size is 89 mm^2. [ ] It has 1 GB of LPDDR3 RAM included in the package. It is dual core, and has a frequency of 1.38 GHz.



# Notebooks ... as designed in 2006 ...

2006 Apple MacBook -- 5.2 lbs

- **Performance:** Must be "close enough" to desktop performance ... most people no longer used a desktop (even in 2006).
- **Size and Weight.** Ideal: paper notebook.
- **Heat:** No longer "laptops" -- top may get "warm", bottom "hot". Quiet fans OK.


UC Regents Spring 2016 © UCB

# Battery: Set by size and weight limits ...

46x more energy than iPod nano battery. And iPod lets you listen to music for 14 hours!

Battery rating: 55 W-hour.

At 2.3 GHz, Intel Core Duo CPU consumes 31 W running a heavy load - under 2 hours battery life! And, just for CPU!

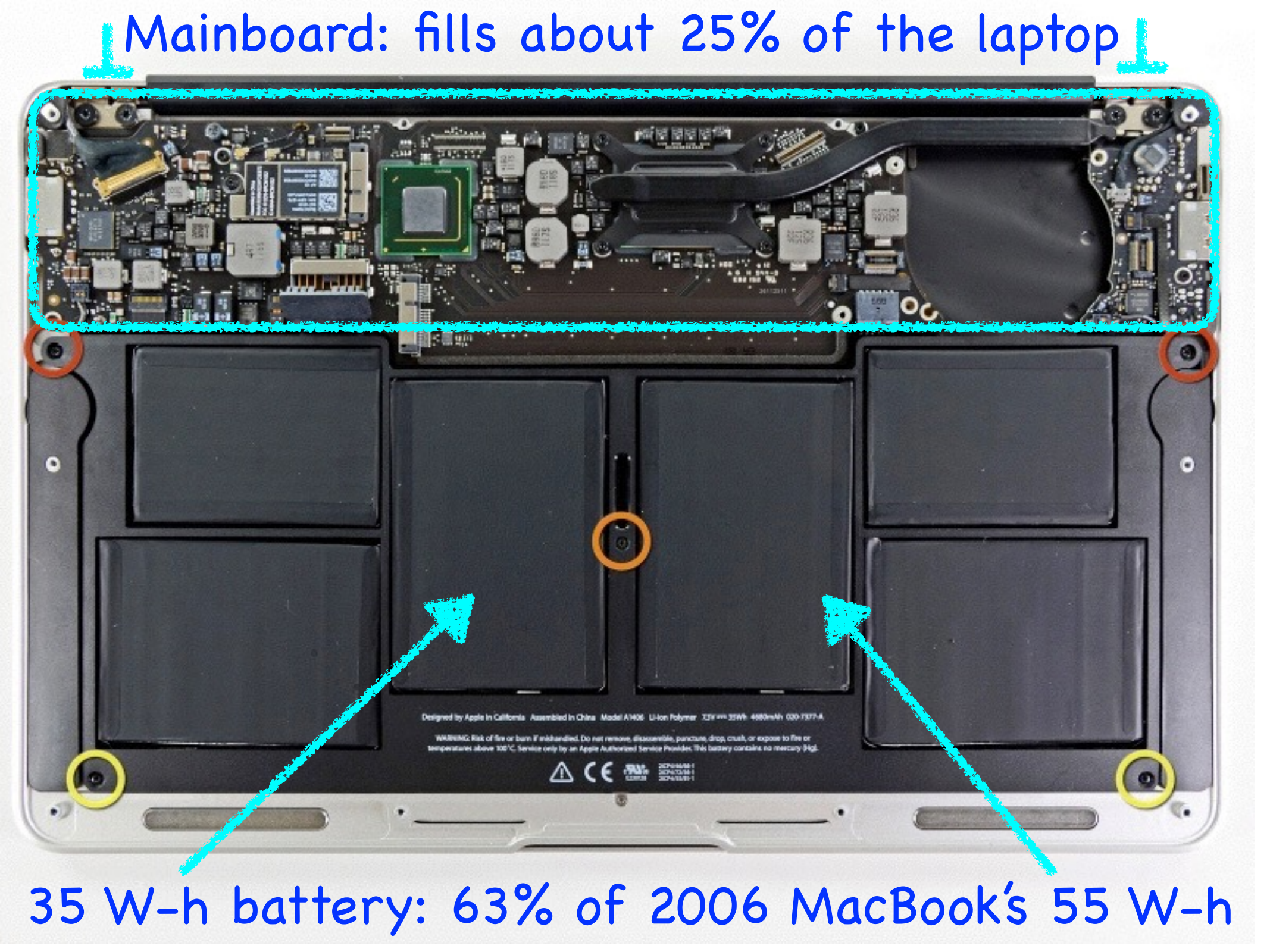
Almost full 1 inch depth. Width and height set by available space, weight.

At 1 GHz, CPU consumes 13 Watts. "Energy saver" option uses this mode ...

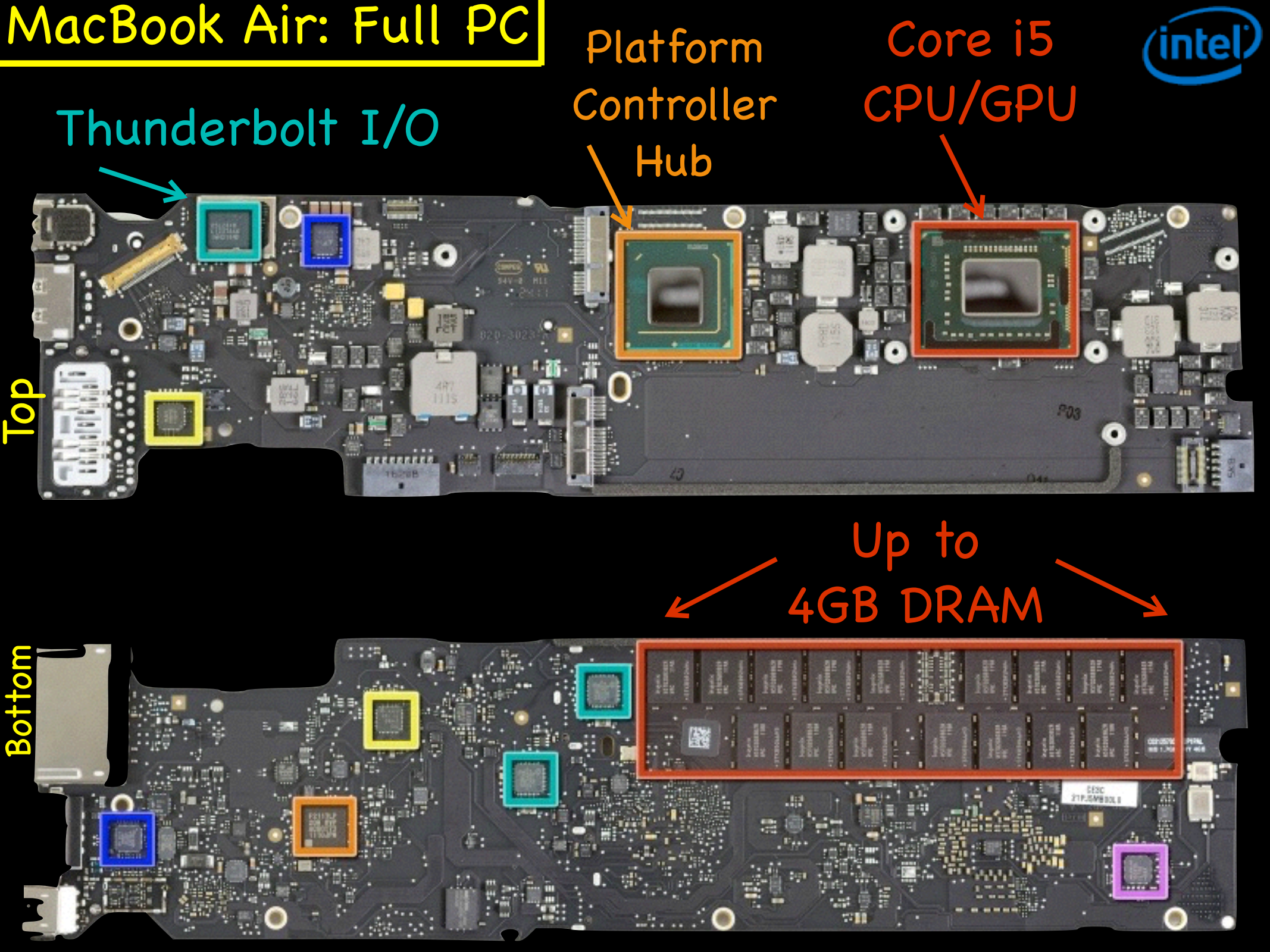


UC Regents Spring 2016 © UCB

# MacBook Air … design the laptop like an iPod


Mainboard: fills about 25% of the laptop
35 W-h battery: 63% of 2006 MacBook's 55 W-h

# MacBook Air: Full PC



# Servers: Total Cost of Ownership (TCO)

Machine rooms are expensive. Removing heat dictates how many servers to put in a machine room.

Electric bill adds up! Powering the servers + powering the air conditioners is a big part of TCO.

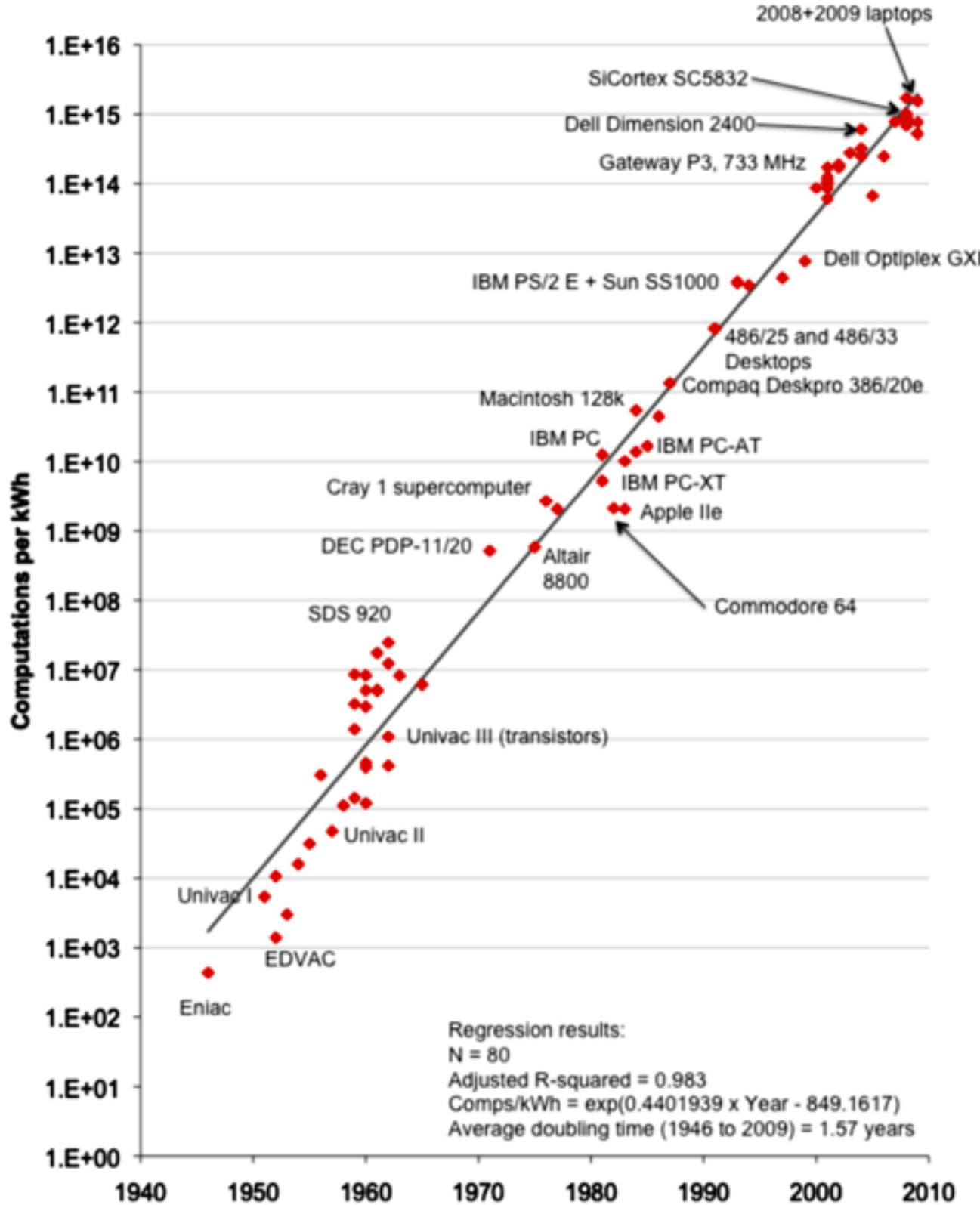
Reliability: running computers hot makes them fail more often.



UC Regents Spring 2016 © UCB

Computations per W-h doubles every 1.6 years, going back to the first computer.

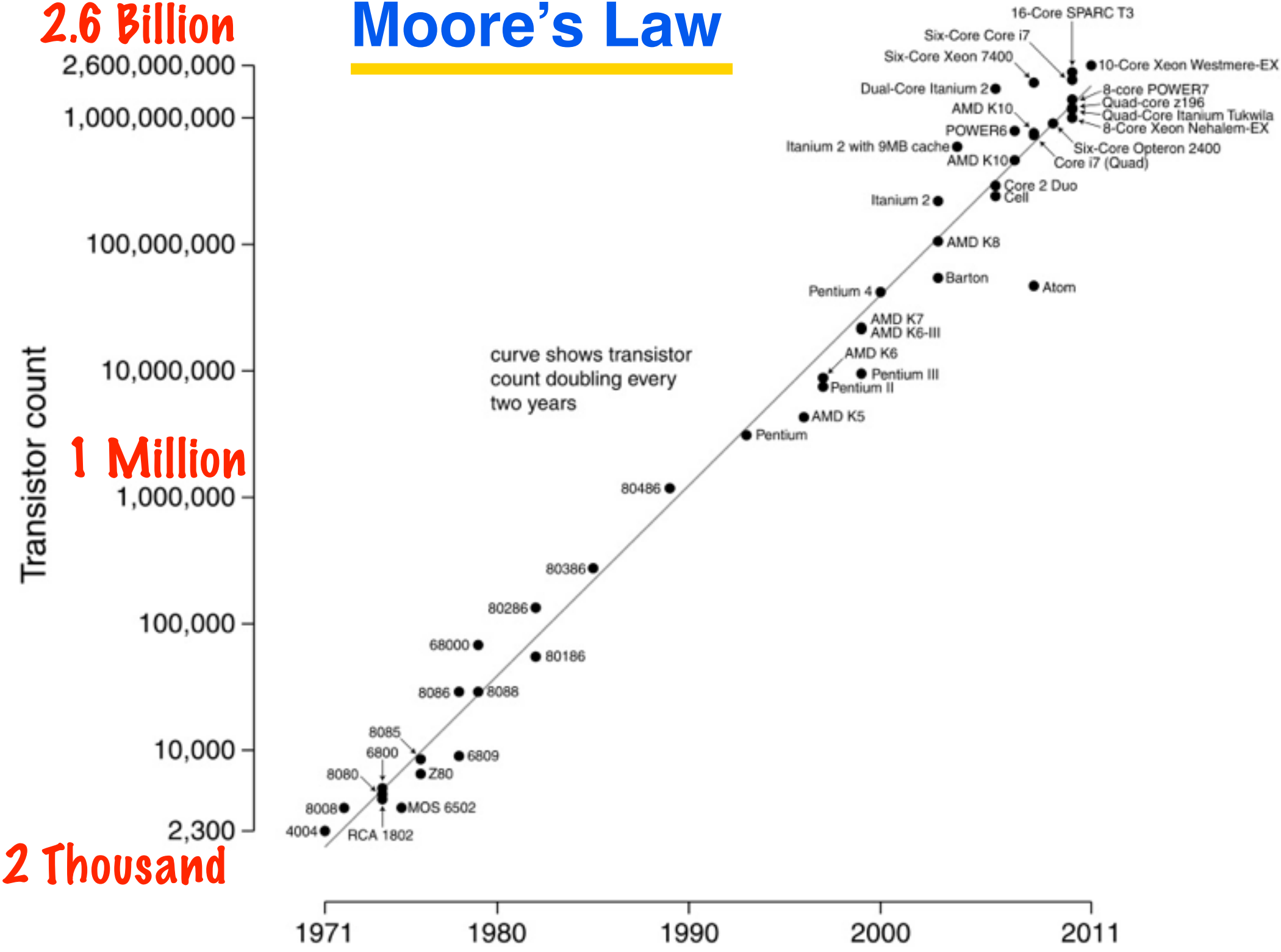
(Jonathan Koomey, Stanford).



# Processors and Energy

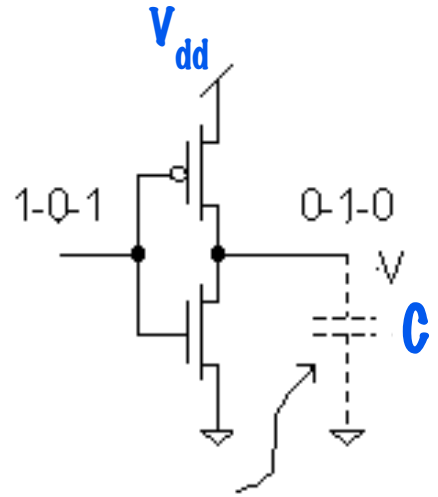
UC Regents Spring 2016 © UCB

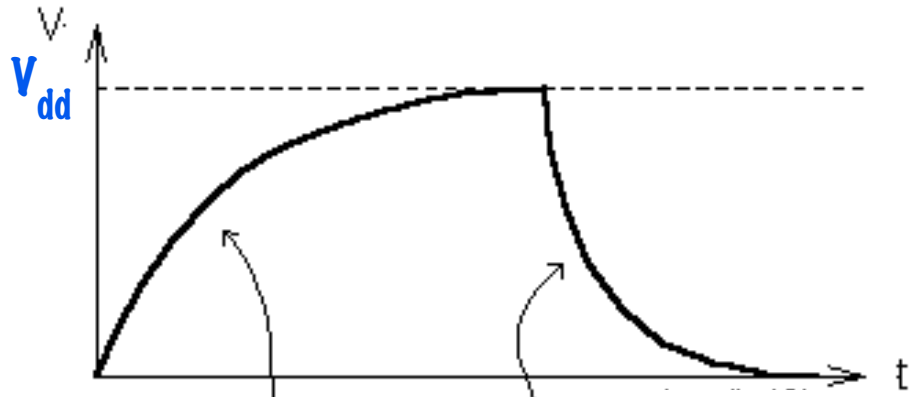
# Moore's Law


2.6 Billion
1 Million
2 Thousand
Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
1971
1980
1990
2000
2011
curve shows transistor count doubling every two years
16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
AMD K10
Quad-Core Itanium Tukwila
POWER6
8-Core Xeon Nehalem-EX
Itanium 2 with 9MB cache
Six-Core Opteron 2400
AMD K10
Core i7 (Quad)
Core 2 Duo
Cell
Itanium 2
AMD K8
Barton
Atom
Pentium 4
AMD K7
AMD K6-III
AMD K6
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
6809
Z80
8080
8008
MOS 6502
4004
RCA 1802

# Switching Energy: Fundamental Physics

## Every logic transition dissipates energy.




$$E_{0\to1} = \frac{1}{2} C V_{dd}^2 \qquad E_{1\to0} = \frac{1}{2} C V_{dd}^2$$

Strong result: Independent of technology.

**How can we limit switching energy?**

(1) Reduce # of clock transitions. But we have work to do ...

(2) Reduce Vdd. But lowering Vdd limits the clock speed ...

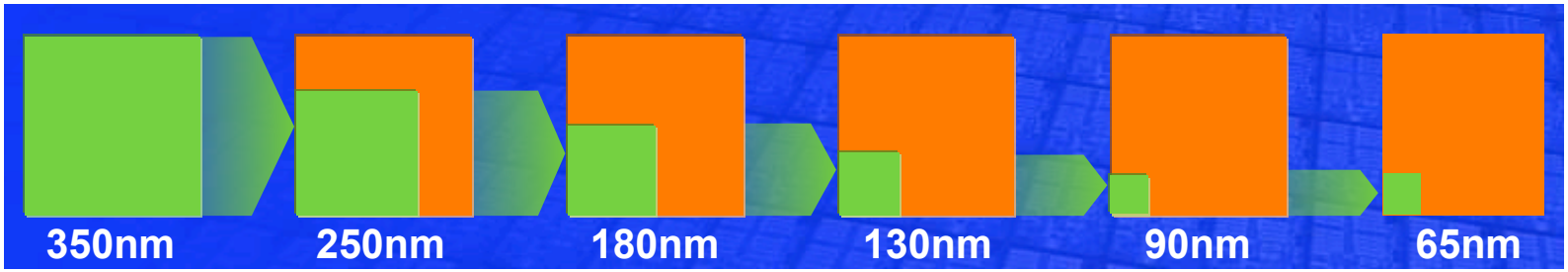
(3) Fewer circuits. But more transistors can do more work.

(4) Reduce C per node. One reason why we scale processes.

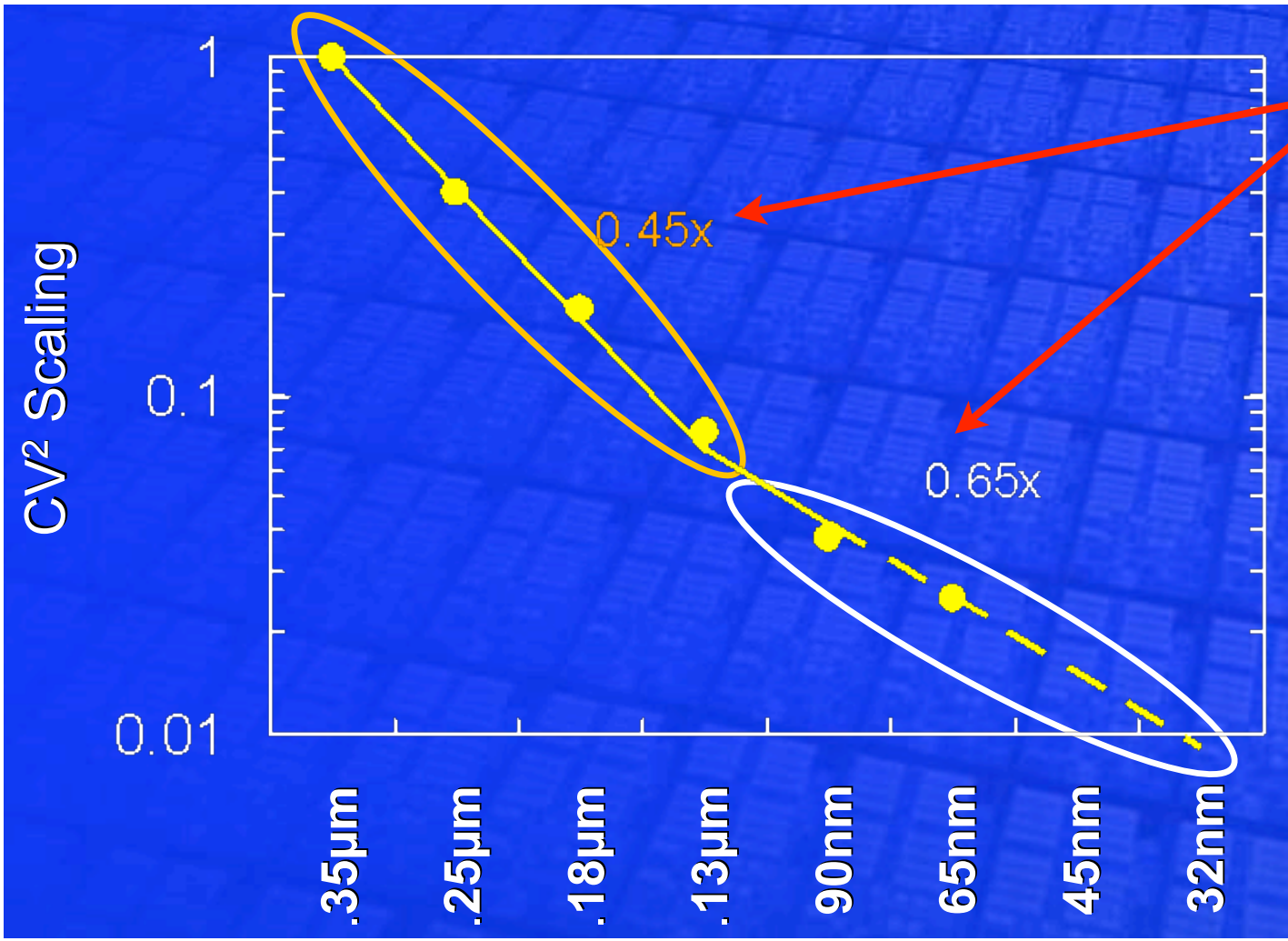


UC Regents Spring 2016 © UCB

# Scaling switching energy per gate ...




IC process scaling ("Moore's Law")




Due to reducing V and C (length and width of Cs decrease, but plate distance gets smaller).

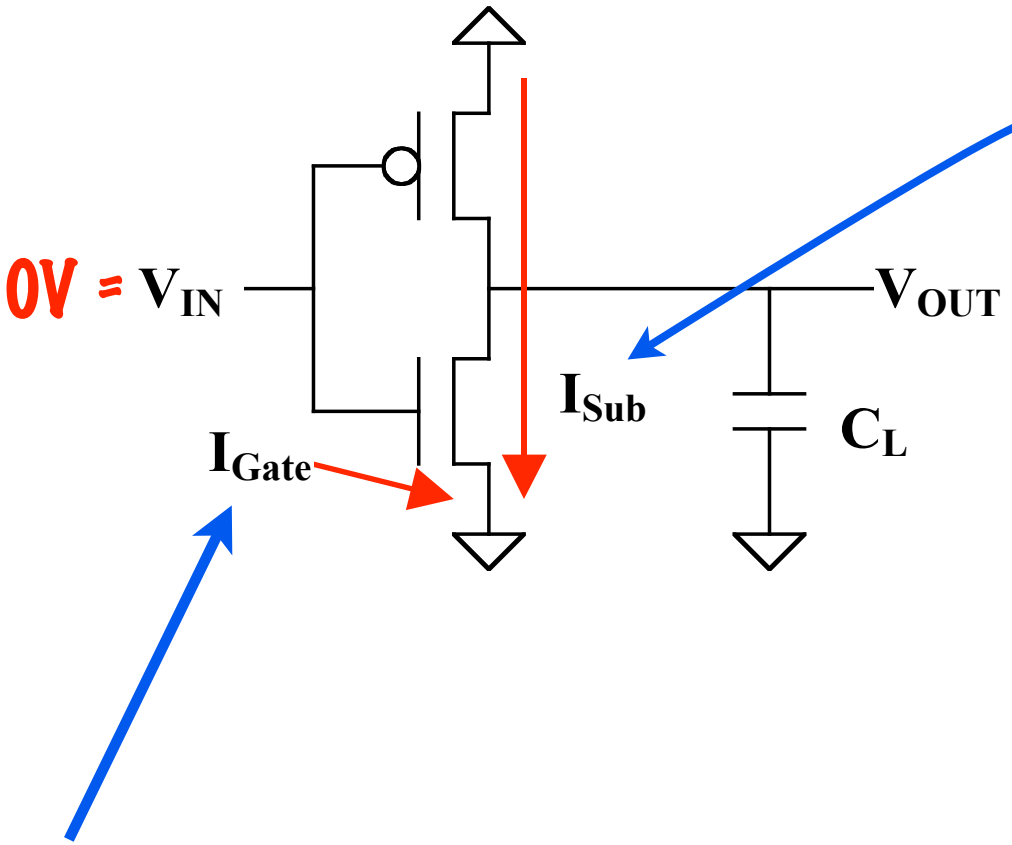
Recent slope more shallow because V is being scaled less aggressively.

From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.


UC Regents Spring 2016 © UCB

# Second Factor: Leakage Currents

Even when a logic gate isn't switching, it burns power.

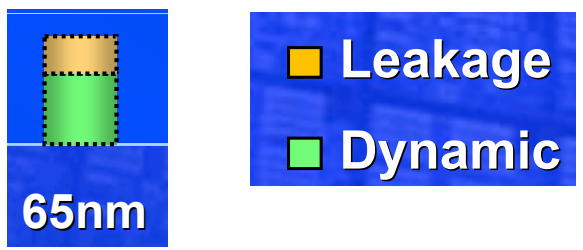



Isub: Even when this nFet is off, it passes an Ioff leakage current.

We can engineer any Ioff we like, but a lower Ioff also results in a lower Ion, and thus a lower maximum clock speed.

Igate: Ideal capacitors have zero DC current. But modern transistor gates are a few atoms thick, and are not ideal.

## Intel's 2006 processor designs, leakage vs switching power



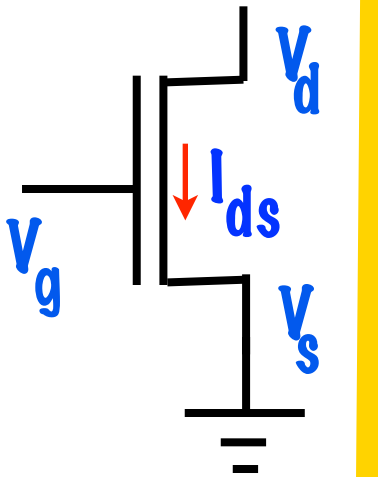

A lot of work was done to get a ratio this good ... 50/50 is common.

Bill Holt, Intel, Hot Chips 17

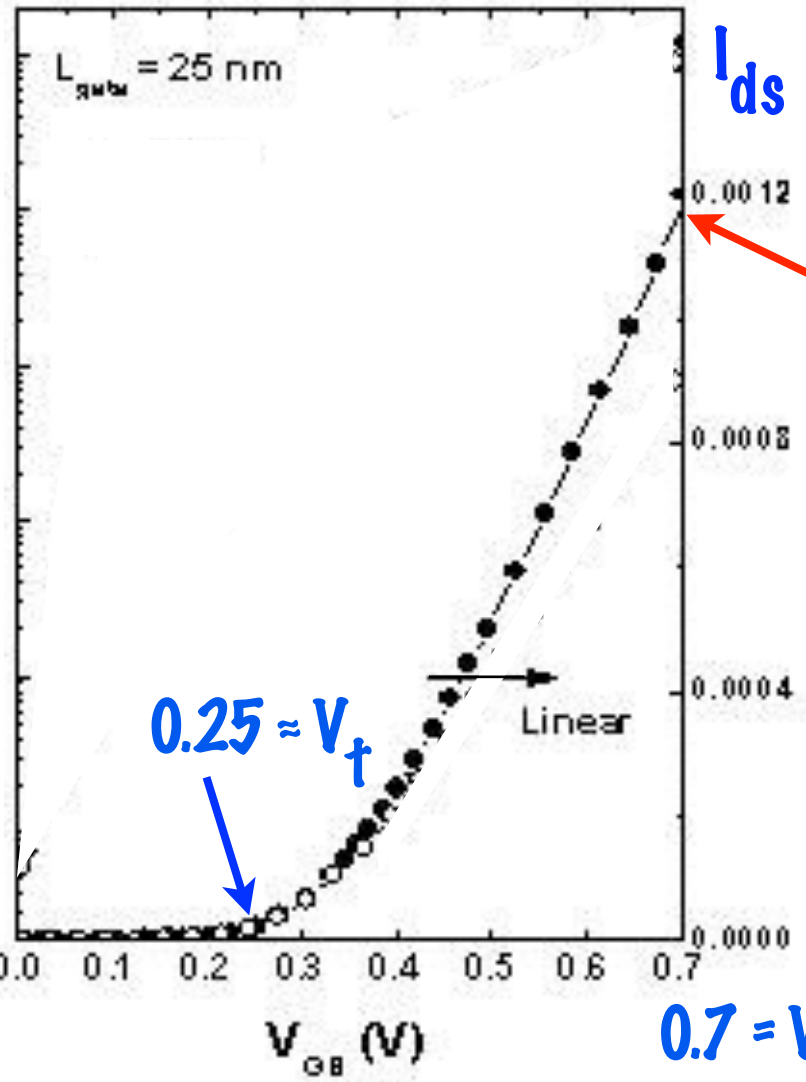


UC Regents Spring 2016 © UCB

# Engineering "On" Current at 25 nm …




We can increase $I_{on}$ by raising $V_{dd}$ and/or lowering $V_t$.




1.2 mA = $I_{on}$

0.25 ≈ $V_t$

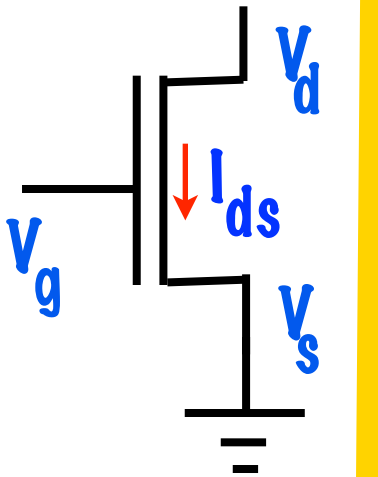
$I_{off}$ = 0 ???

0.7 = $V_{dd}$

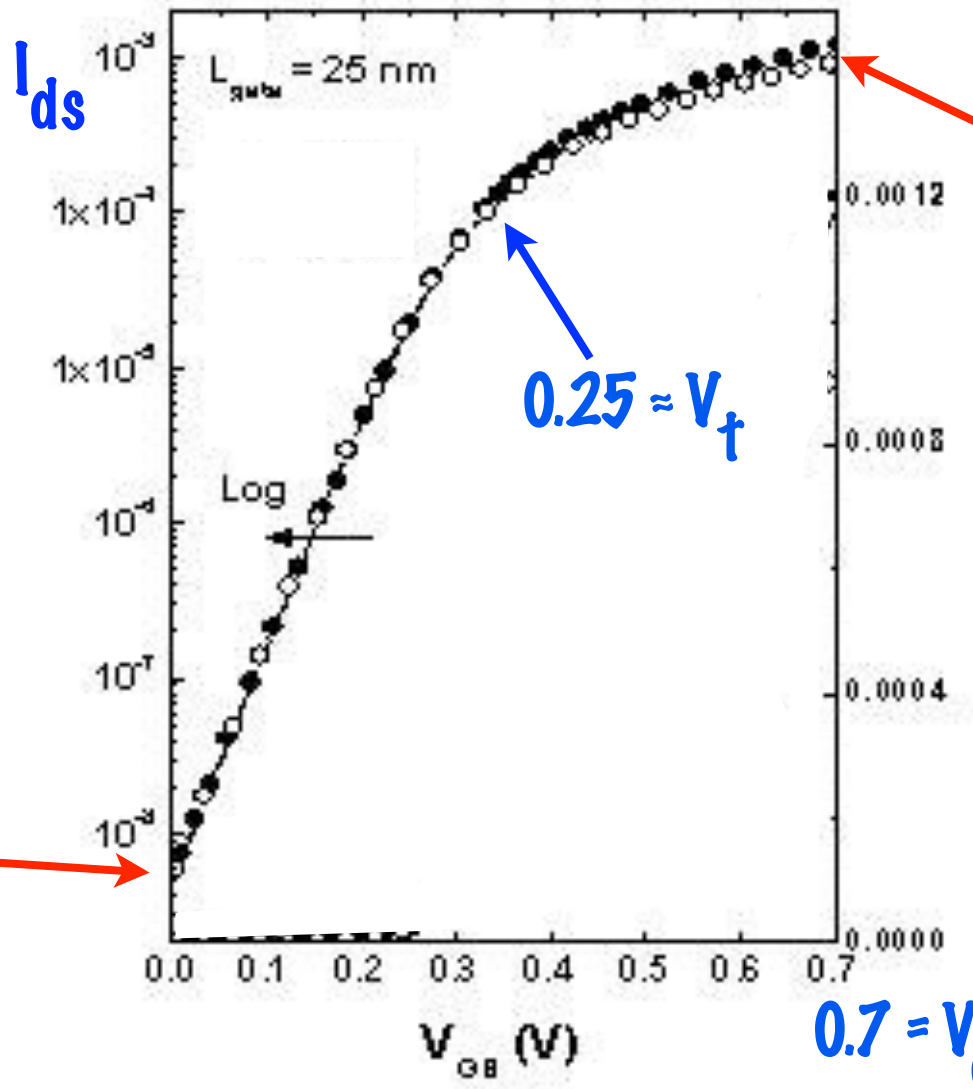


UC Regents Spring 2016 © UCB

# Plot on a "Log" Scale to See "Off" Current




We can decrease $I_{off}$ by raising $V_t$ - but that lowers $I_{on}$.





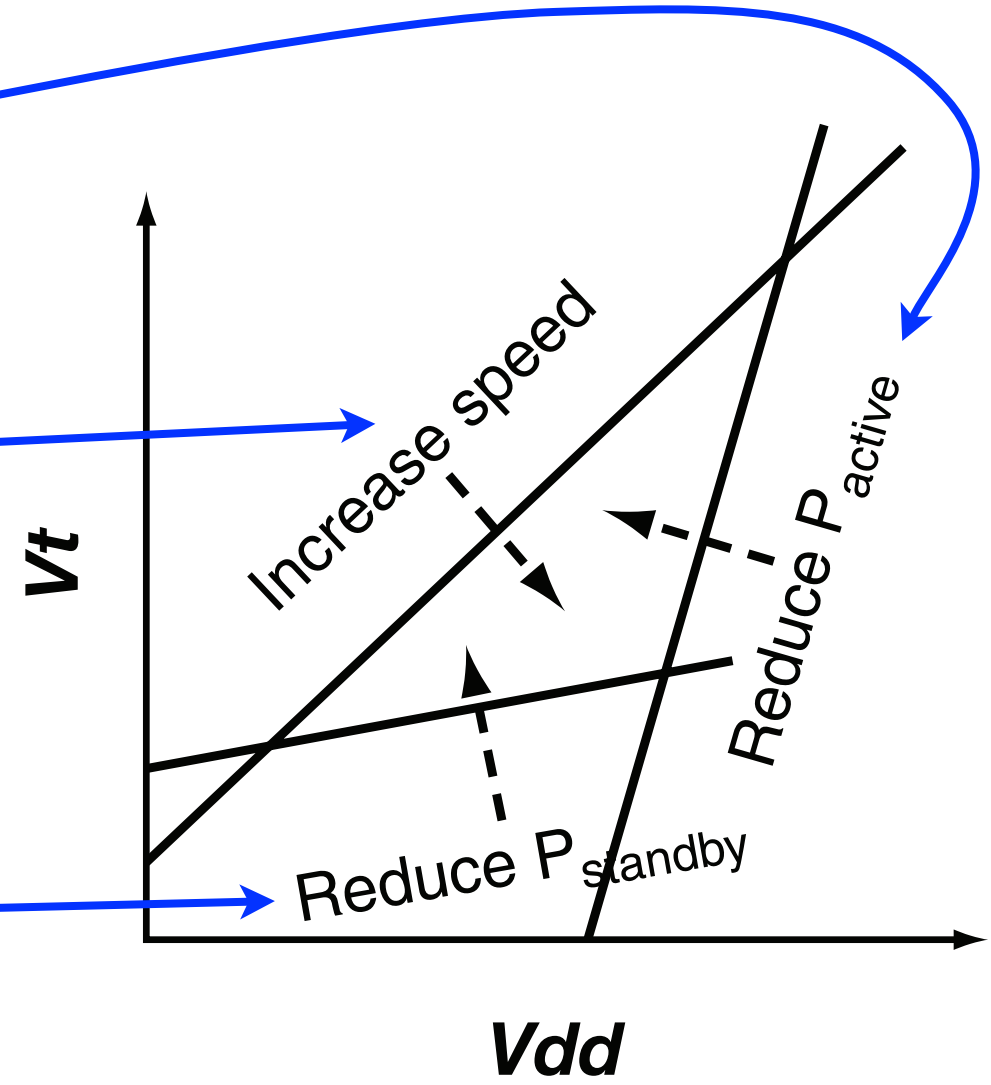

UC Regents Spring 2016 © UCB

# Device engineers trade speed and power

We can reduce $CV^2$ ($P_{active}$) by lowering $V_{dd}$.

We can increase speed by raising $V_{dd}$ and lowering $V_t$.

We can reduce leakage ($P_{standby}$) by raising $V_t$.



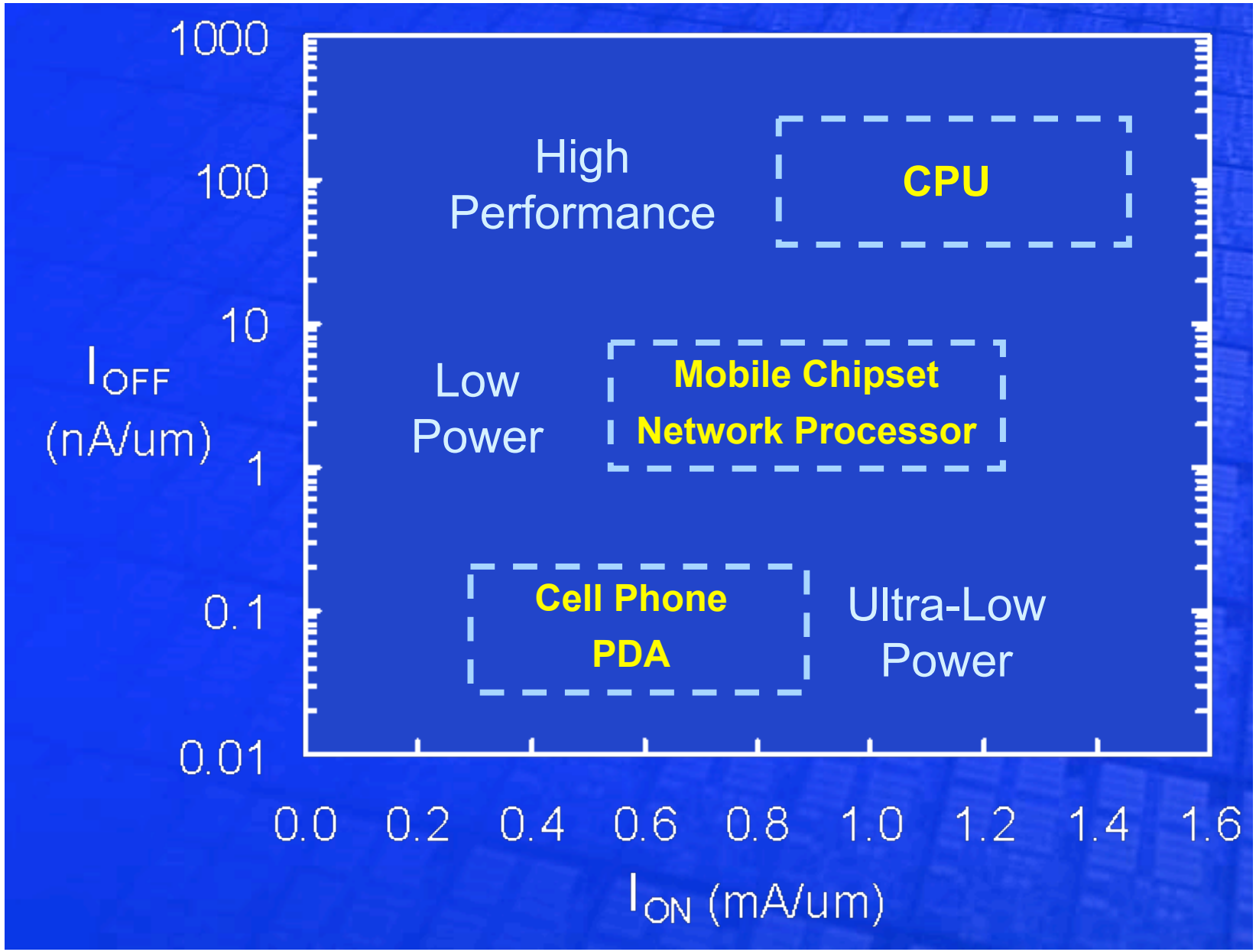

From: Silicon Device Scaling to the Sub-10-nm Regime

Meikei Ieong,[1*] Bruce Doris,[2] Jakub Kedzierski,[1] Ken Rim,[1] Min Yang[1]



UC Regents Spring 2016 © UCB

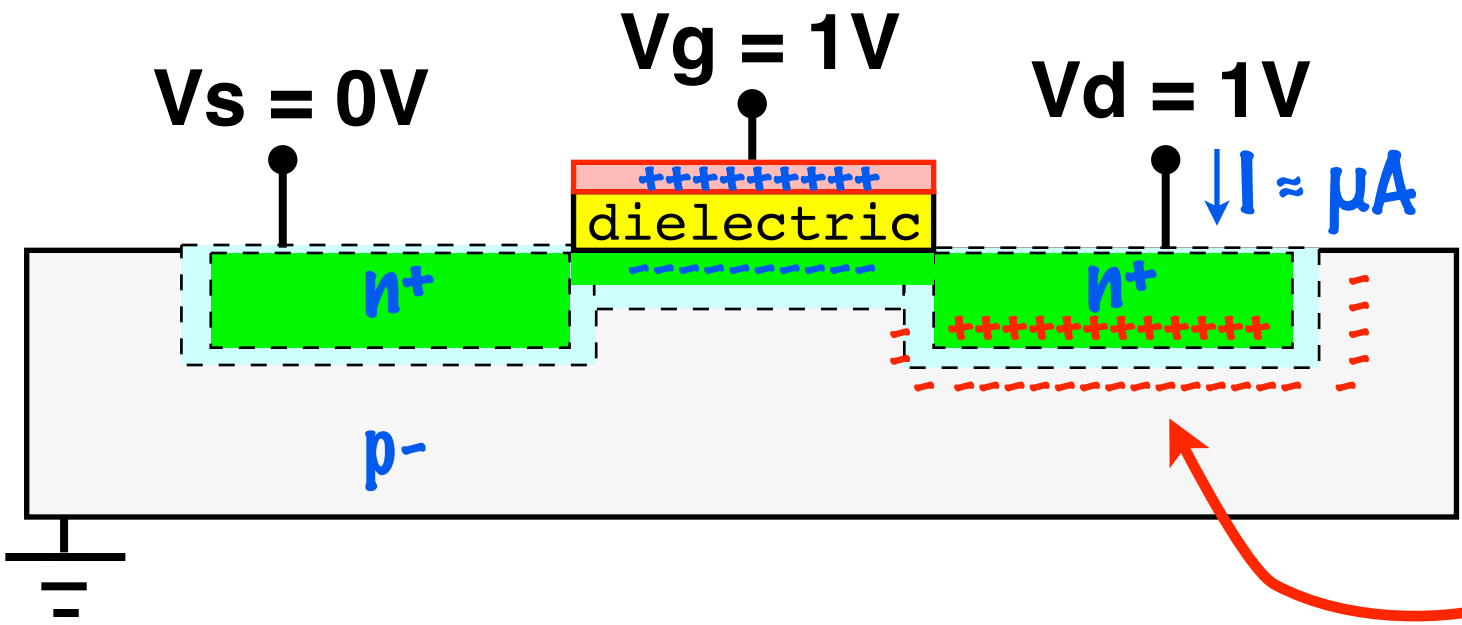
# Customize processes for product types ...



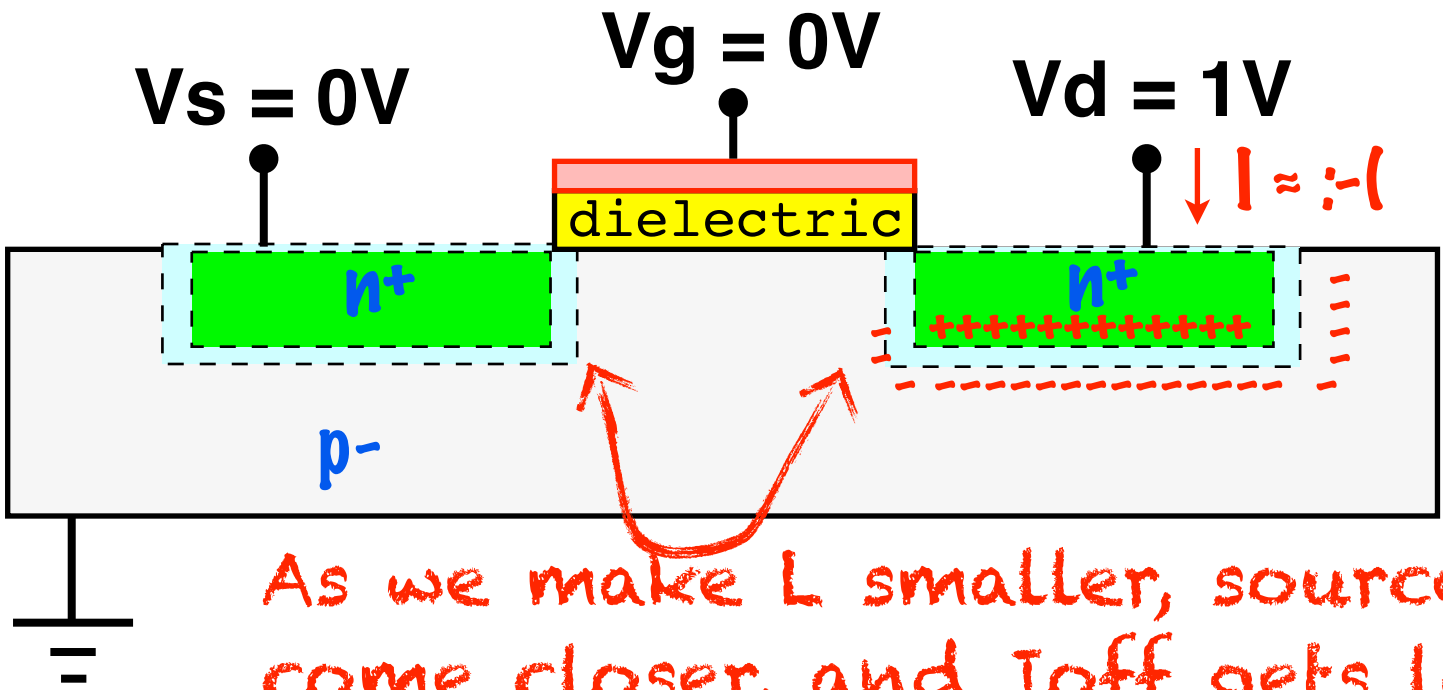

From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.


UC Regents Spring 2016 © UCB

# Transistor physics revisited ...




The drain junction is also a capacitor, and puts - charges in the substrate.



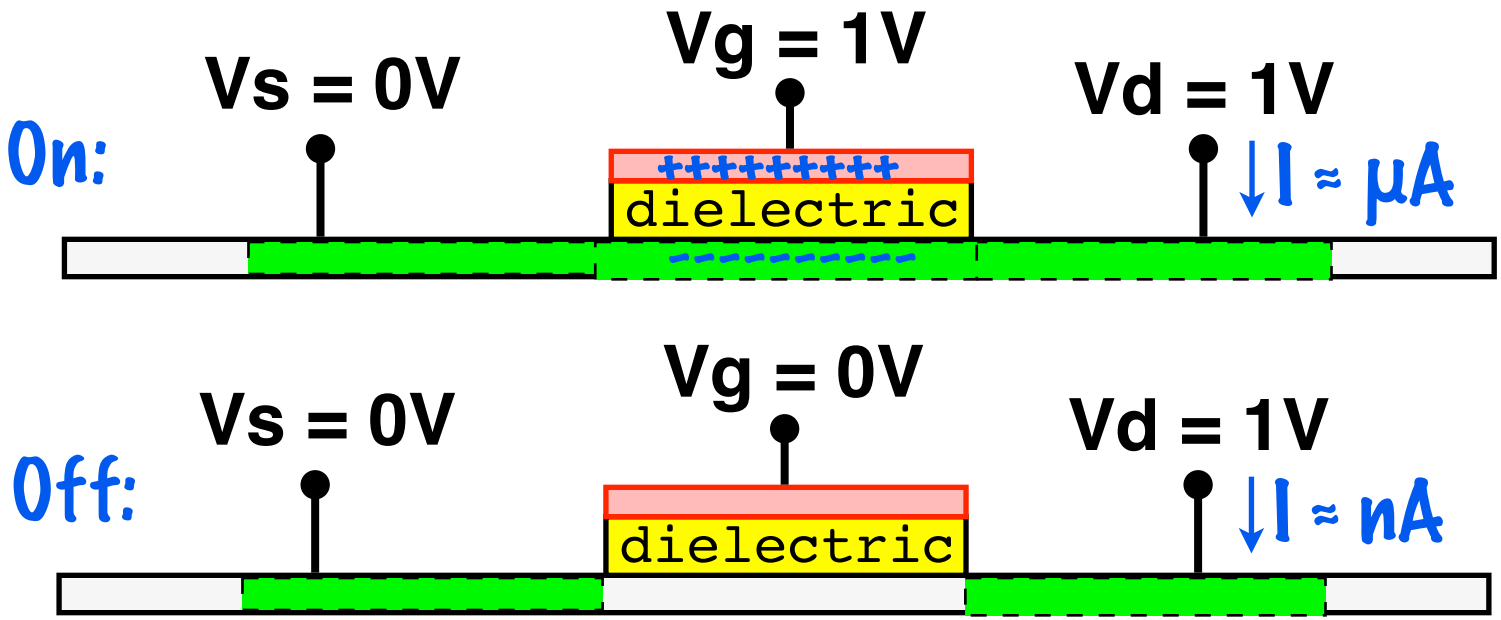

Away from the surface, the drain-induced charges remain even when the gate is off!

As we make L smaller, source and drain come closer, and Ioff gets larger!



UC Regents Spring 2016 © UCB

# Solution concept: Fully-depleted channel



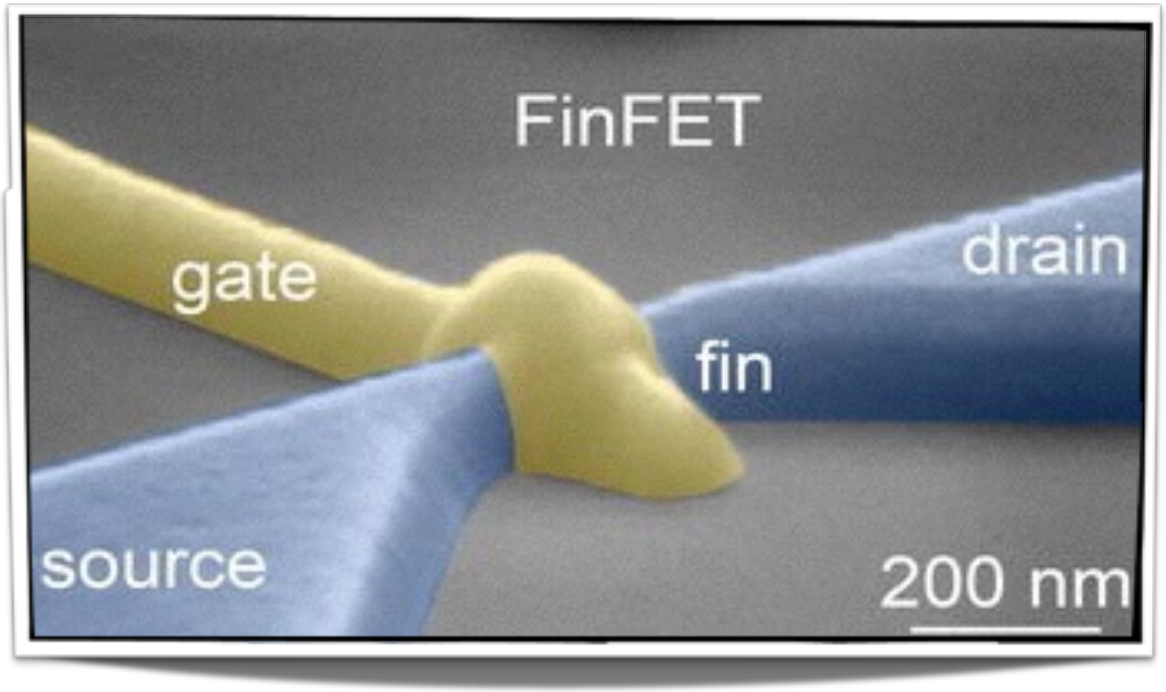

**We limit the depth of the channel so that the gate voltage "wins" over the drain voltage.**

**Done as shown, 5 to 7 nm depth for a 20 nm transistor.**

Requires expensive wafers

"FD-SOI" -- Fully-Depleted Silicon-On-Insulator

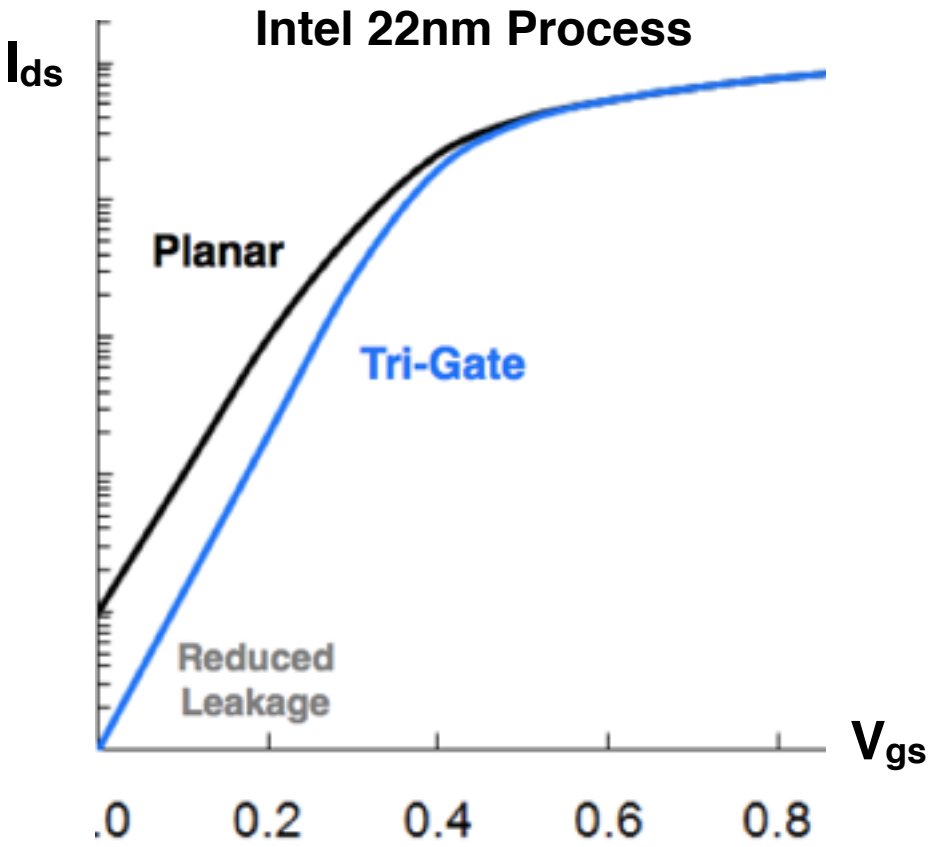

UC Regents Spring 2016 © UCB




Transistor channel is a raised fin.

Gate controls channel from sides and top.

Channel depth is fin width. 12-15nm for L=22nm.

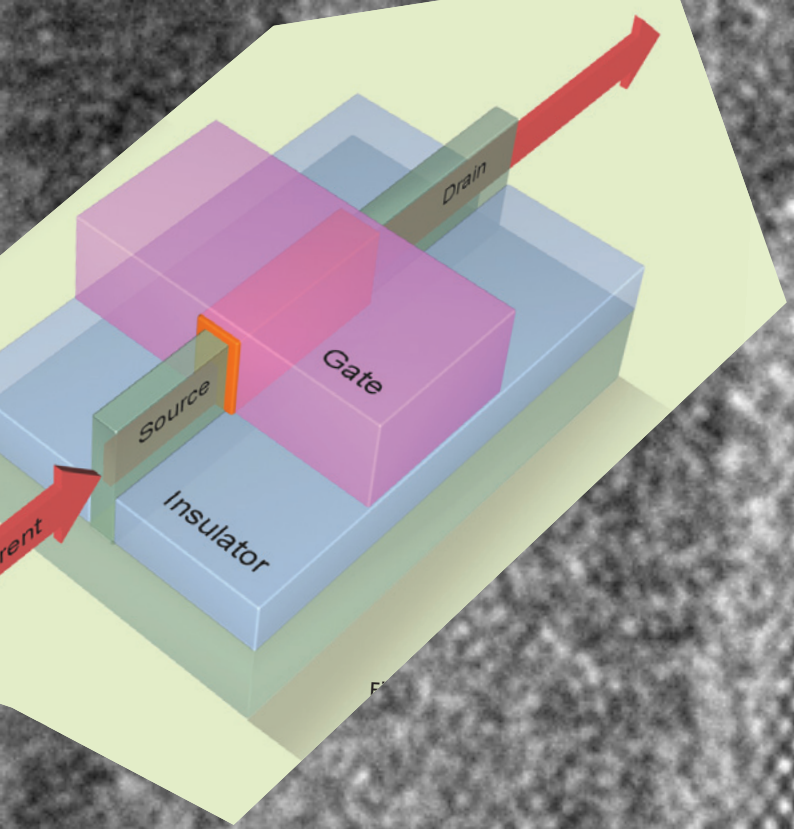



(12) **United States Patent**
**Hu et al.** Filed: **Oct. 23, 2000**

(54) **FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE**

(75) Inventors: **Chenming Hu**, Alamo; **Tsu-Jae King**, Fremont; **Vivek Subramanian**, Redwood City; **Leland Chang**, Berkeley; **Xuejue Huang**; **Yang-Kyu Choi**, both of Albany; **Jakub Tadeusz Kedzierski**, Hayward; **Nick Lindert**, Berkeley; **Jeffrey Bokor**, Oakland, all of CA (US); **Wen-Chin Lee**, Beaverton, OR (US)

UC Regents Spring 2016 © UCB

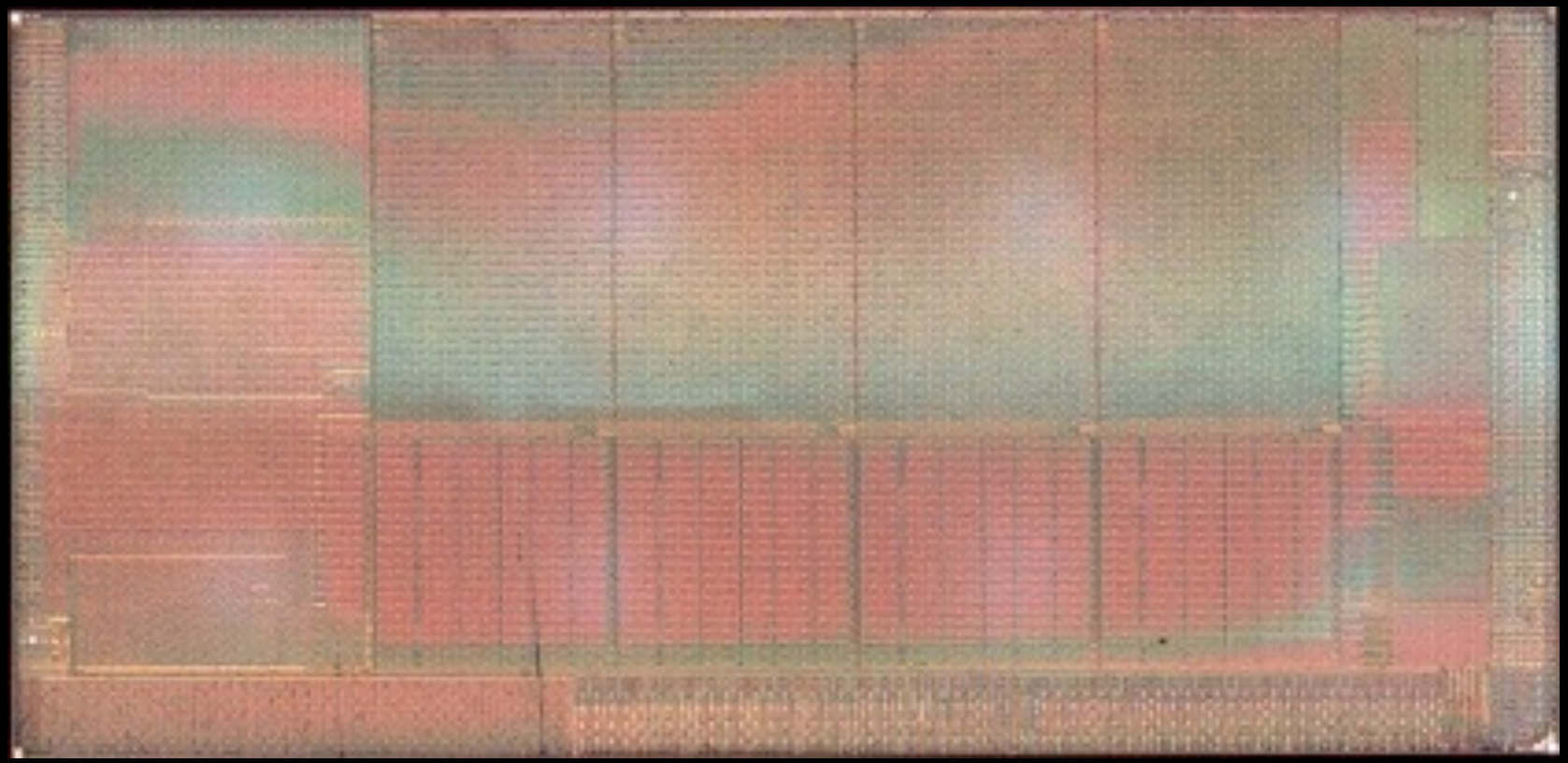



Intel
22nm
NMOS

Sandy Bridge

32nm planar

1.16B transistors

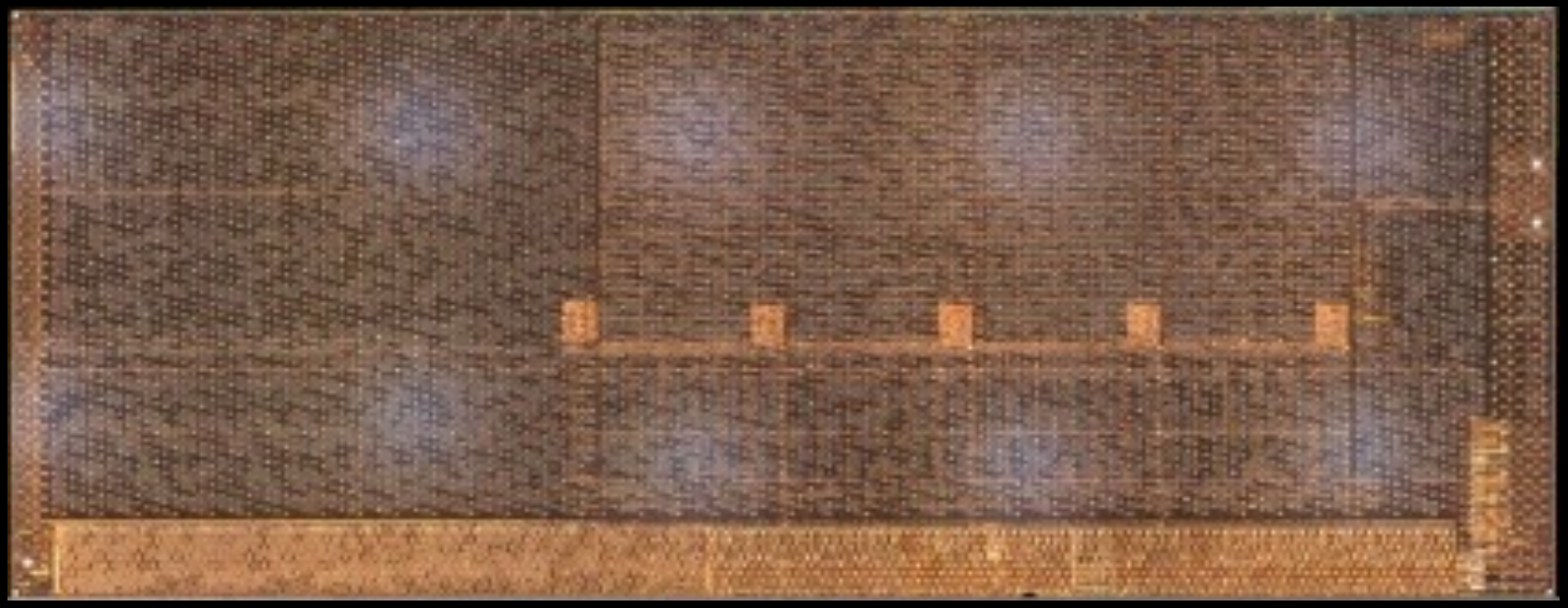


"Less than half the power @ same performance"

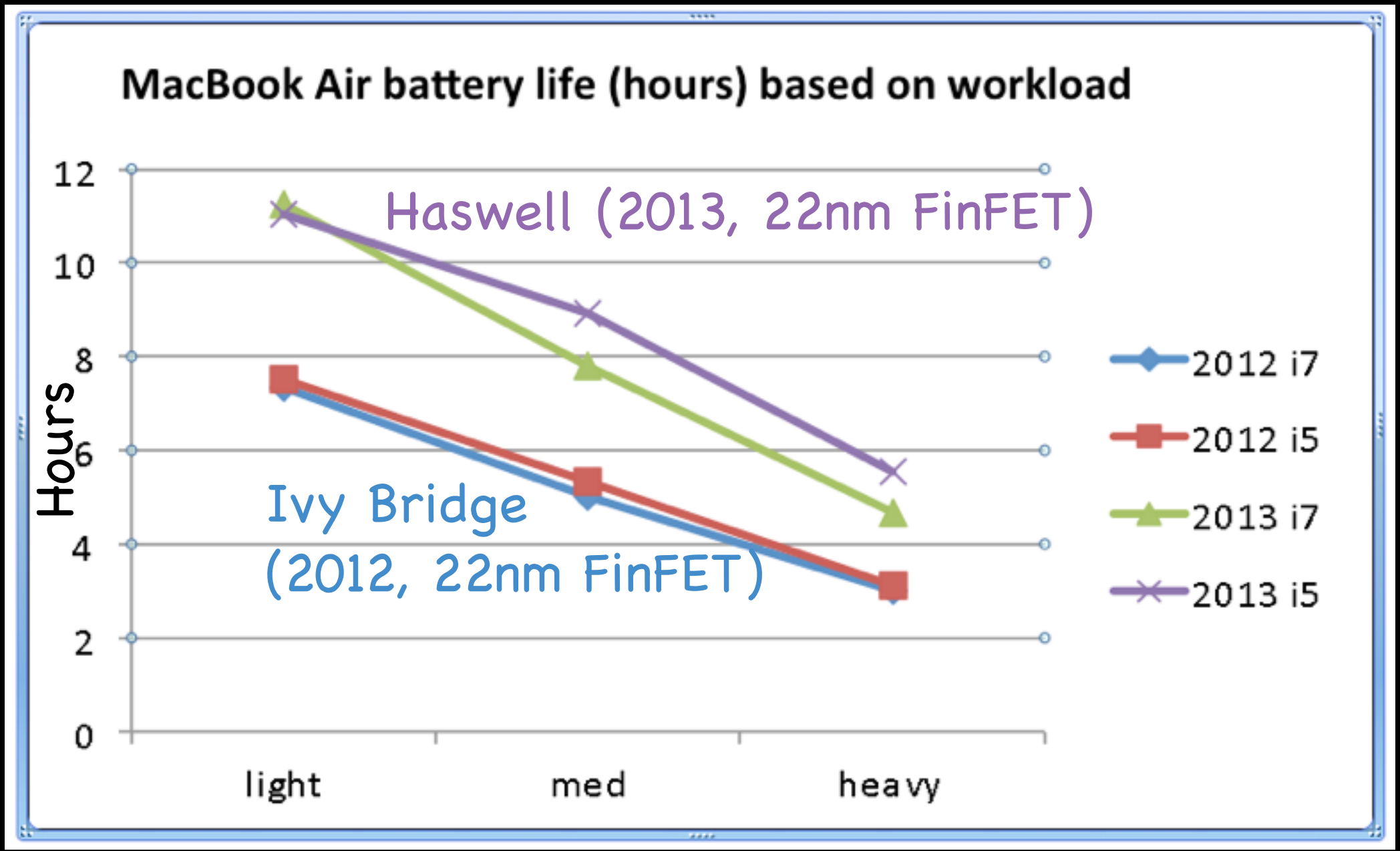
Ivy Bridge

22nm FinFet

1.4B transistors



# Leakage reduction in "Tock" 22nm Intel CPUs




*—Cary Chin is director of marketing for low-power solutions at Synopsys.*

# Break

UC Regents Spring 2016 © UCB

# Six low-power design techniques

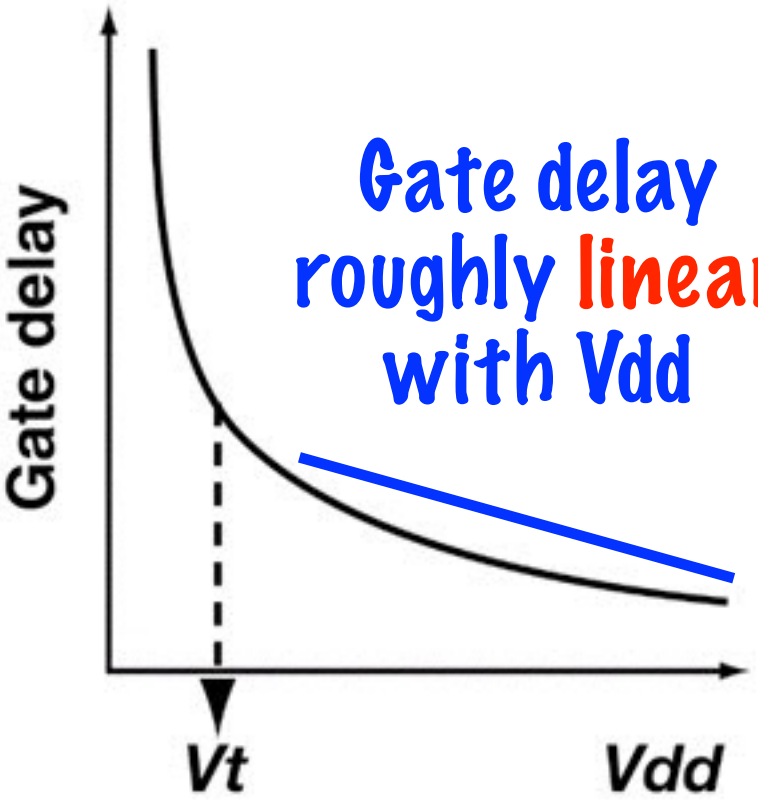
- Parallelism and pipelining
- Power-down idle transistors
- Slow down non-critical paths
- Clock gating
- Data-dependent processing
- Thermal management

UC Regents Spring 2016 © UCB

# Trading Hardware for Power

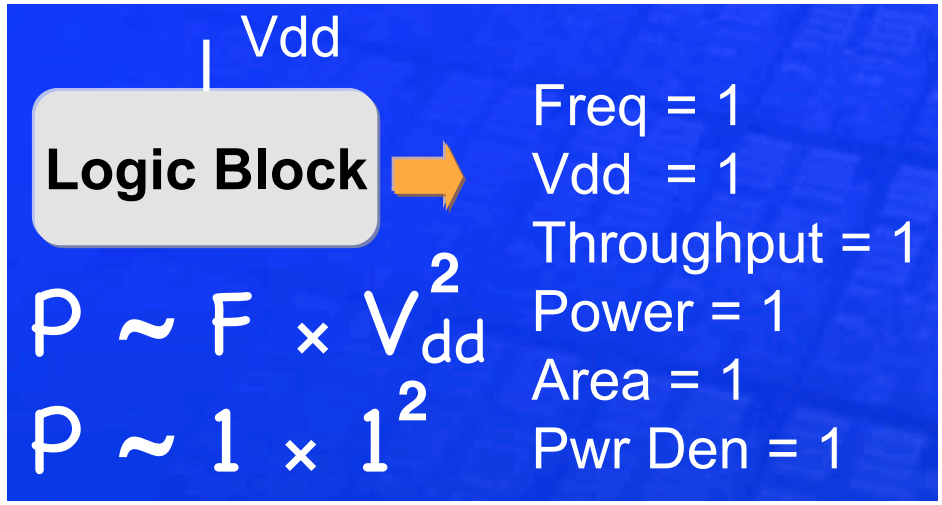
via Parallelism and Pipelining ...

UC Regents Spring 2016 © UCB




Gate delay roughly linear with Vdd

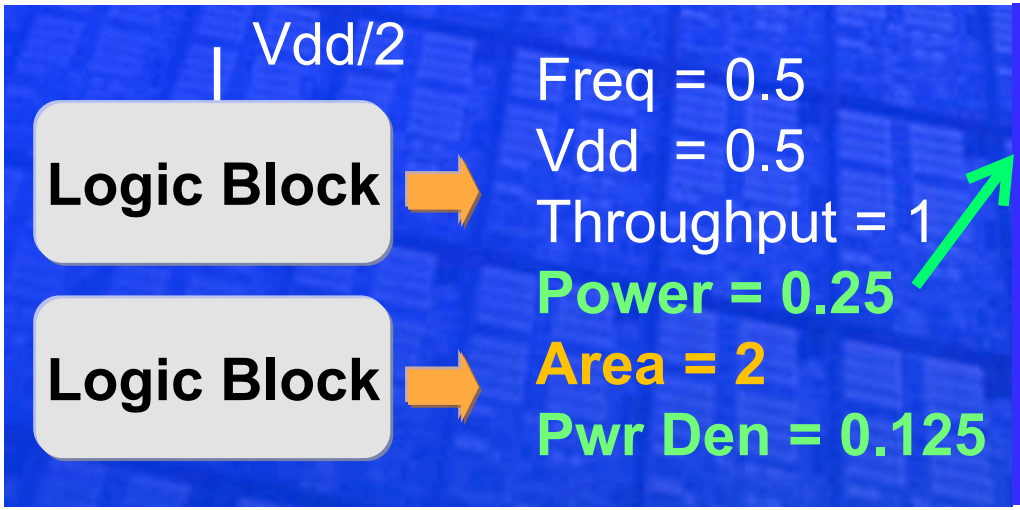
## And so, we can transform this:




Block processes stereo audio. 1/2 of clocks for "left", 1/2 for "right".

## Into this:

Top block processes "left", bottom "right".




$P \sim \#blks \times F \times V_{dd}^2$

$P \sim 2 \times 1/2 \times 1/4 = 1/4$

$CV^2$ power only

THIS MAGIC TRICK BROUGHT TO YOU BY CORY HALL ...



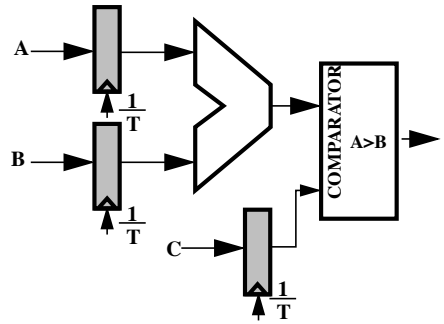
UC Regents Spring 2016 © UCB

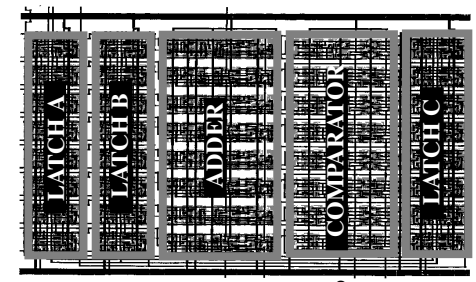
# Chandrakasan & Brodersen (UCB, 1992)

| Architecture | Power (normalized) |
|---|---|
| Simple | 1 |
| Parallel | 0.36 |
| Pipelined | 0.39 |
| Pipelined-Parallel | 0.2 |

| Architecture | Area (normalized) |
|---|---|
| Simple | 1 |
| Parallel | 3.4 |
| Pipelined | 1.3 |
| Pipelined-Parallel | 3.7 |

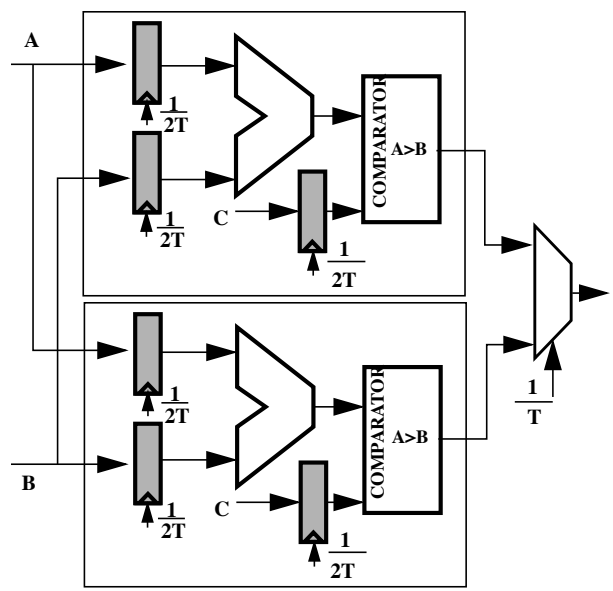
| Architecture | Voltage |
|---|---|
| Simple | 5V |
| Parallel | 2.9V |
| Pipelined | 2.9V |
| Pipelined-Parallel | 2.0 |

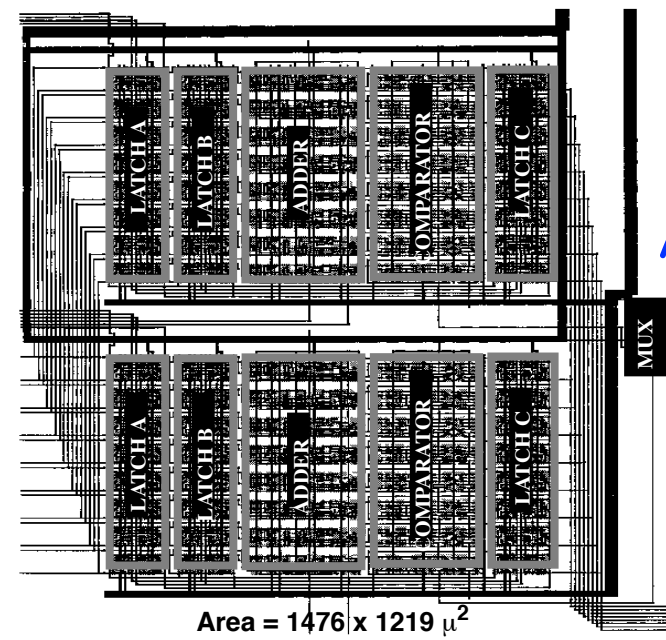



Area = 636 x 833 $\mu^2$

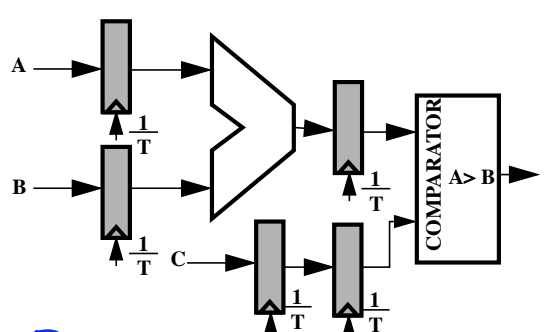
Simple

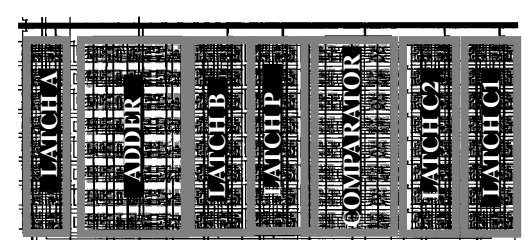



Area = 1476 x 1219 $\mu^2$

Parallel




Area = 640 x 1081 $\mu^2$

Pipelined

From:

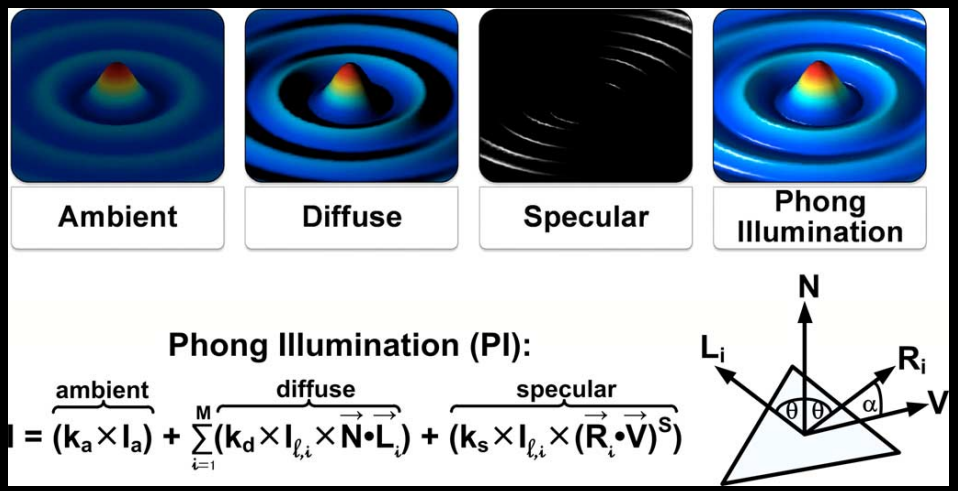
**Minimizing Power Consumption in CMOS Circuits**

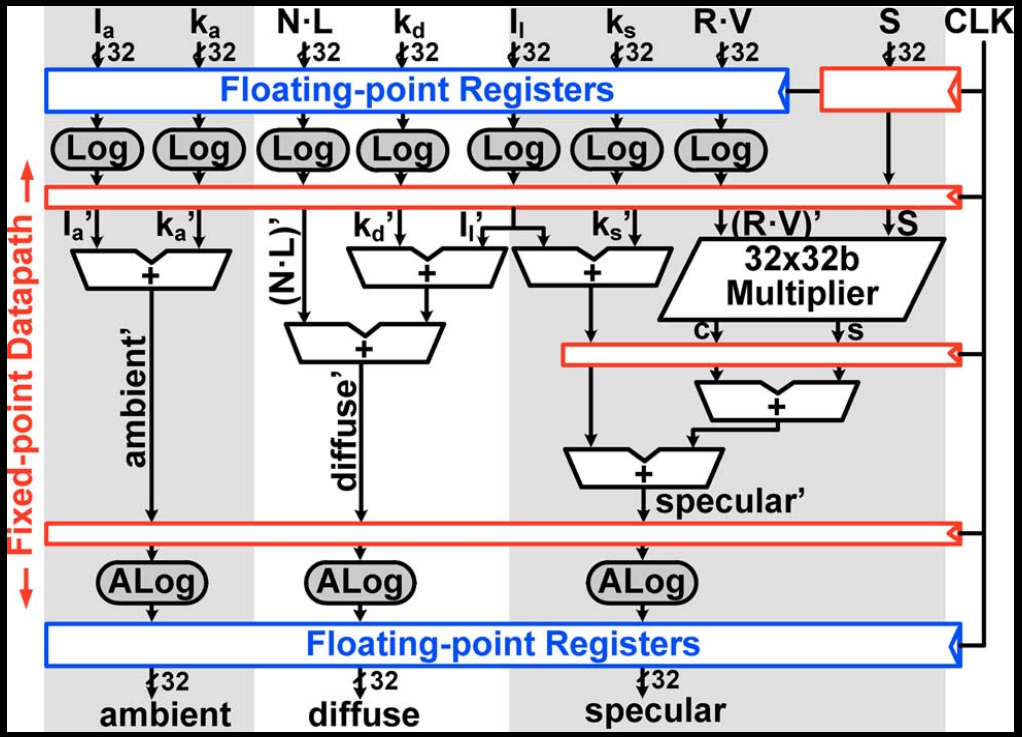
Anantha P. Chandrakasan
Robert W. Brodersen

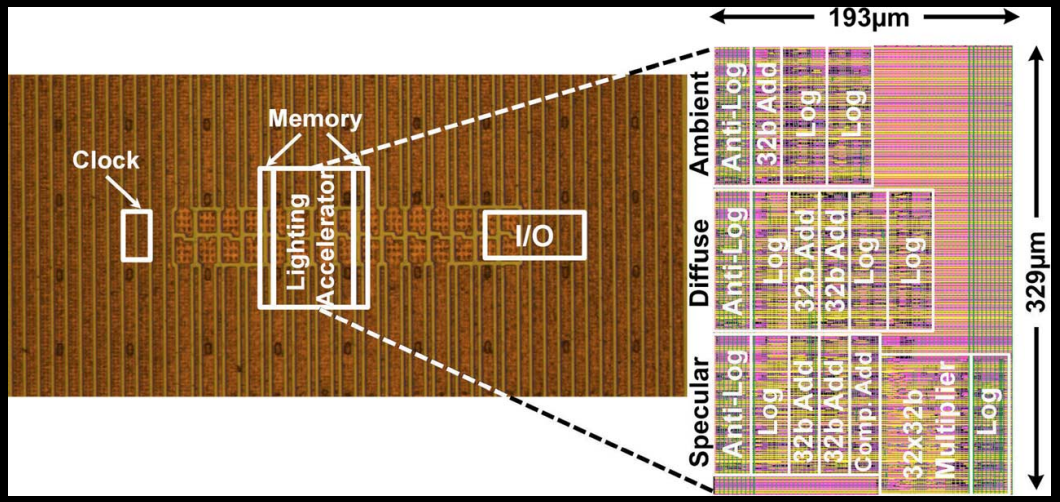


Regents Spring 2016 © UCB

# Example: Intel Graphics Pipeline IP



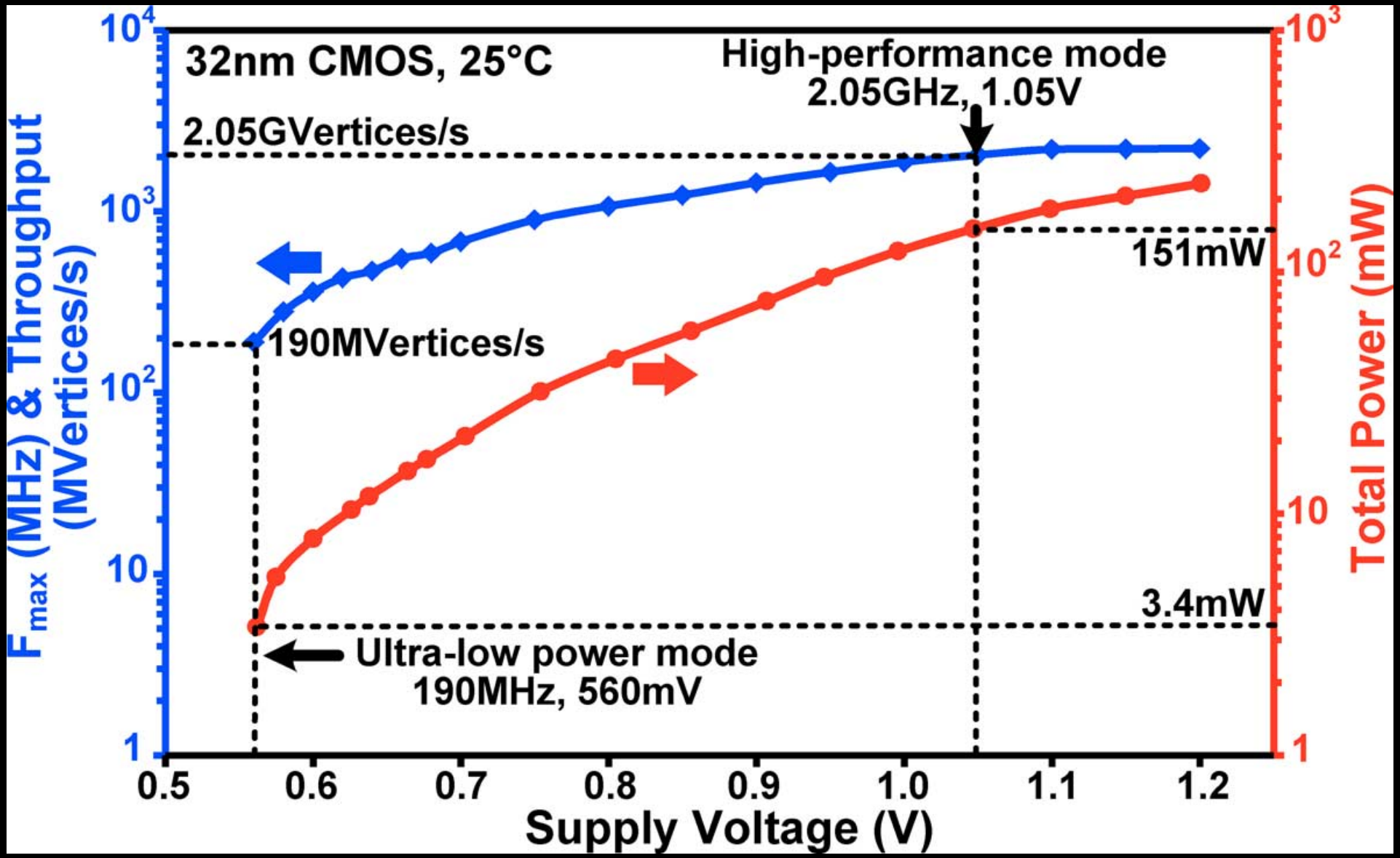




A 2.05 GVertices/s 151 mW Lighting Accelerator for 3D Graphics Vertex and Pixel Shading in 32 nm CMOS

Farhana Sheikh, *Member, IEEE*, Sanu K. Mathew, *Member, IEEE*, Mark A. Anders, *Member, IEEE*, Himanshu Kaul, *Member, IEEE*, Steven K. Hsu, *Member, IEEE*, Amit Agarwal, *Member, IEEE*, Ram K. Krishnamurthy, *Fellow, IEEE*, and Shekhar Borkar, *Fellow, IEEE*

# Clock Rate and Power vs Voltage




A 2.05 GVertices/s 151 mW Lighting Accelerator for 3D Graphics Vertex and Pixel Shading in 32 nm CMOS

Farhana Sheikh, *Member, IEEE*, Sanu K. Mathew, *Member, IEEE*, Mark A. Anders, *Member, IEEE*, Himanshu Kaul, *Member, IEEE*, Steven K. Hsu, *Member, IEEE*, Amit Agarwal, *Member, IEEE*, Ram K. Krishnamurthy, *Fellow, IEEE*, and Shekhar Borkar, *Fellow, IEEE*

# Multiple Cores for Low Power

Trade hardware for power,
on a large scale ...

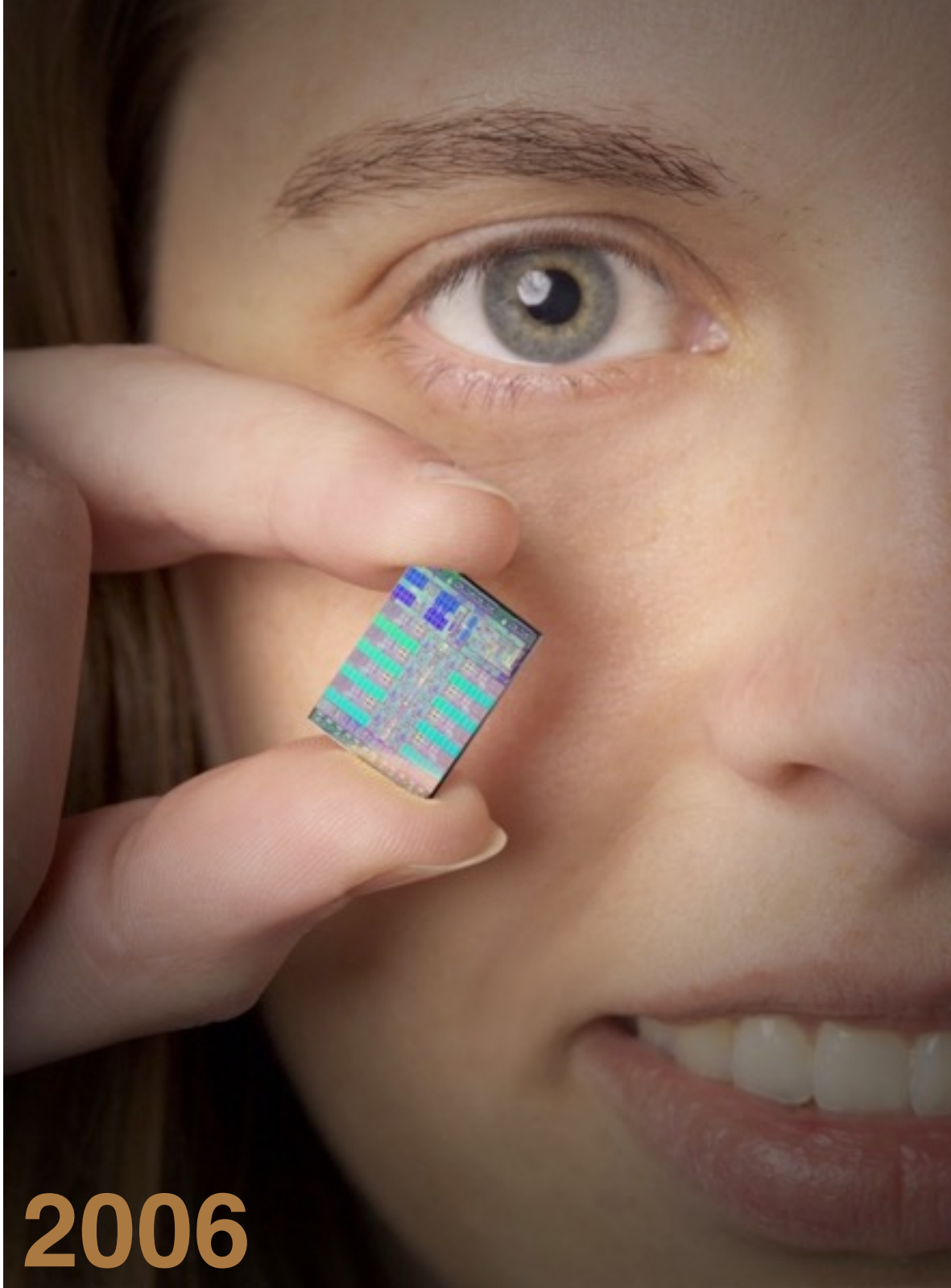
UC Regents Spring 2016 © UCB

# Cell: The PS3 chip

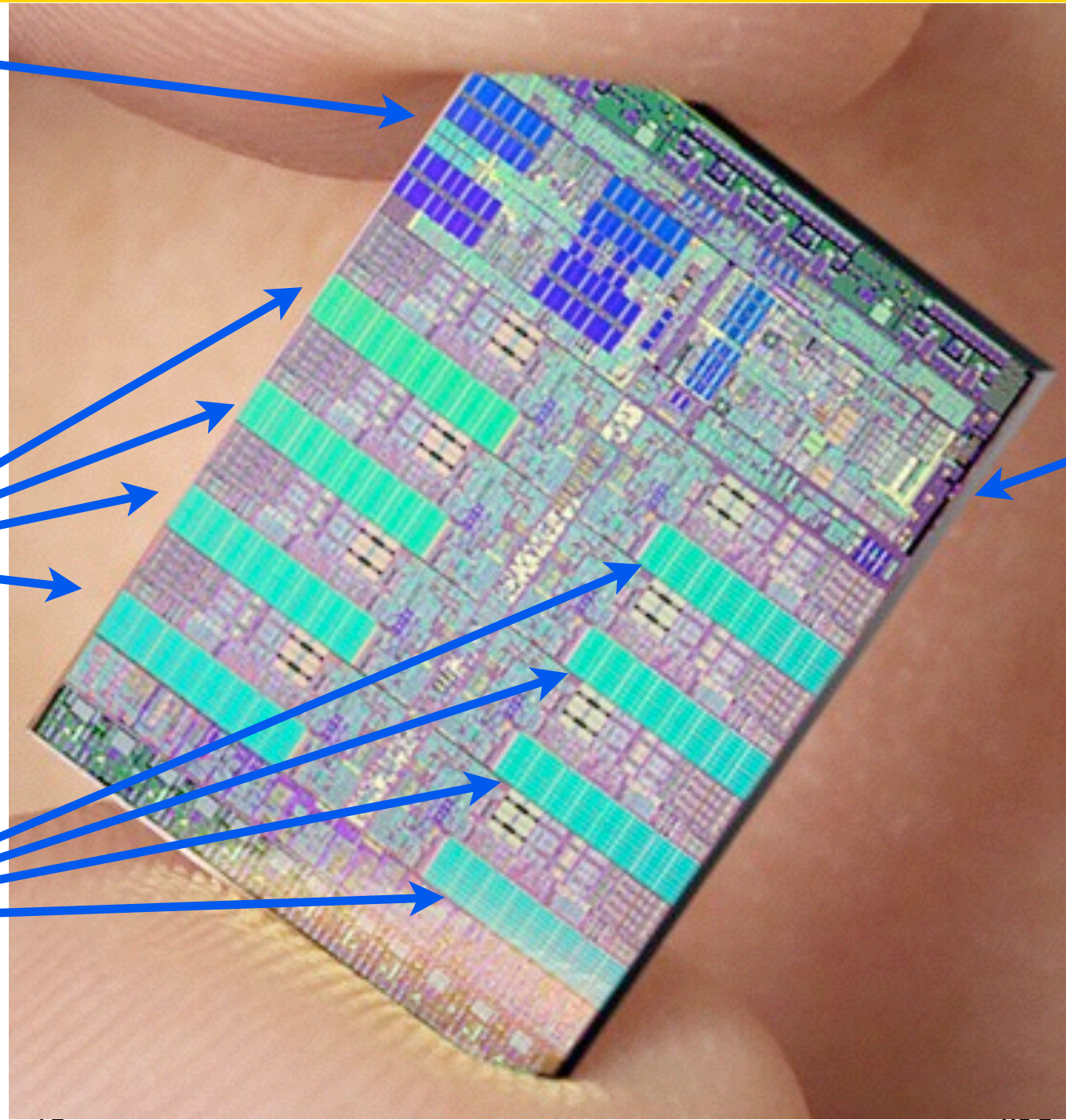
IBM

SONY COMPUTER ENTERTAINMENT

TOSHIBA



# Cell (PS3 Chip): 1 CPU + 8 "SPUs"




IBM

SONY
COMPUTER
ENTERTAINMENT

TOSHIBA



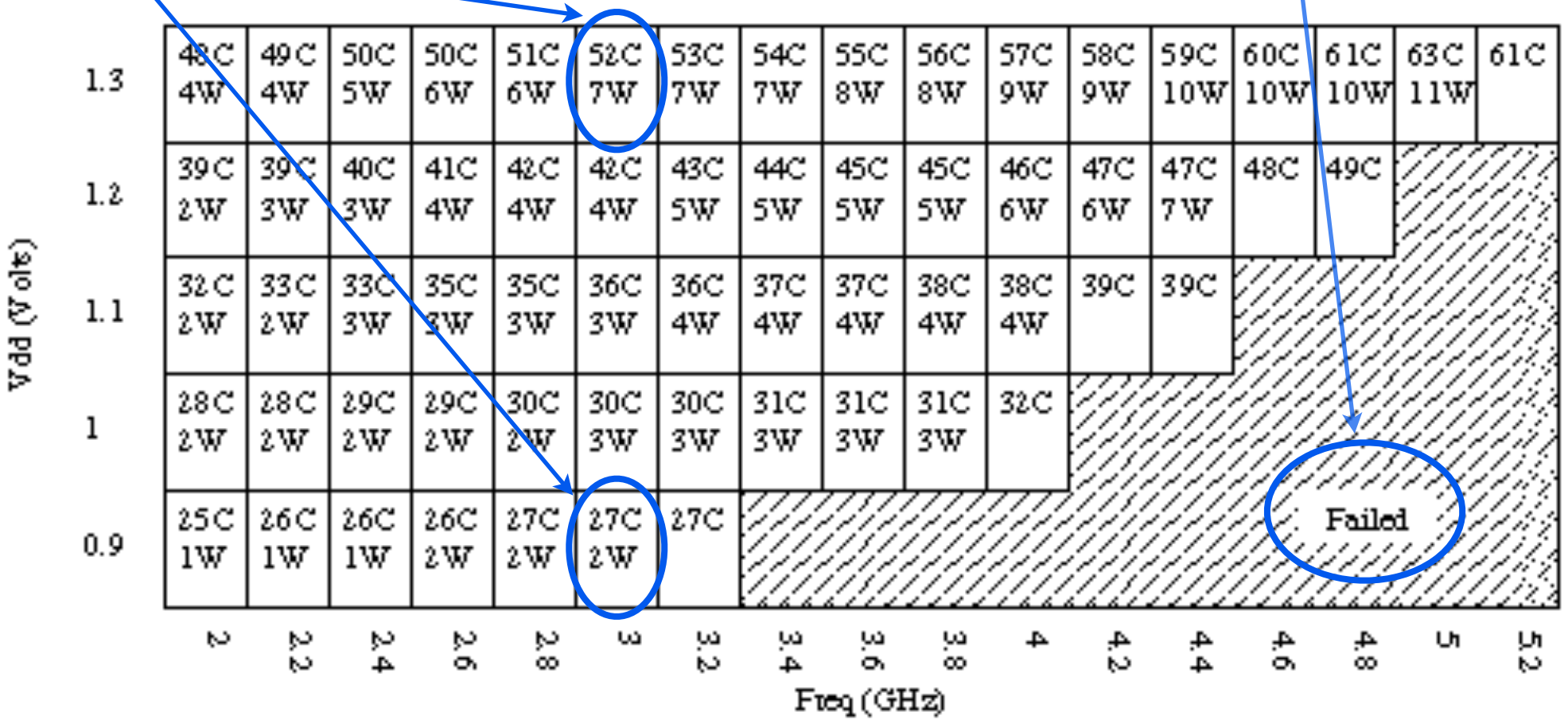
UC Regents Spring 2016 © UCB

# A "Schmoo" plot for a Cell SPU ...

The lower Vdd, the less dynamic energy consumption.

$$E_{0\to1} = \frac{1}{2} C V_{dd}^2 \qquad E_{1\to0} = \frac{1}{2} C V_{dd}^2$$

The lower Vdd, the longer the maximum clock period, the slower the clock frequency.



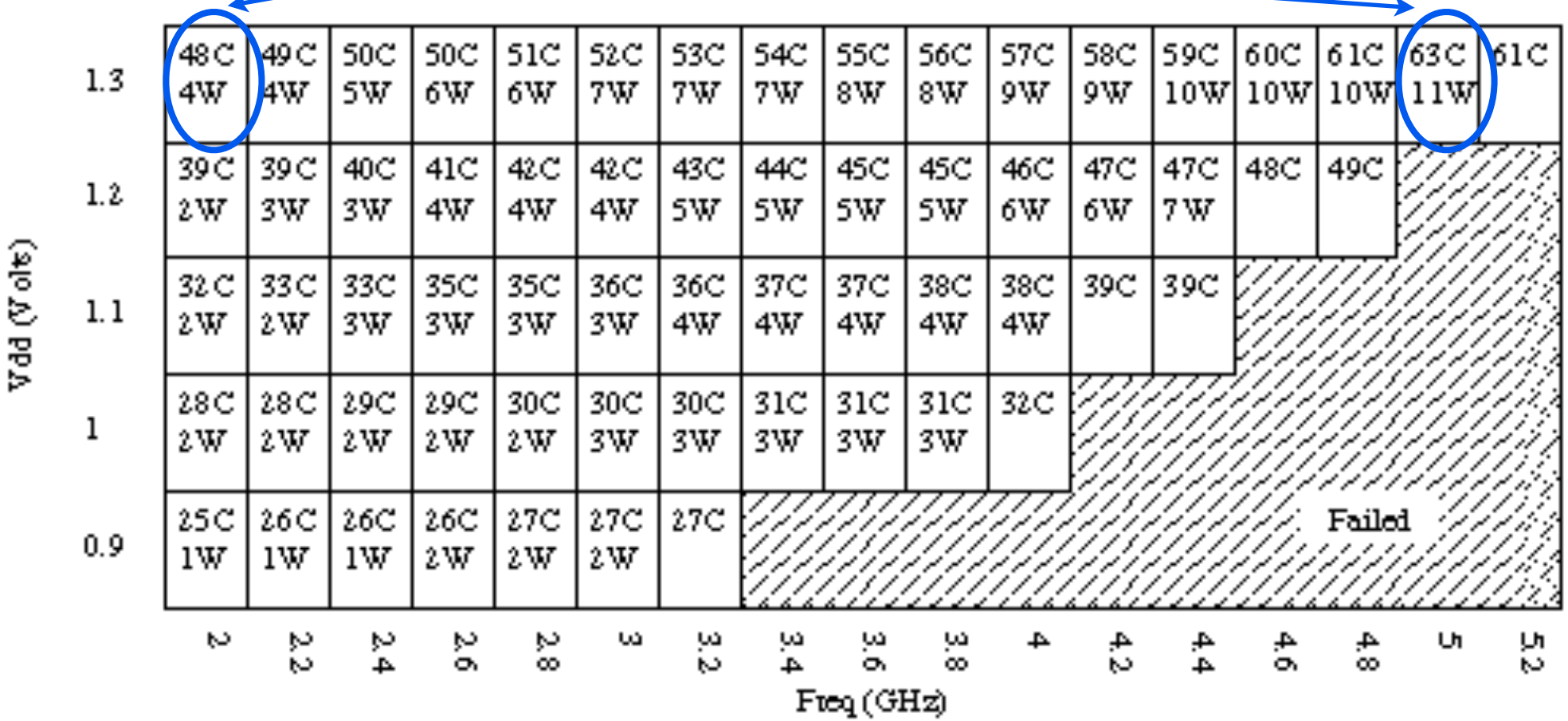



UC Regents Spring 2016 © UCB

# Clock speed alone doesn't help E/op ...

But, lowering clock frequency while keeping voltage constant spreads the same amount of work over a longer time, so chip stays cooler ...

$$E_{0->1} = \frac{1}{2} C V_{dd}^2 \qquad E_{1->0} = \frac{1}{2} C V_{dd}^2$$





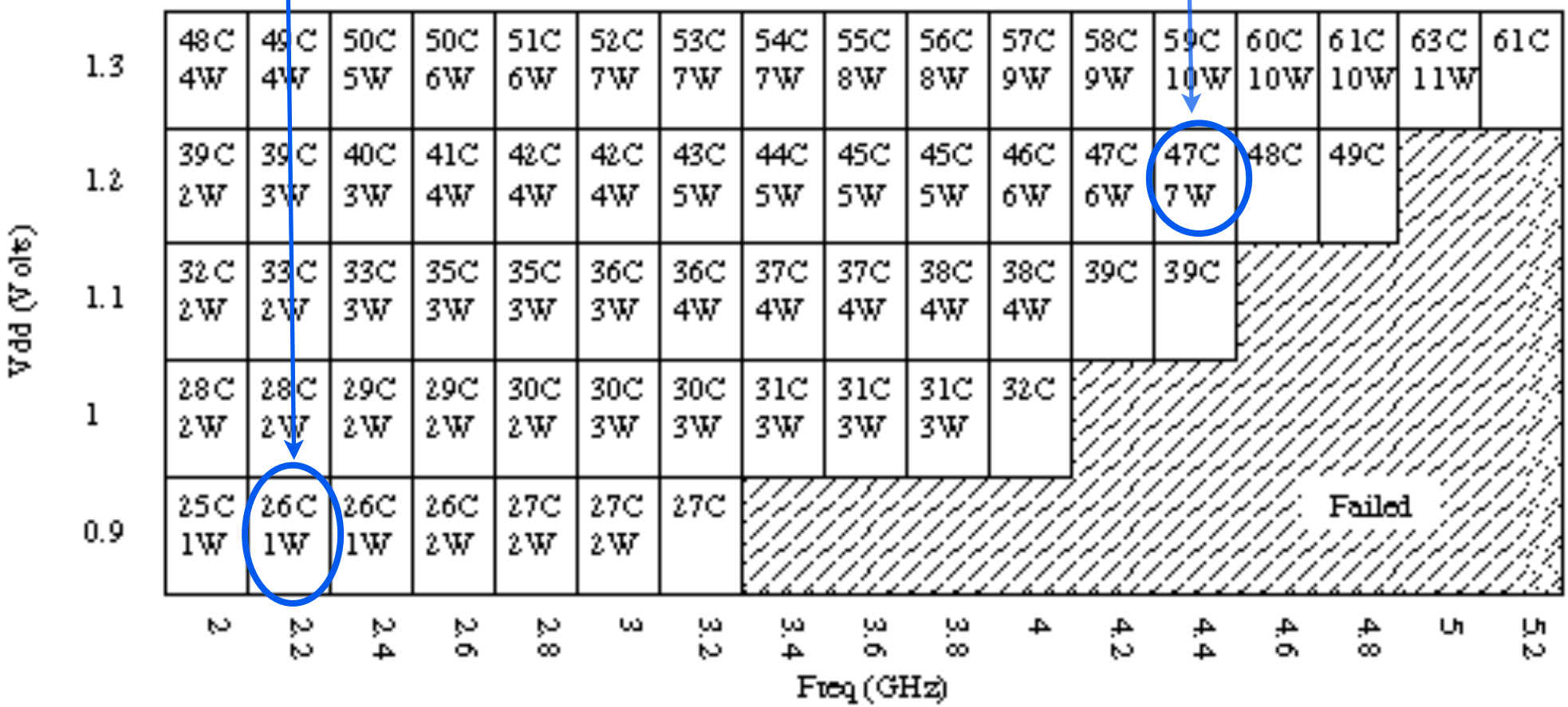

UC Regents Spring 2016 © UCB

# Scaling V and f *does* lower energy/op

1 W to get 2.2 GHz performance. 26 C die temp.

7W to reliably get 4.4 GHz performance. 47C die temp.

If a program that needs a 4.4 Ghz CPU can be recoded to use two 2.2 Ghz CPUs ... big win.





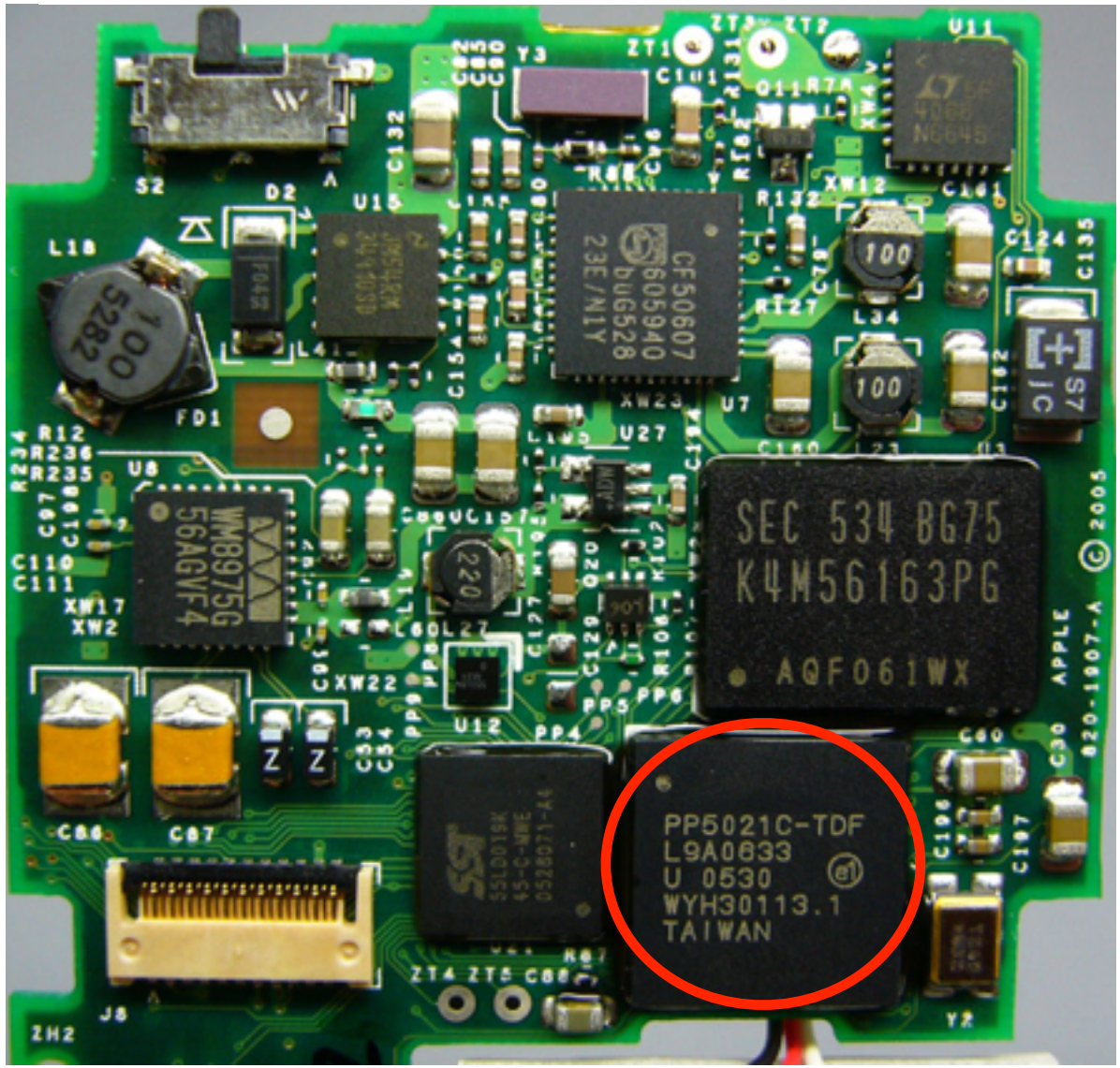

UC Regents Spring 2016 © UCB

# How iPod nano 2005 puts its 2 cores to use ...

portalplayer™

**PP5020**

digital media management system-on-chip




## Dual ARM Processors

- Dual 32-bit ARM7TDMI processors
- Up to 80 MHz processor operation per core with independent clock-skipping feature on COP
- Efficient cross-bar implementation providing zero wait state access to internal RAM
- Integrated 96KB of SRAM
- 8KB of unified cache per processor
- Six DMA channels

Two 80 MHz CPUs. Was used in several nano generations, with one CPU doing audio decoding, the other doing photos, etc.

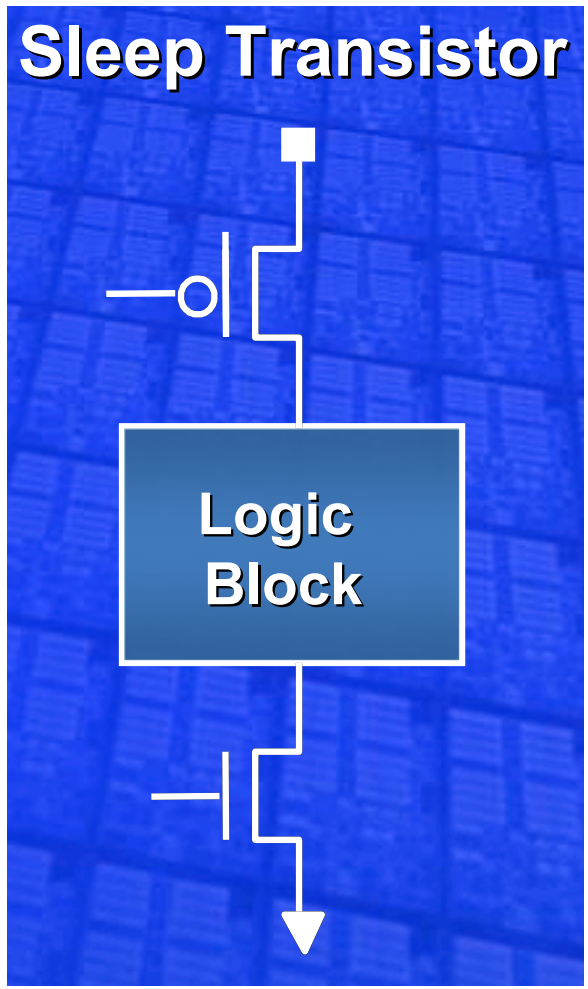


UC Regents Spring 2016 © UCB

# Powering down idle circuits

UC Regents Spring 2016 © UCB

# Add “sleep” transistors to logic ...




Example: Floating point unit logic.

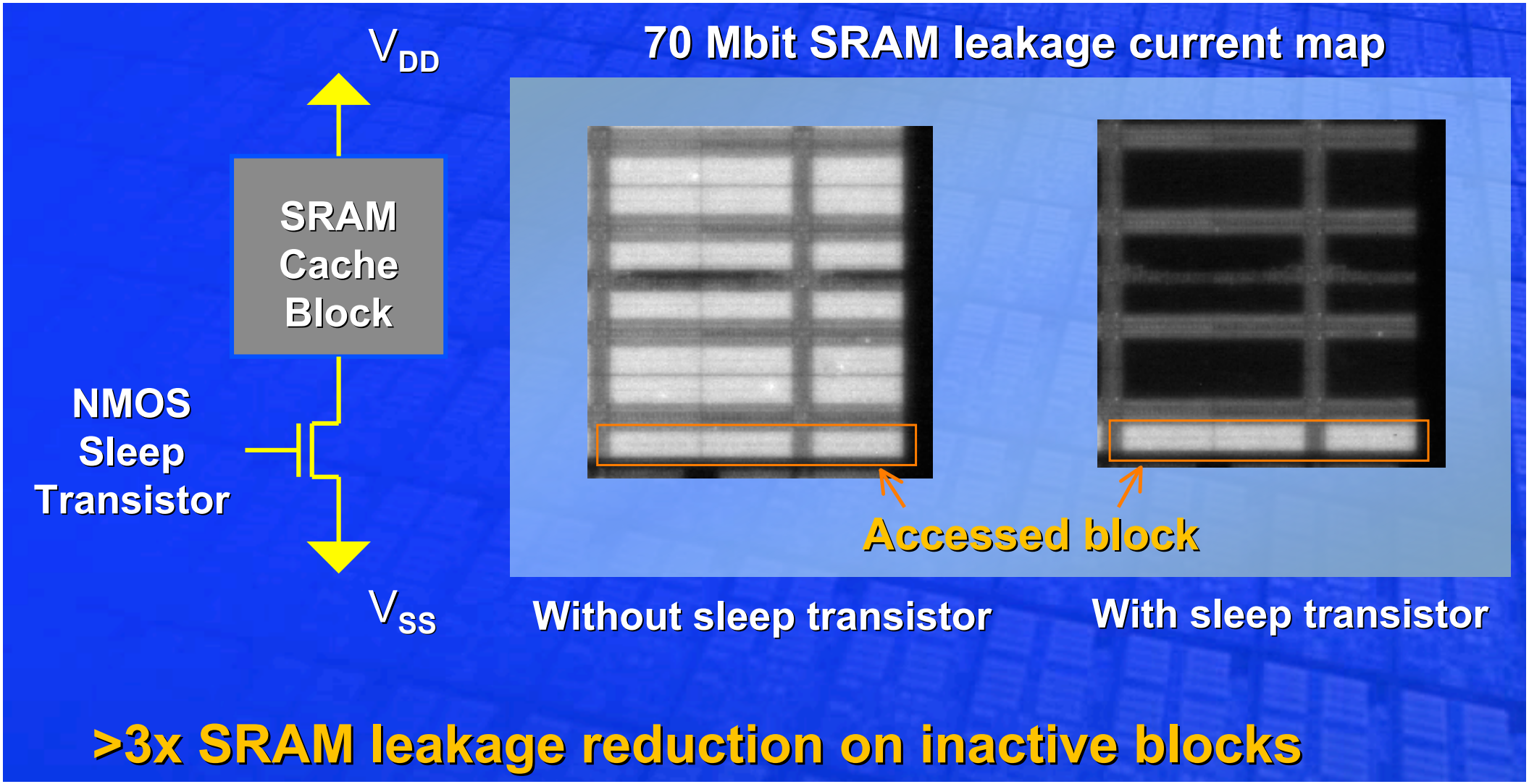
When running fixed-point instructions, put logic “to sleep”.

+++ When “asleep”, leakage power is dramatically reduced.

--- Presence of sleep transistors slows down the clock rate when the logic block is in use.


UC Regents Spring 2016 © UCB

# Intel example: Sleeping cache blocks

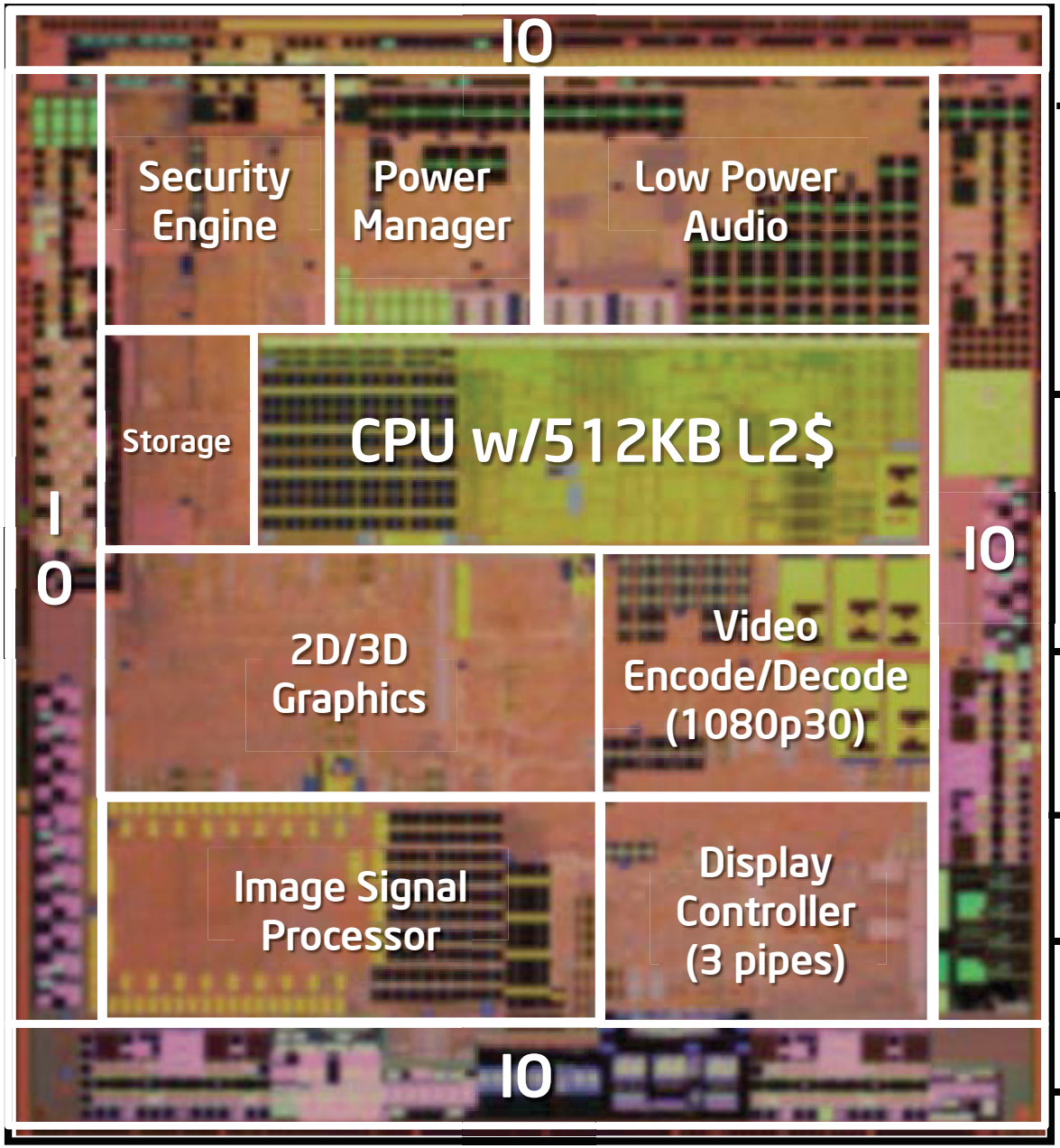



A tiny current supplied in "sleep" maintains SRAM state.

From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.


UC Regents Spring 2016 © UCB

# Intel Medfield




LPDDR2

eMMC

SD/MMC

Primary Camera: 8MP, 15fps, 1080p

MIPI-CSI

Secondary Camera: 1.3MP, 1080p

MIPI-CSI

Rails I2S ULPI

Power Delivery IC: VRs Audio CODEC USB2 OTG

MIPI-HSI

IMC 6260 HSPA+ Modem

SDIO

TI WiFi & BT

UART

CSR GPS

HDMI 1.3a

HDMI Display

MIPI-DSI

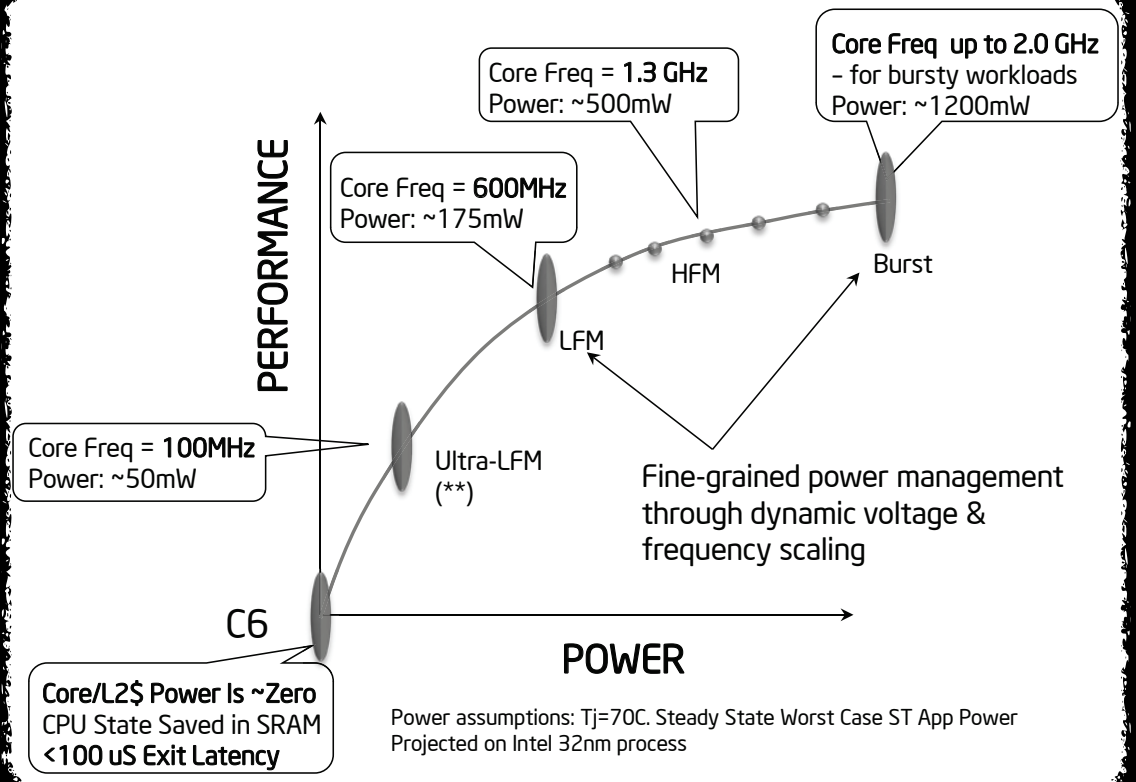
Internal Display

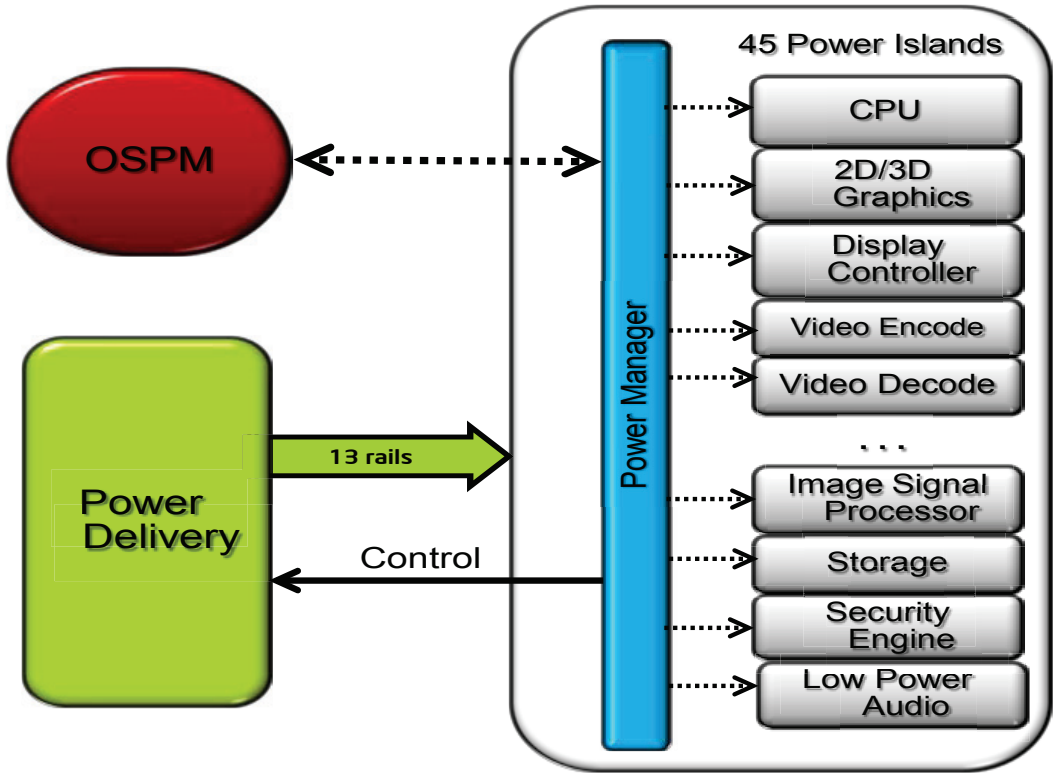
# Intel Medfield

Switches 45 power "islands."

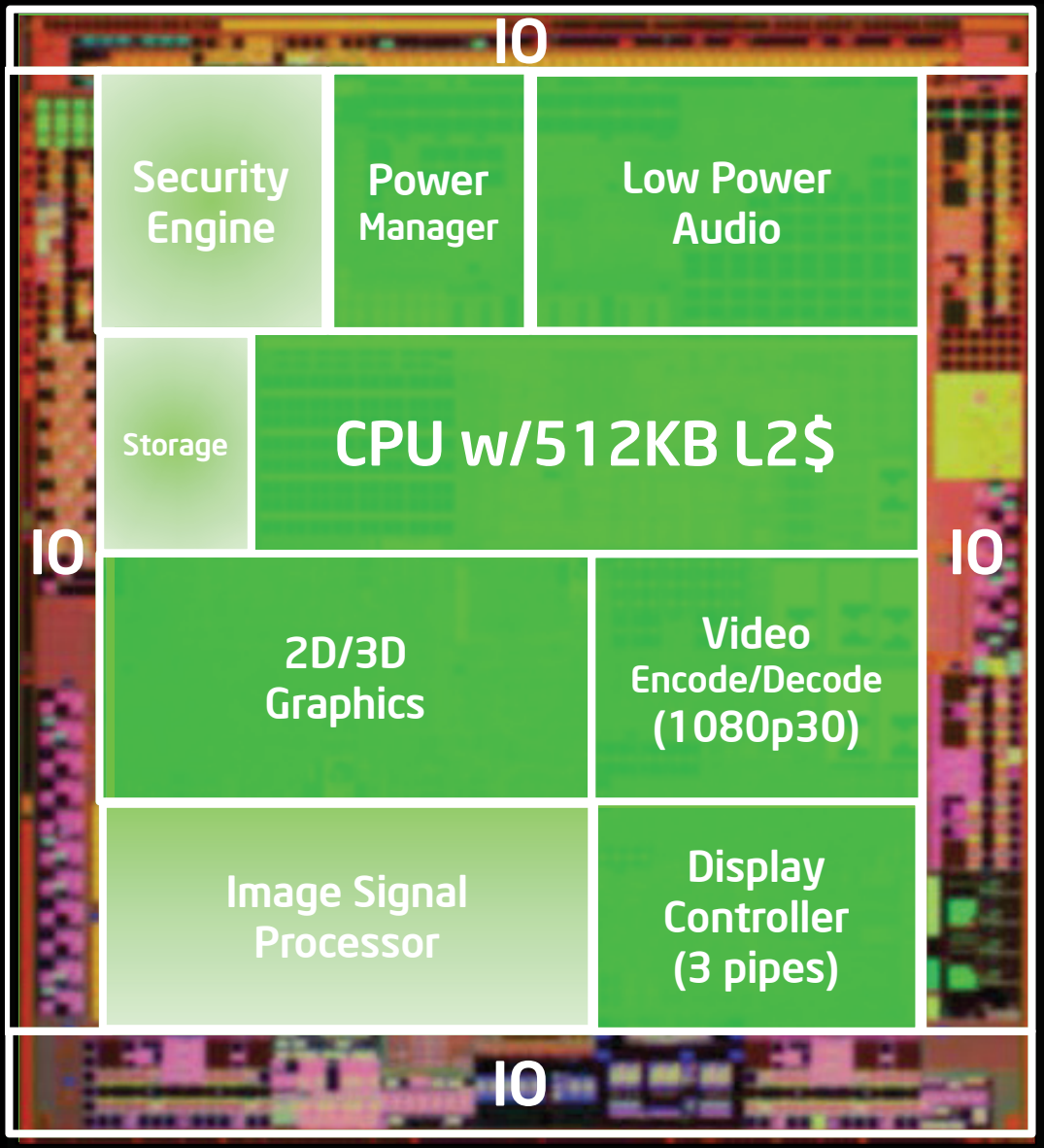
Fine-grained control of leakage power, to track user activity.

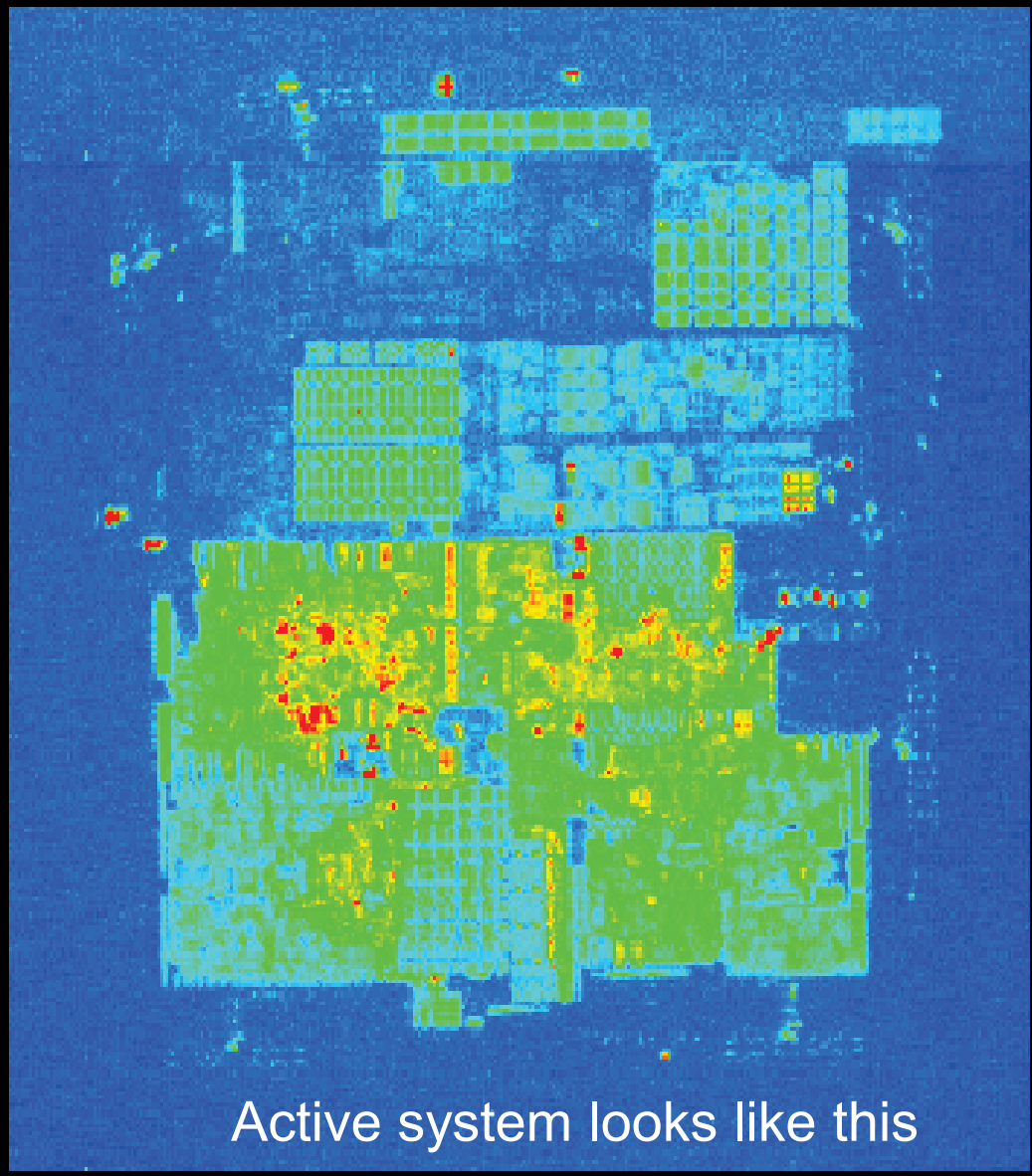
"Race to idle" strategy -- finish tasks quickly, to get to power down.



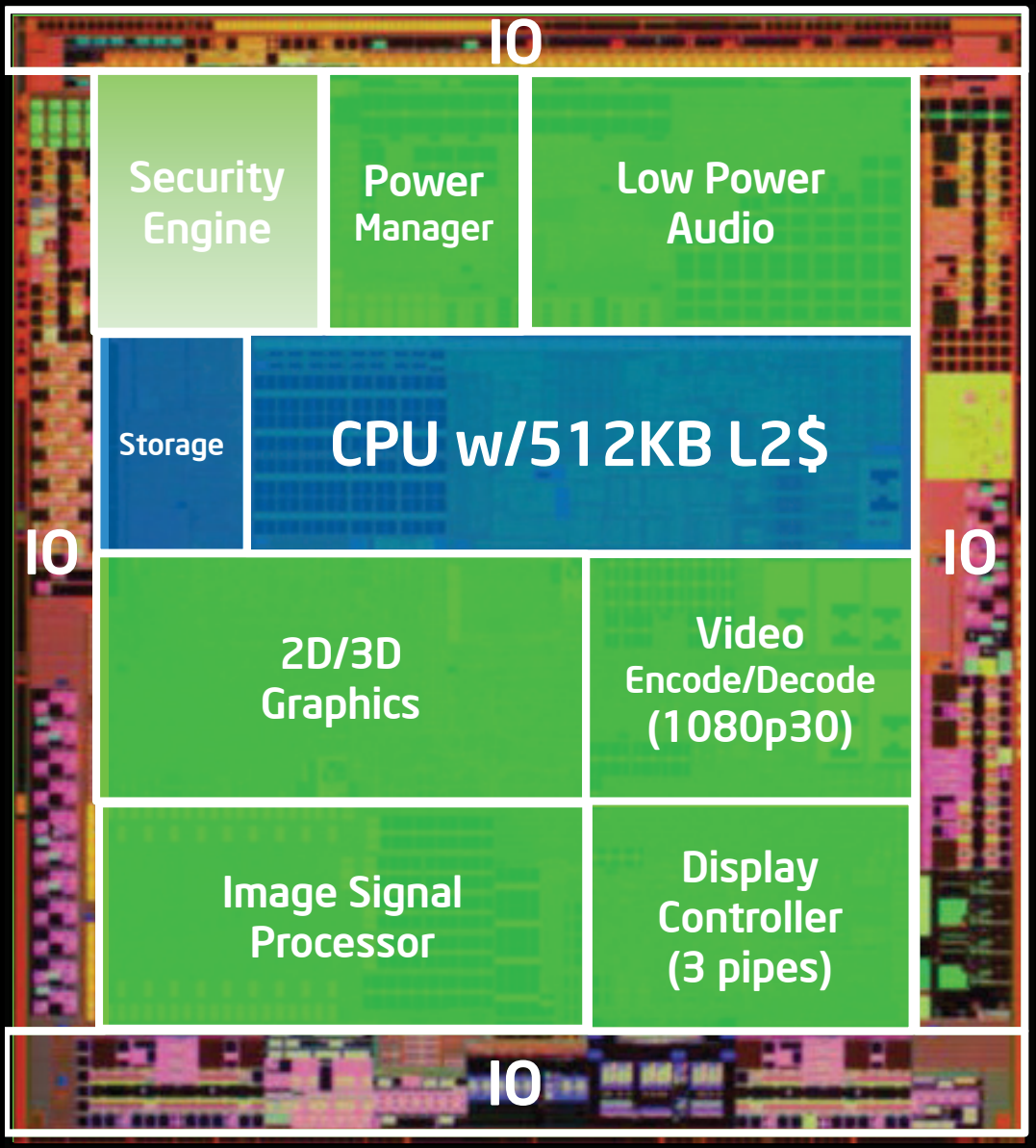



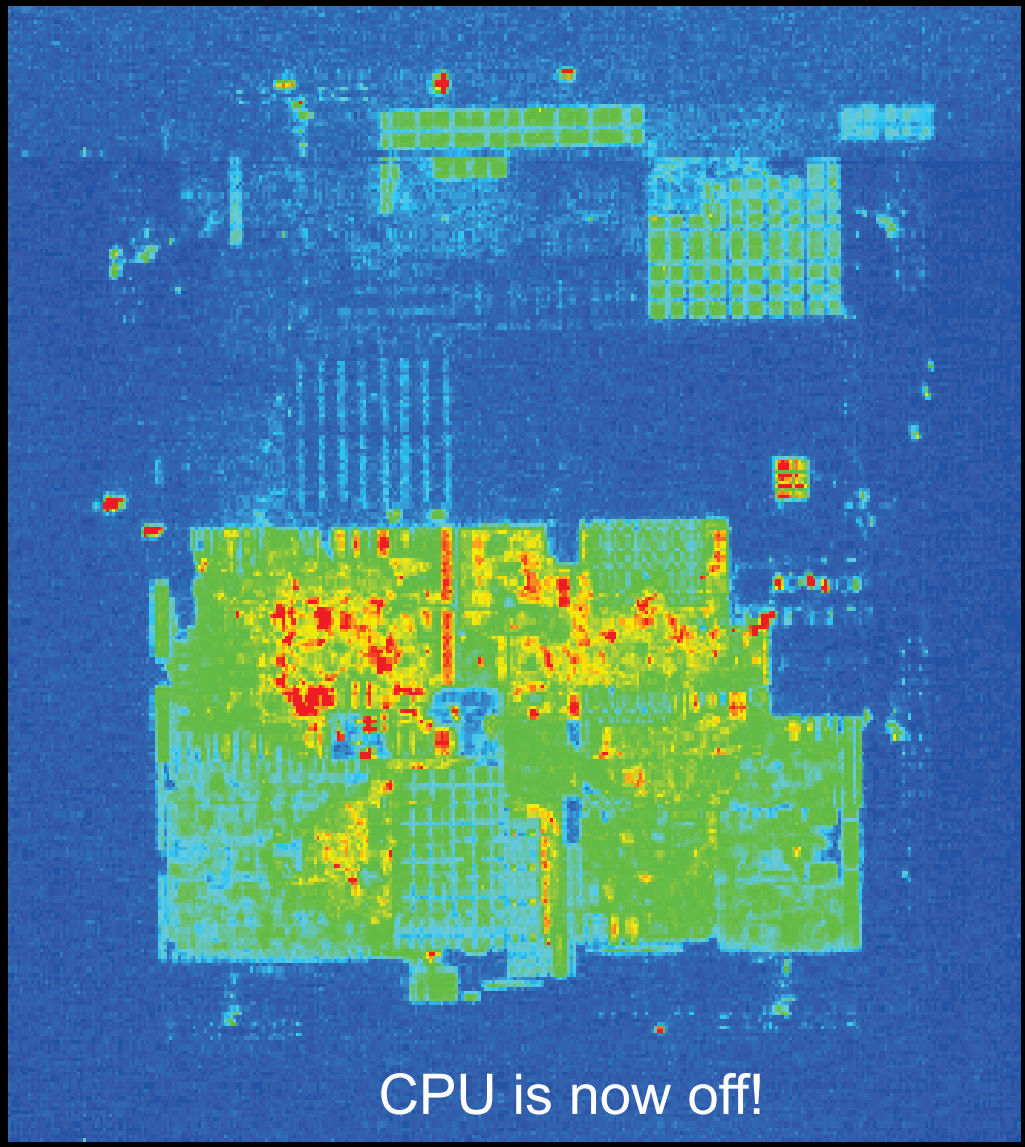
# Playing a game …



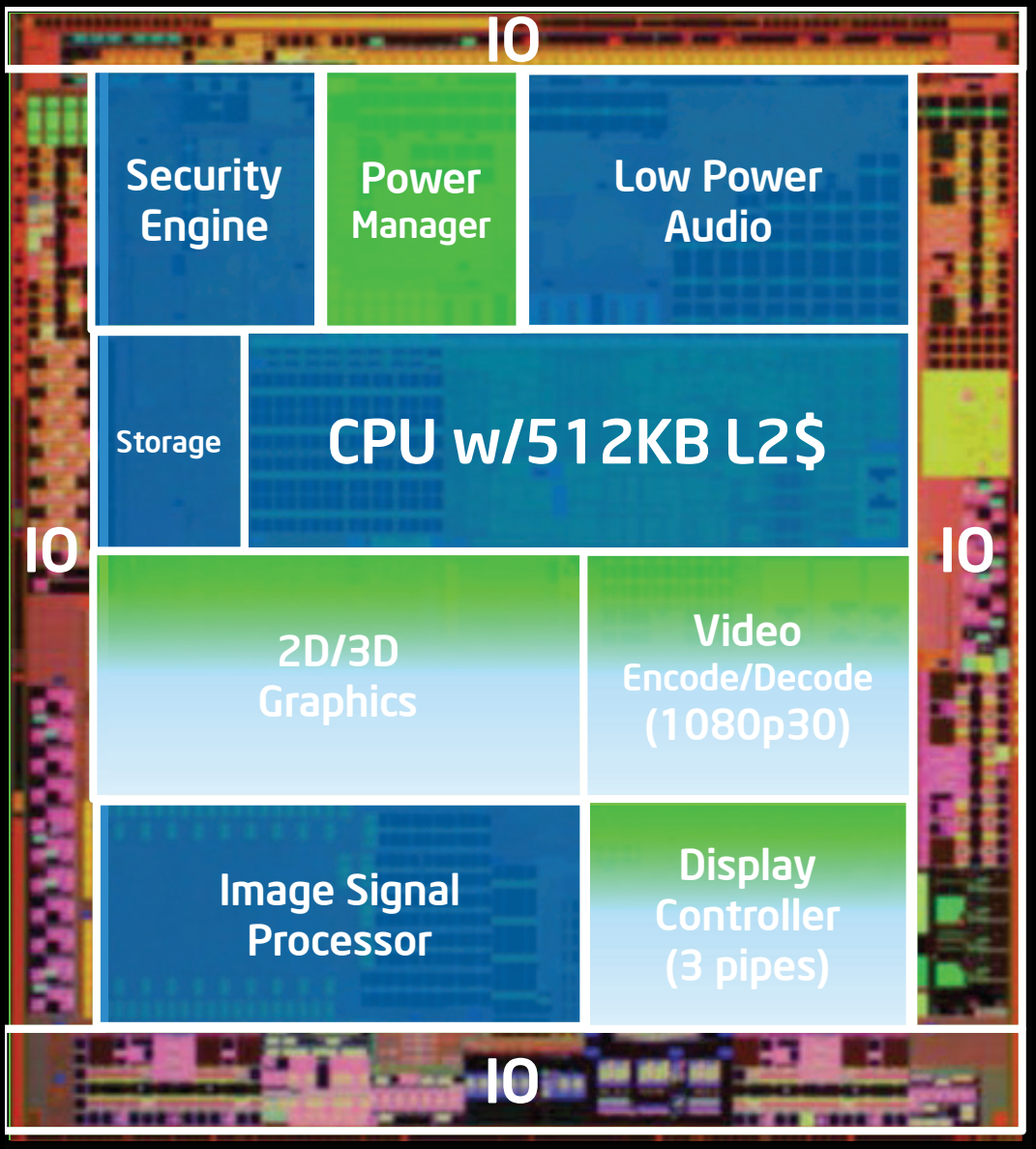



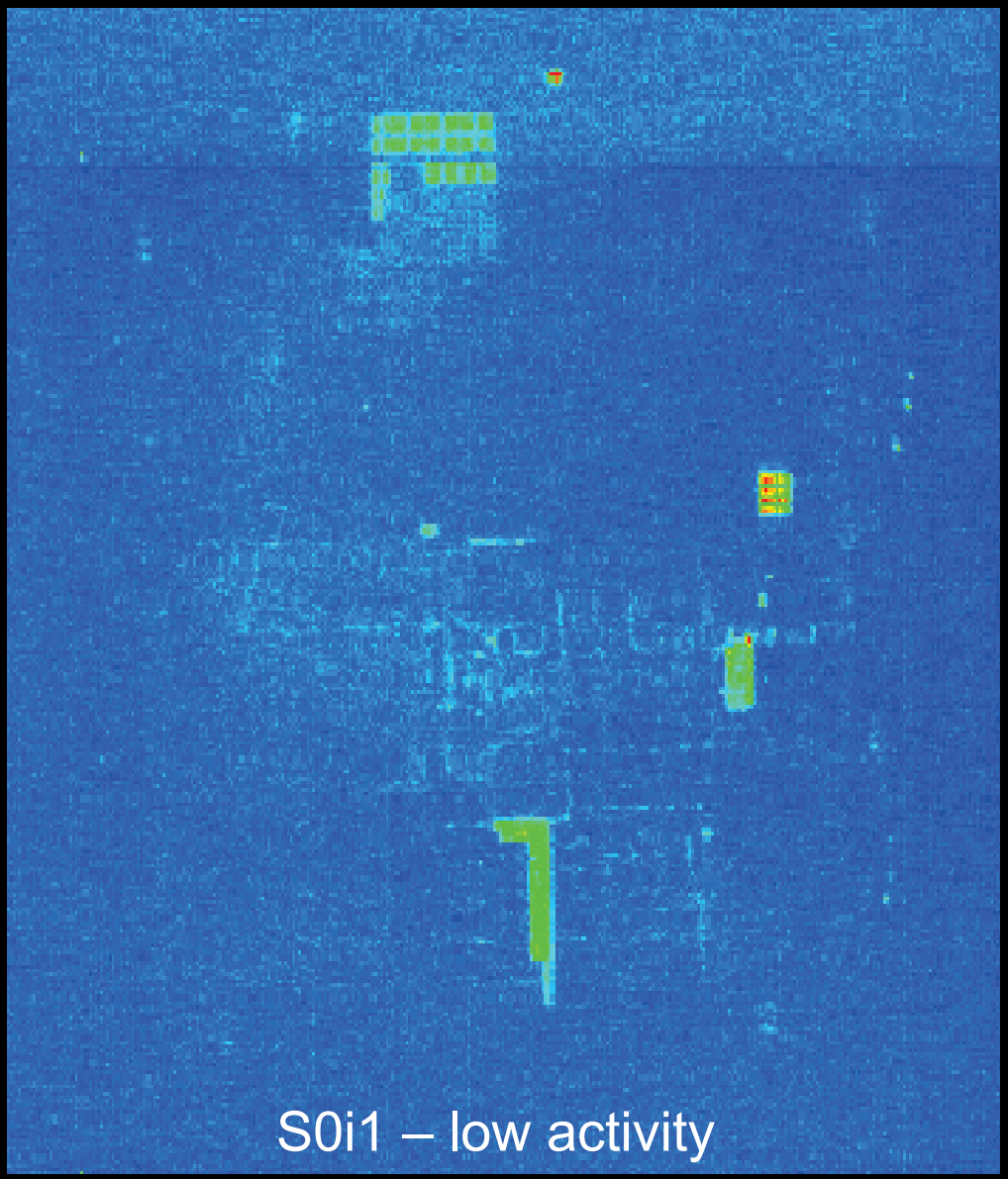
# Watching a video …



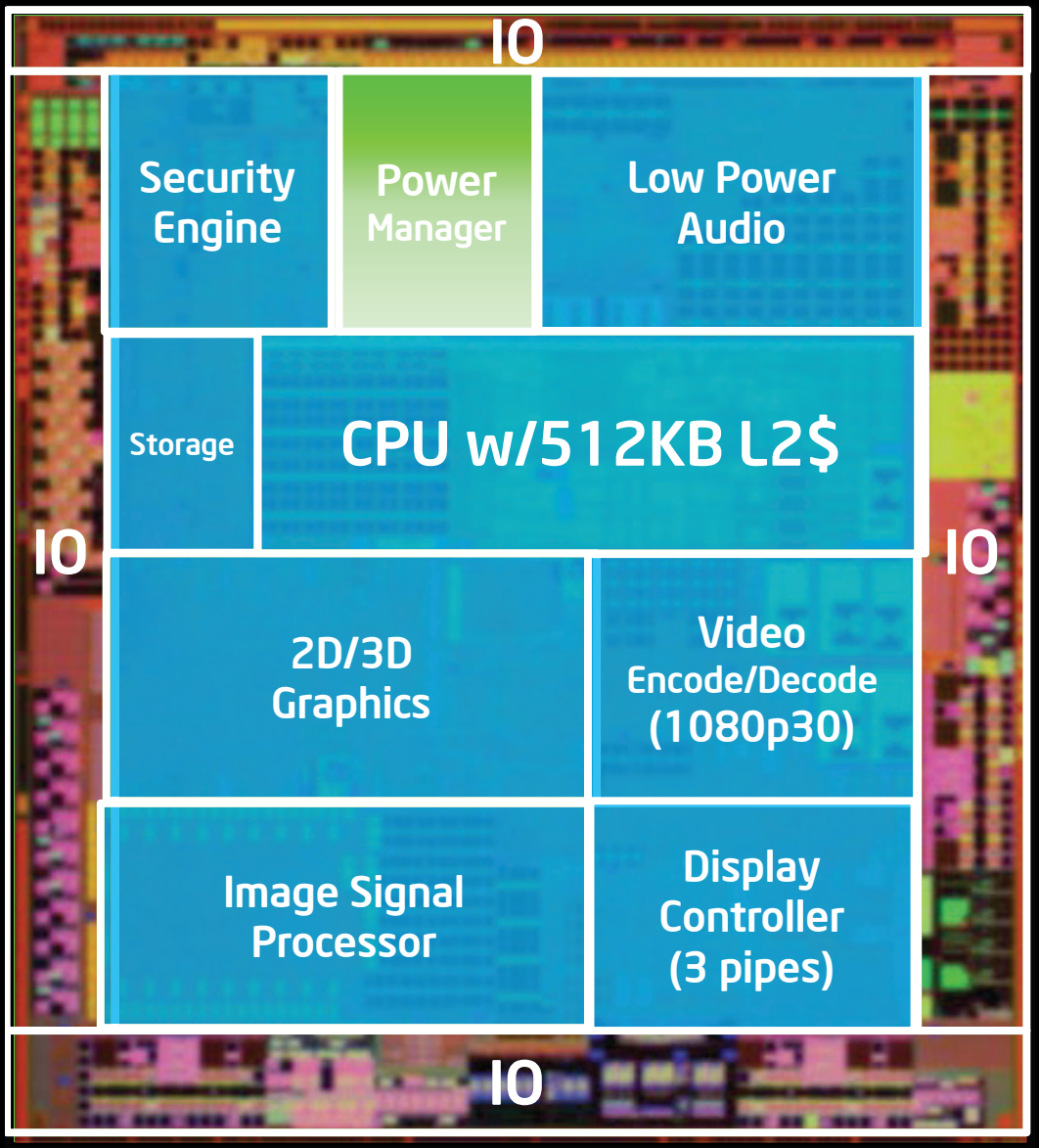



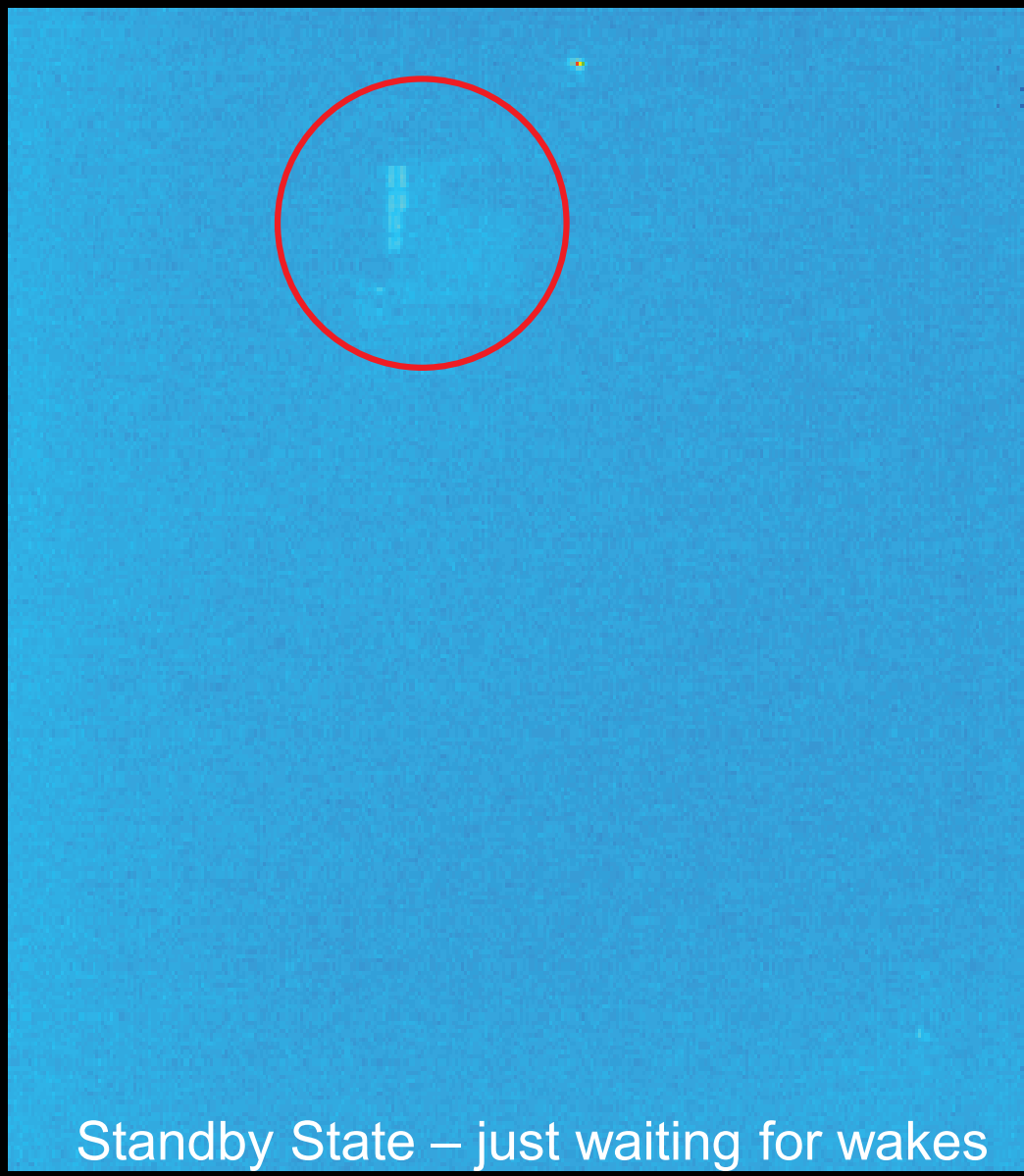
# Looking at phone screen, not doing anything …



# Phone in your pocket, waiting for a call …



Standby State – just waiting for wakes

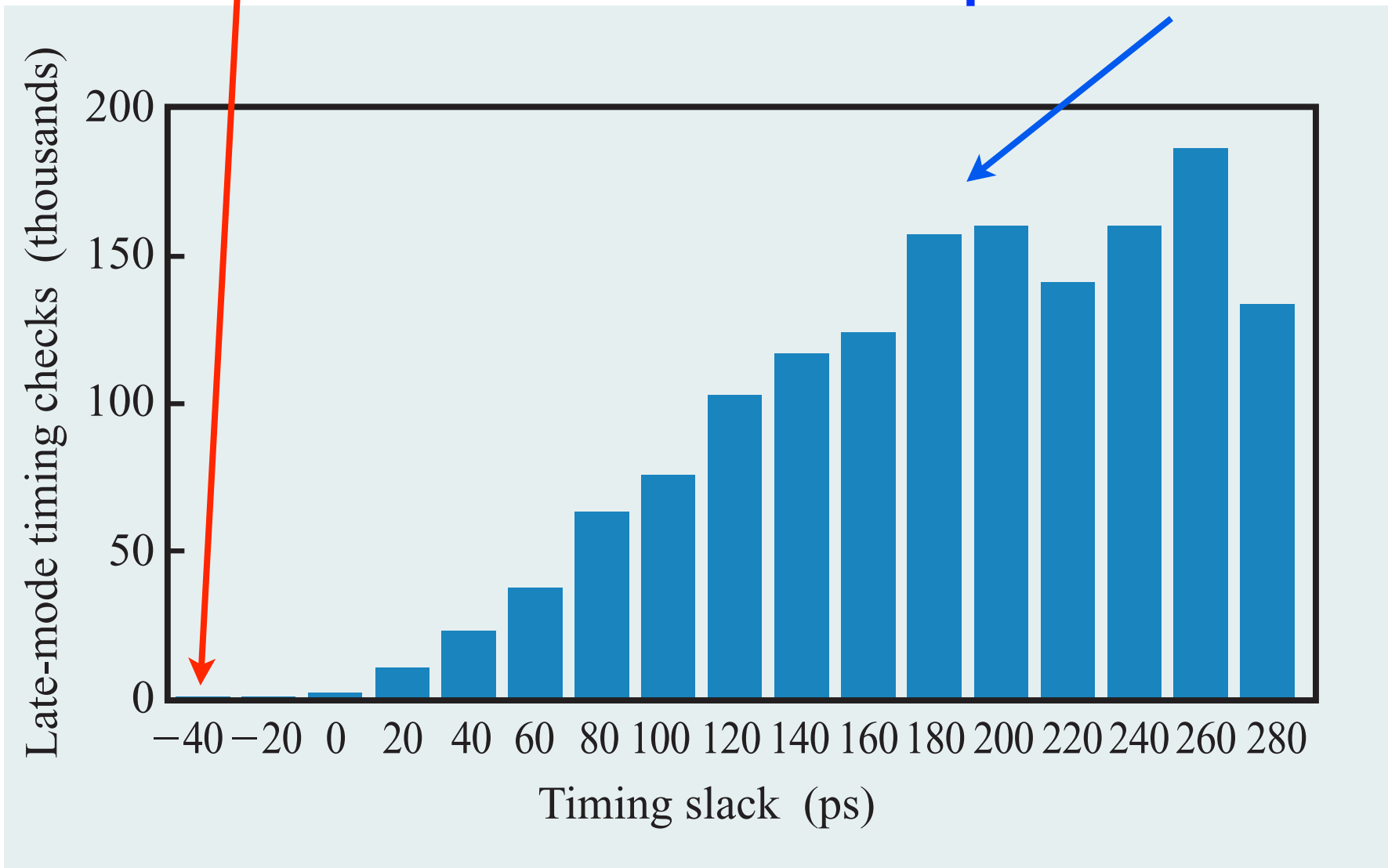
# Slow down "slack paths"

UC Regents Spring 2016 © UCB

# Fact: Most logic on a chip is "too fast"

The critical path

Most wires have hundreds of picoseconds to spare.

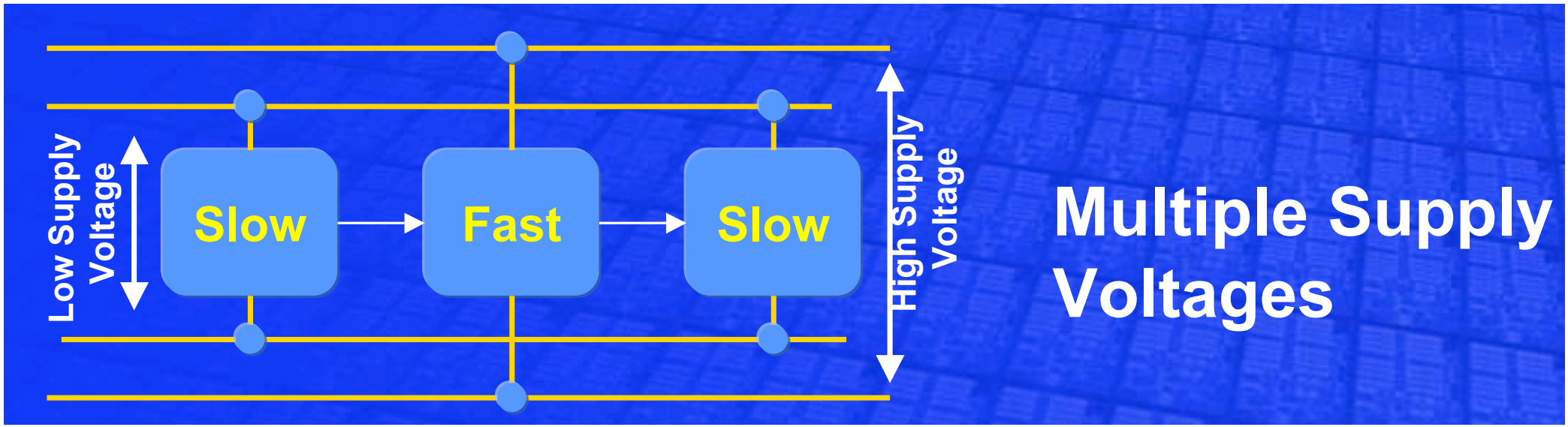



*From "The circuit and physical design of the POWER4 microprocessor", IBM J Res and Dev, 46:1, Jan 2002, J.D. Warnock et al.*



UC Regents Spring 2016 © UCB

# Use several supply voltages on a chip …




Why use multi-Vdd? We can reduce dynamic power by using low-power Vdd for logic off the critical path.

What if we can't do a multi-Vdd design?
In a multi-Vt process, we can reduce leakage power on the slow logic by using high-Vth transistors.

From: "Facing the Hot Chips Challenge Again", Bill Holt, Intel, presented at Hot Chips 17, 2005.


UC Regents Spring 2016 © UCB

# LOW POWER ARM 1136JF-S™ DESIGN

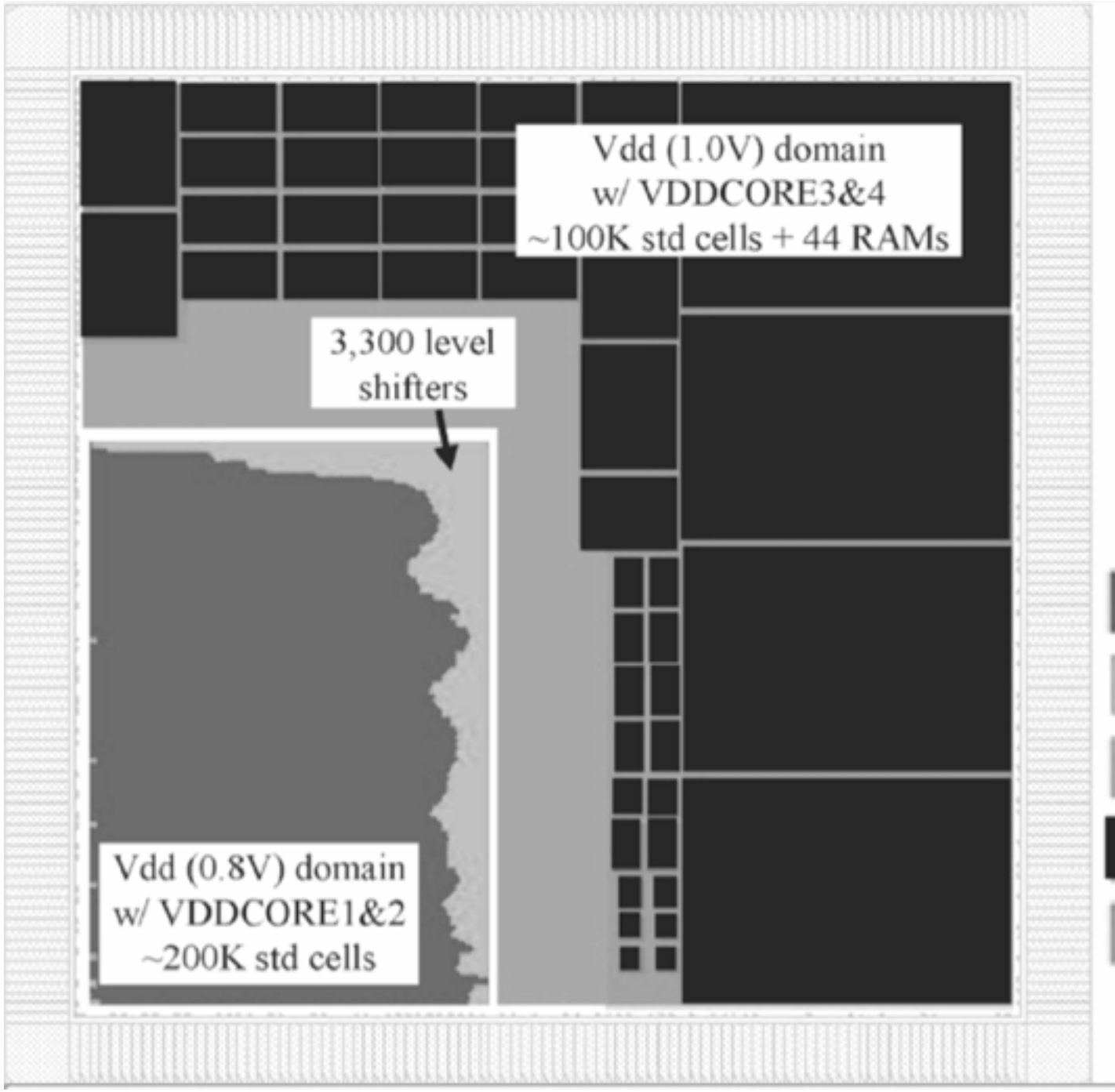
George Kuo, Anand Iyer
*Cadence Design Systems, Inc.*
*San Jose, CA 95134, USA*

Logical partition into 0.8V and 1.0V nets done manually to meet 350 MHz spec (90nm).

Level-shifter insertion and placement done automatically.

Dynamic power in 0.8V section cut 50% below baseline.

Leakage power in 1.0V section cut 70% by using high $V_T$.




From a chapter from new book on ASIC design by Chinnery and Keutzer (UCB).

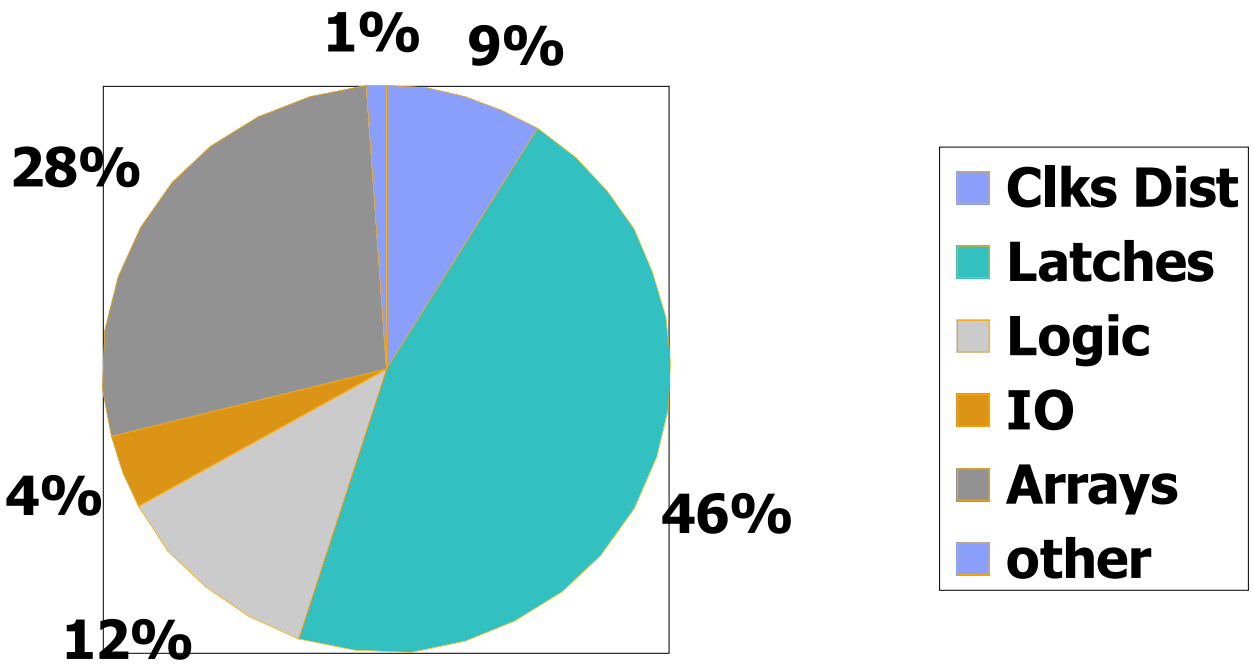


UC Regents Spring 2016 © UCB

# Gating clocks to save power

UC Regents Spring 2016 © UCB

# On a CPU, where does the power go?




Half of the power goes to latches (Flip-Flops).

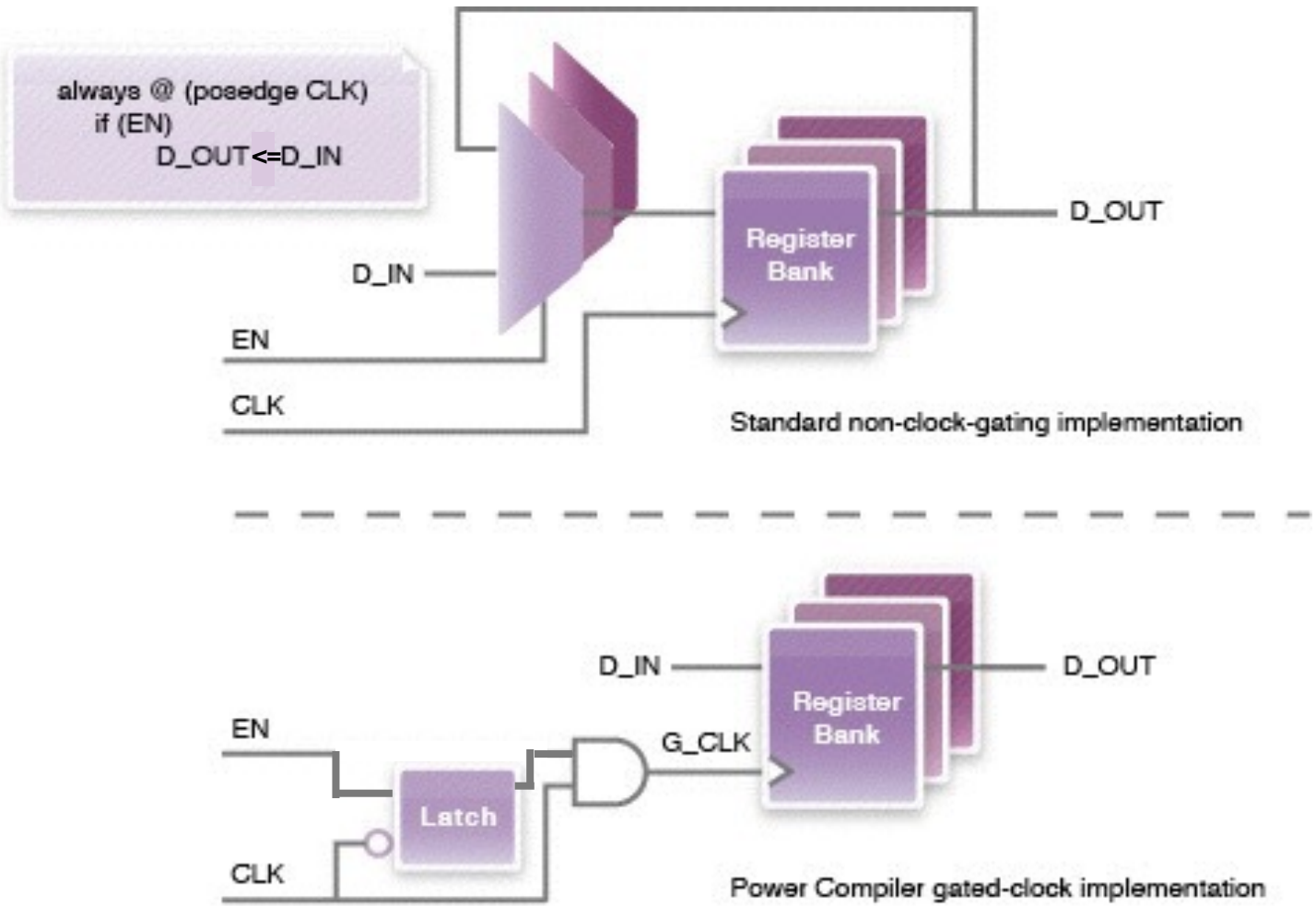
Most of the time, the latches don't change state.

So (gasp) gated clocks are a big win.
But, done with CAD tools in a disciplined way.

From: Bose, Martonosi, Brooks: Sigmetrics-2001 Tutorial


UC Regents Spring 2016 © UCB

# Synopsis Design Compiler can do this ...




"Up to 70% power savings at the block level, for applicable circuits"
Synopsis Data Sheet


UC Regents Spring 2016 © UCB

# Data-Dependent Processing

UC Regents Spring 2016 © UCB

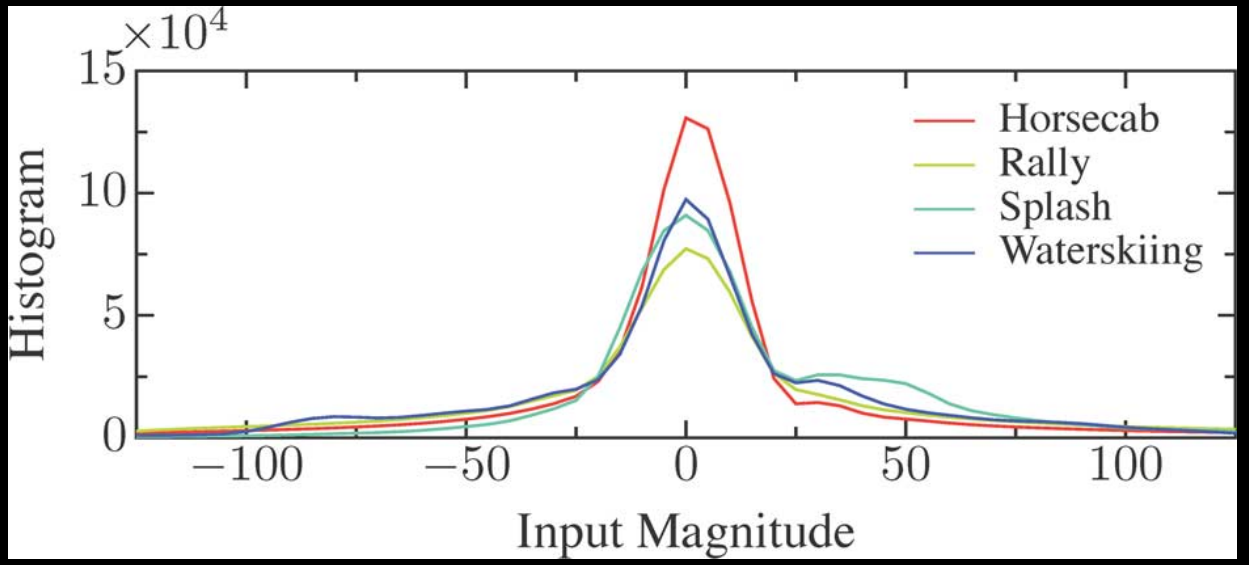
# Example: Video Decode Transform

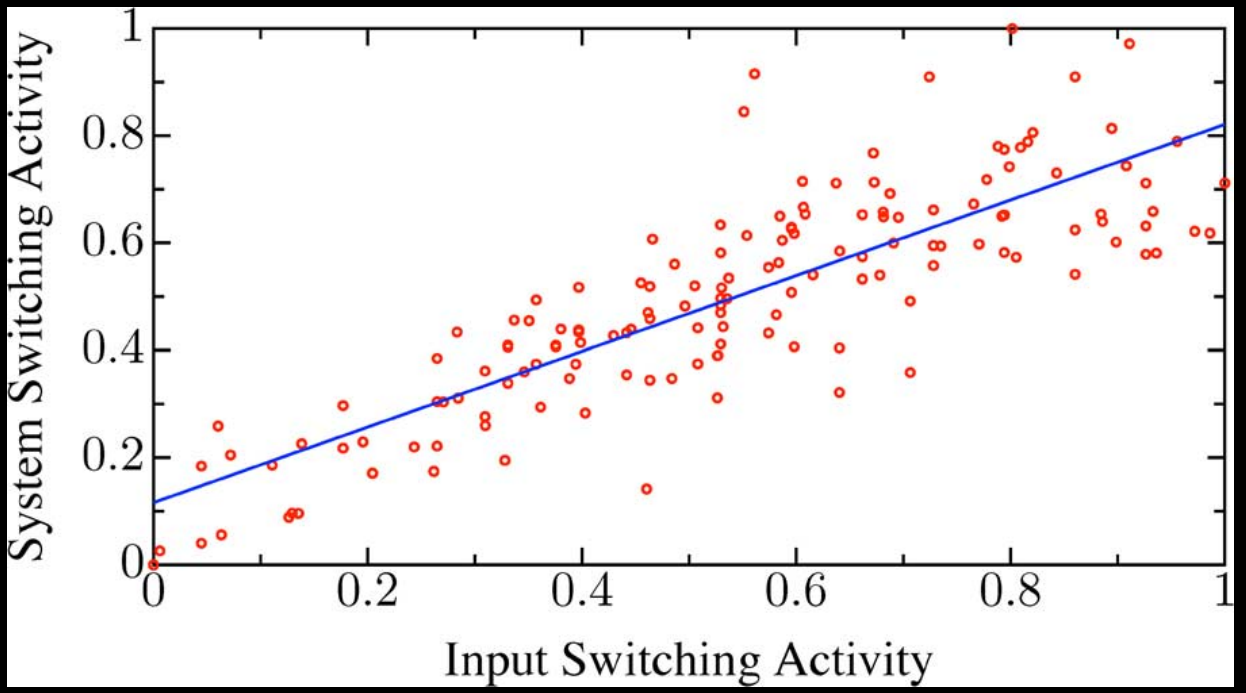
Most of the time, the inputs flip between small positive and negative integers.

In 2's complement, wastes power:

+1: 0b00001

-1: 0b11110



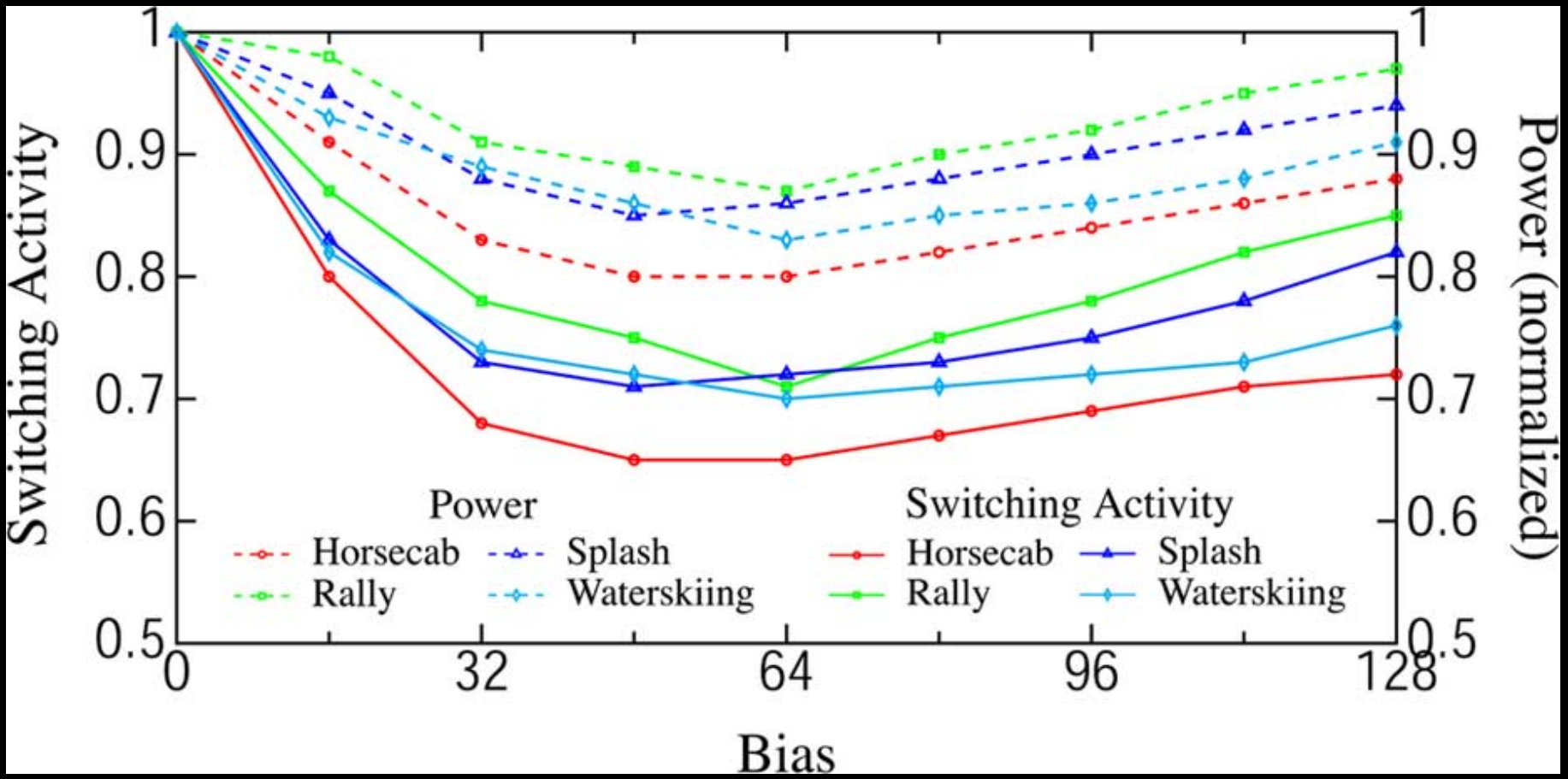




Quad Full-HD Transform Engine for Dual-Standard Low-Power Video Coding

Rahul Rithe, *Student Member, IEEE*, Chih-Chi Cheng, *Member, IEEE*, and Anantha P. Chandrakasan, *Fellow, IEEE*

# Solution: Add bias value to all inputs

30+% power reduction for a bias of 64. For this linear transform, correcting the output for the bias is trivial.




Quad Full-HD Transform Engine for Dual-Standard Low-Power Video Coding

Rahul Rithe, *Student Member, IEEE*, Chih-Chi Cheng, *Member, IEEE*, and Anantha P. Chandrakasan, *Fellow, IEEE*

# Thermal Management

UC Regents Spring 2016 © UCB

# Keep chip cool to minimize leakage power

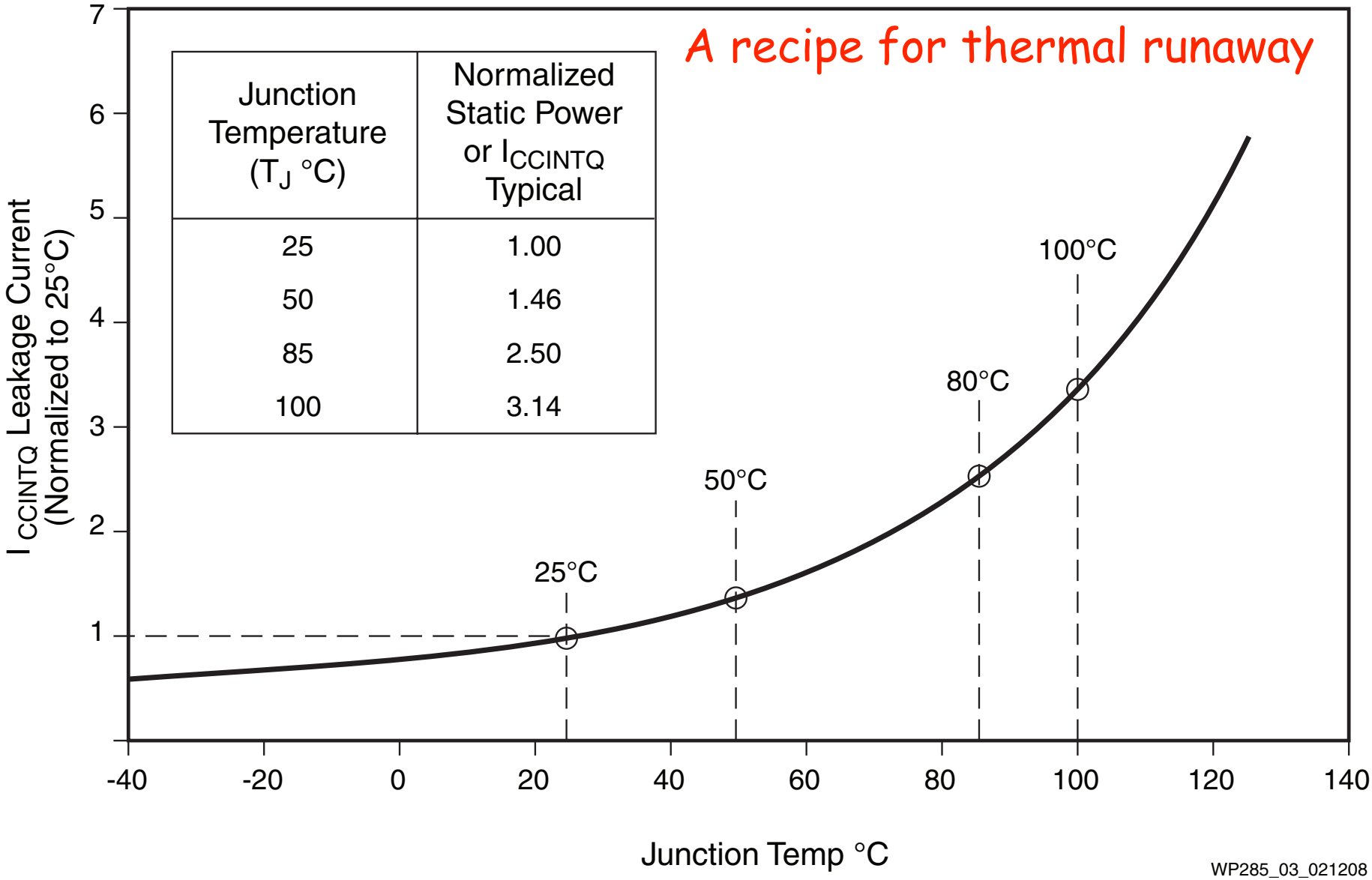
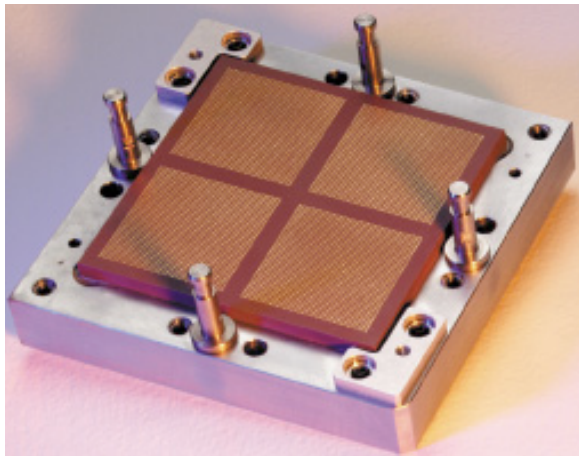


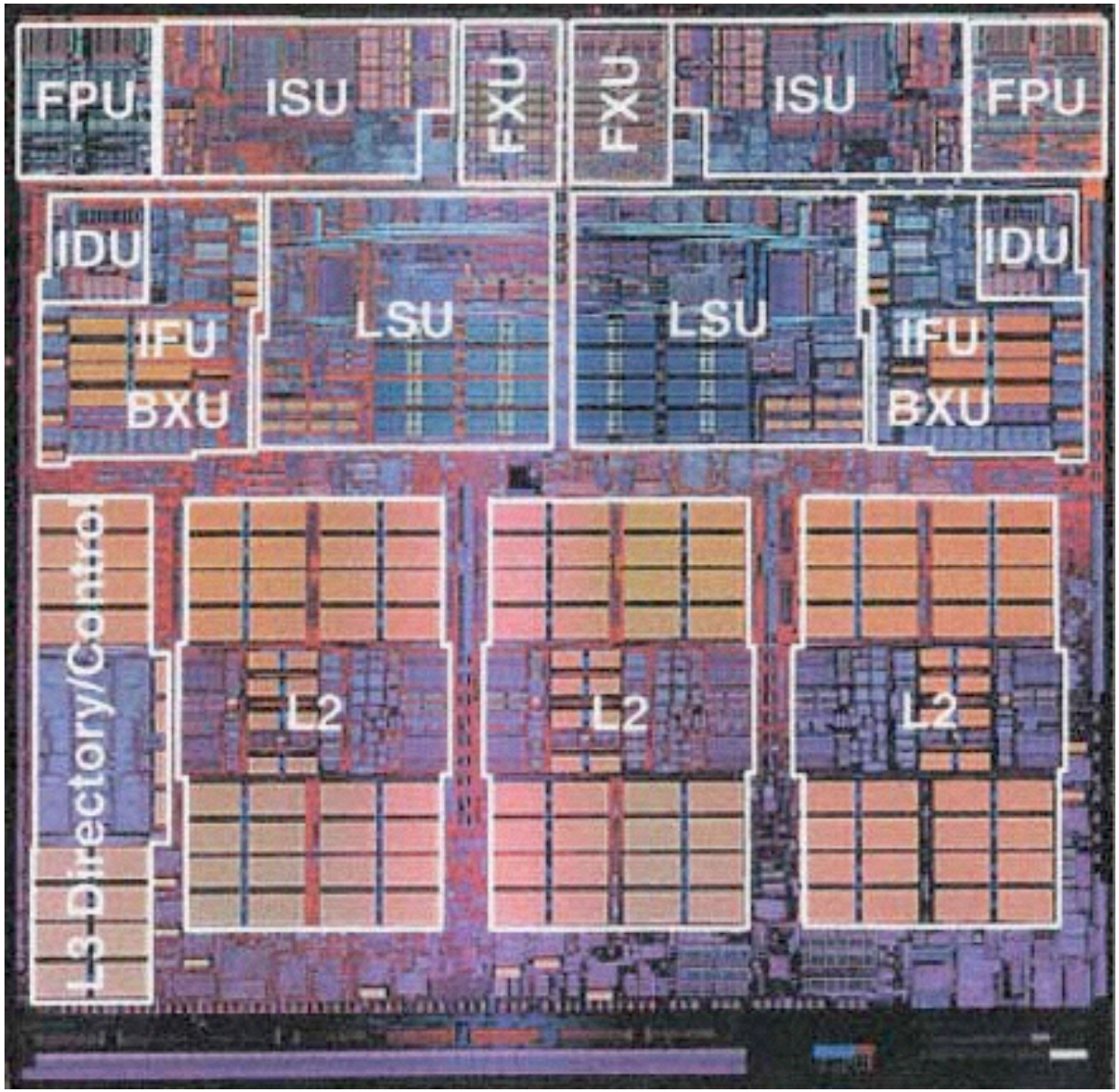

*Figure 3:* **$I_{CCINTQ}$ vs. Junction Temperature with Increase Relative to 25°C**

# IBM Power 4: How does die heat up?



4 dies on a multi-chip module

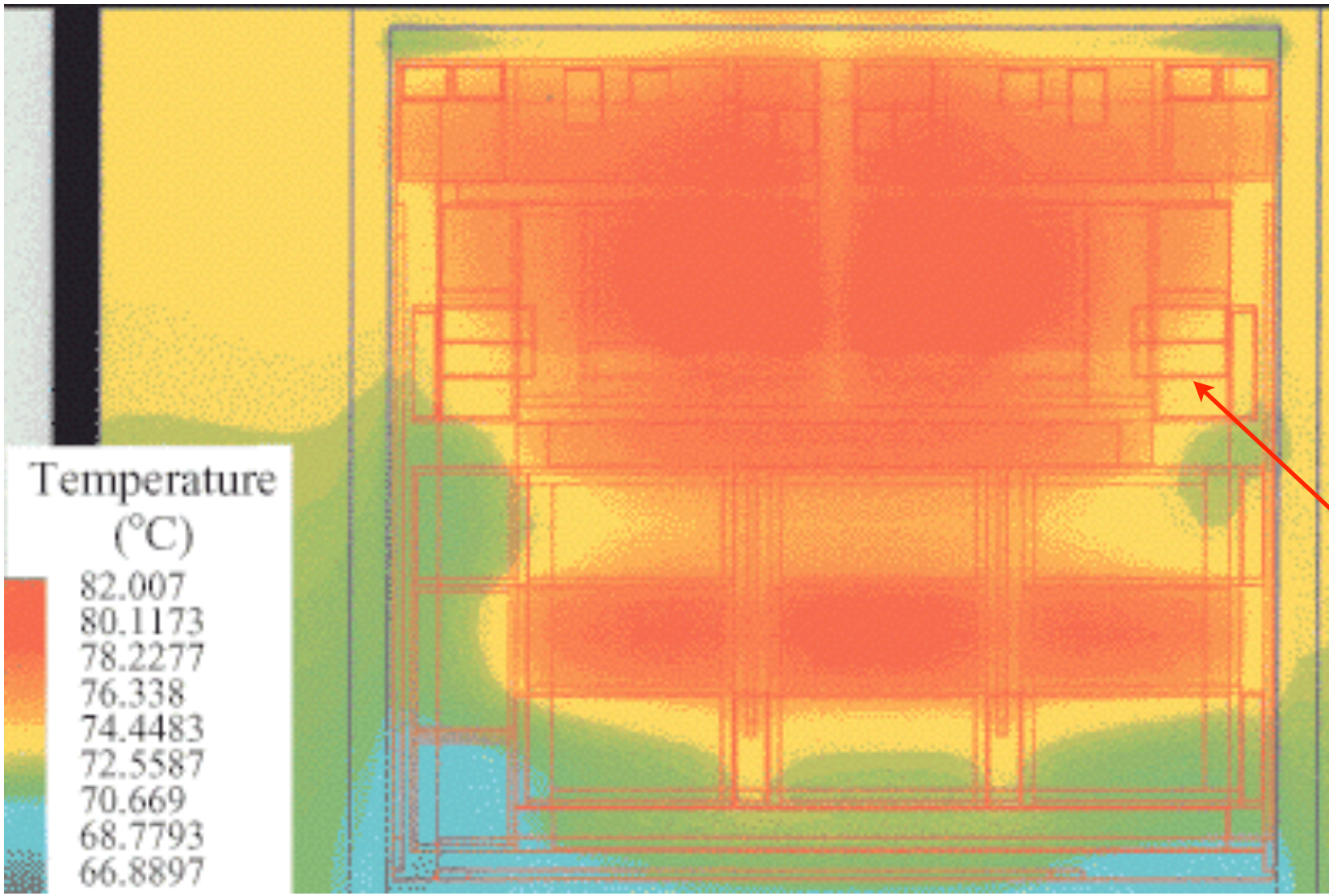
2 CPUs per die






UC Regents Spring 2016 © UCB

# 115 Watts: Concentrated in "hot spots"




Hot spots

Fixed point units

Cache logic

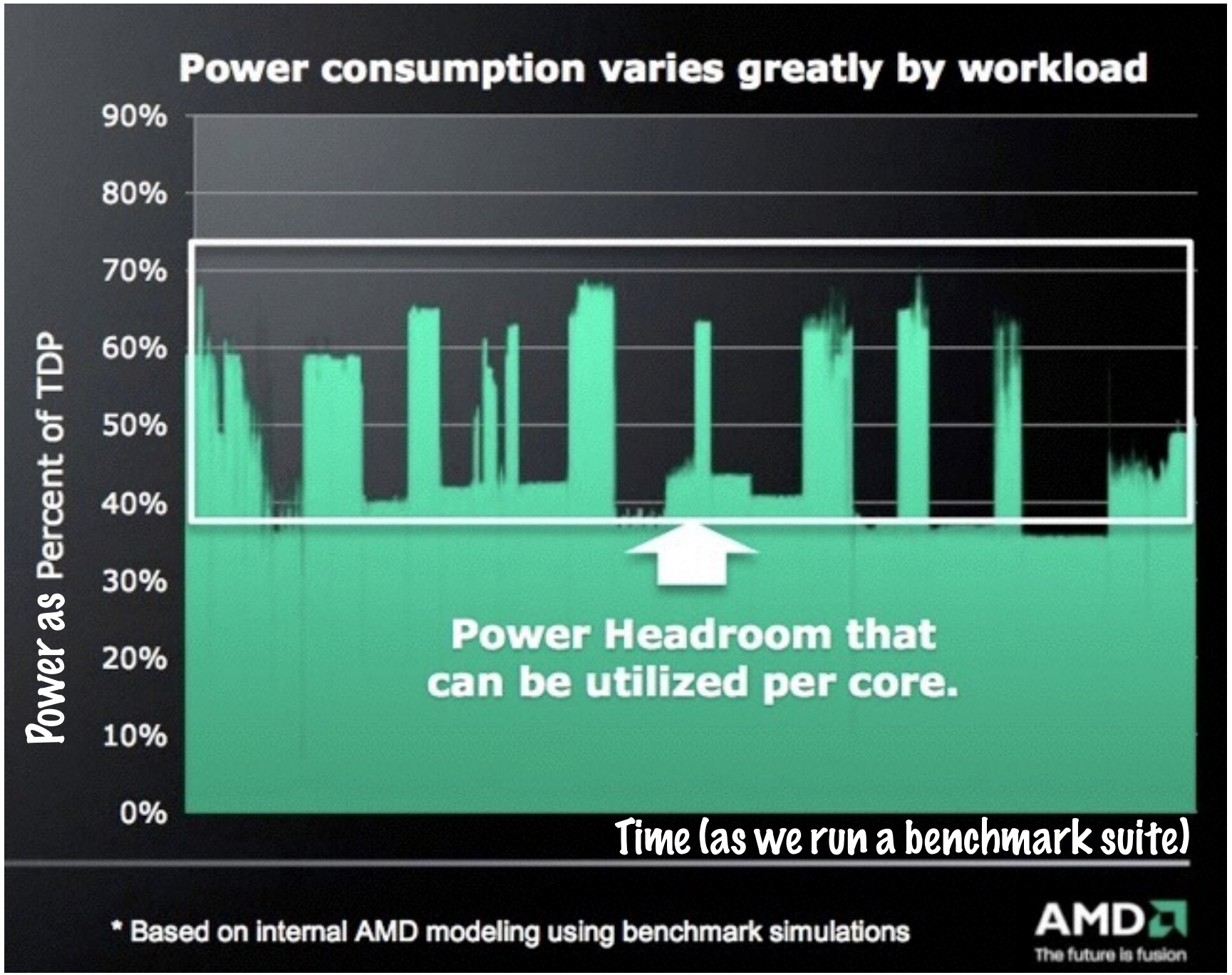
66.8 C == 152 F

82 C == 179.6 F



UC Regents Spring 2016 © UCB

# Idea: Monitor temperature, servo clock speed

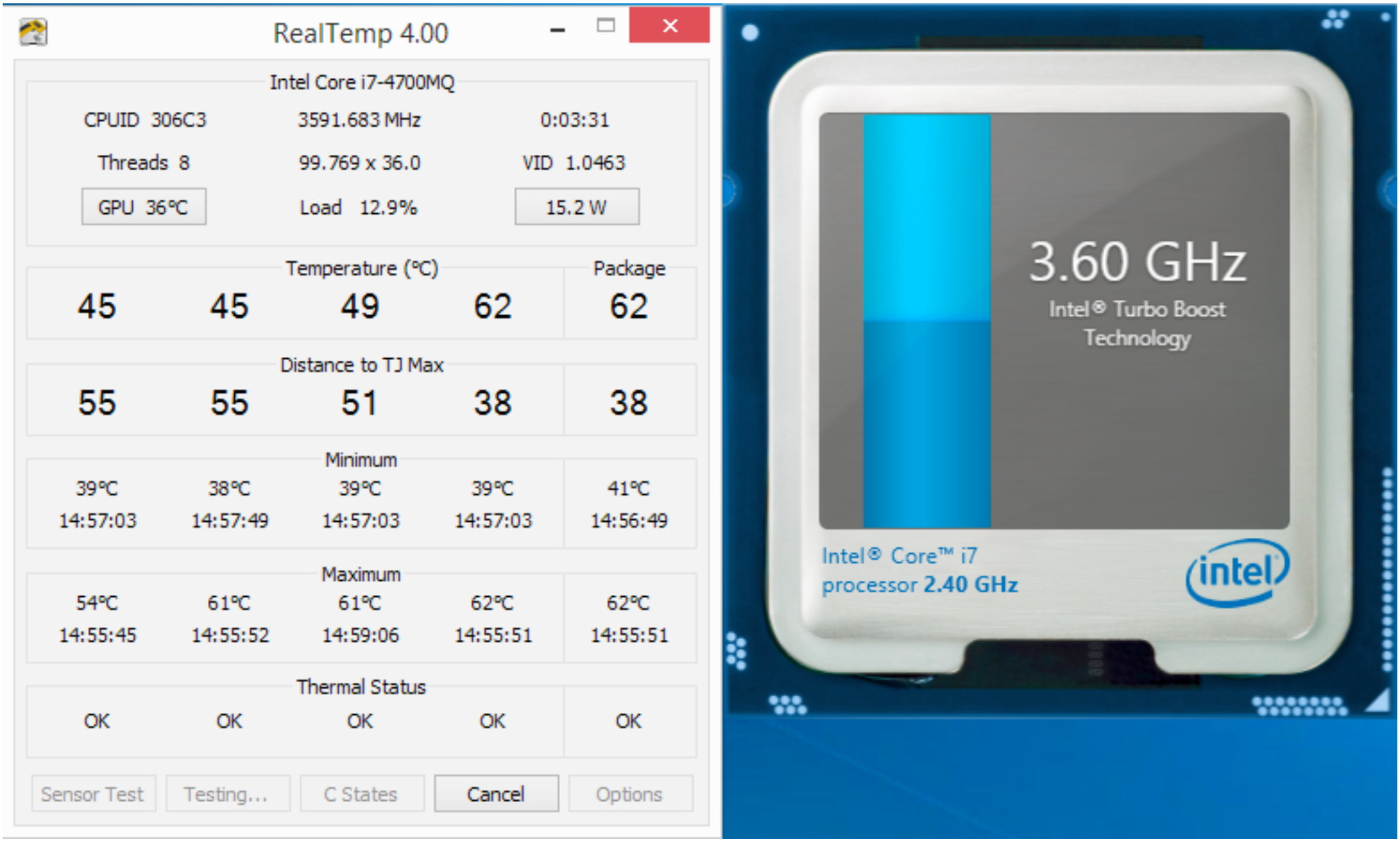



TDP = Thermal Design Point



UC Regents Spring 2016 © UCB

# Intel realtime temp monitoring






UC Regents Spring 2016 © UCB

# Six low-power design techniques

- Parallelism and pipelining
- Power-down idle transistors
- Slow down non-critical paths
- Clock gating
- Data-dependent processing
- Thermal management

UC Regents Spring 2016 © UCB