CS250 DISCUSSION #3

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Slides by Colin Schmidt
with modifications by Christopher Yarp

Std. Cell Slides adapted from Ben Keller

COURSE LIBRARIES

- Synopsys 32nm Educational Library

  - "saed" - Synopsys Armenia Educational

  - Can use without an NDA (not a real process)

  - Includes standard cells, SRAMs, memory compiler

  - Take a look: ~cs250/stdcells/synopsys-32nm/vendor

IMPORTANT COMPLIANCE INFORMATION

- DO NOT post course materials online

  - Synopsys libraries are for educational use only

  - Synopsys tools are **_very, very proprietary_**

  - Even methodology scripts should stay in your private repo

    - The Makefiles and tcl scripts are considered proprietary

SYNTHESIS REPORTS

- Using design compiler to synthesize your RTL to gates has multiple reports output

- You can find reports in build/vlsi/dc-syn/current-dc/reports

  - QOR (quality of results)

  - Timing

  - Area

  - Power

  - Clock-gating

  - Reference

  - Resources

QOR

- General overview of the results

- Timing summaries

- Cell counts

- Areas

- Etc.

```
Timing Path Group 'REGOUT'
------------------------------------
Levels of Logic:            20.00
Critical Path Length:        0.98
Critical Path Slack:         0.13
Critical Path Clk Period:    1.25
Total Negative Slack:        0.00
No. of Violating Paths:      0.00
Worst Hold Violation:        0.00
Total Hold Violation:        0.00
No. of Hold Violations:      0.00
------------------------------------


Timing Path Group 'clk'
------------------------------------
Levels of Logic:            22.00
Critical Path Length:        1.06
Critical Path Slack:         0.09
Critical Path Clk Period:    1.25
Total Negative Slack:        0.00
No. of Violating Paths:      0.00
Worst Hold Violation:        0.00
Total Hold Violation:        0.00
No. of Hold Violations:      0.00
------------------------------------


Cell Count
------------------------------------
Hierarchical Cell Count:        36
Hierarchical Port Count:     15602
Leaf Cell Count:             21063
Buf/Inv Cell Count:           5698
CT Buf/Inv Cell Count:           0
Combinational Cell Count:    18023
Sequential Cell Count:        3040
Macro Count:                     0
------------------------------------


Area
------------------------------------
Combinational Area:     45291.002973
Noncombinational Area:  20570.924212
Buf/Inv Area:           10445.572885
Net Area:                   0.000000
Net XLength       :      329111.72
Net YLength       :      302961.09
------------------------------------
Cell Area:              65861.927185
Design Area:            65861.927185
Net Length        :      632072.81


Design Rules
------------------------------------
Total Number of Nets:        22252
Nets With Violations:          106
Max Trans Violations:            0
Max Cap Violations:            106
------------------------------------
```

TIMING

- Shows multiple path groups

  - we care about "clk"

- Detailed analysis of timing

- Top N critical paths

  - Broken down by delay

- Goto for optimizing critical paths

- If slack is negative, you did not meet timing

- Unit is typically ns

```
Startpoint: ctrl/read_reg_3_
            (rising edge-triggered flip-flop clocked by clk)
Endpoint: ctrl/clk_gate_mem_s_reg/latch
          (gating element for clock clk)
Path Group: clk
Path Type: max

Point                                         Fanout      Cap     Trans      Incr       Path
------------------------------------------------------------------------------------------------
clock clk (rise edge)                                                        0.0000     0.0000
clock network delay (ideal)                                                 0.0000     0.0000
ctrl/read_reg_3_/CLK (DFFX1_RVT)                                 0.0000     0.0000     0.0000 r
ctrl/read_reg_3_/Q (DFFX1_RVT)                                   0.0399     0.1021     0.1021 f
ctrl/T134[3] (net)                             7     5.1830      0.0000     0.1021 f
ctrl/add_x_7_U126/A2 (NAND2X0_RVT)                               0.0399     0.0000 *   0.1021 f
ctrl/add_x_7_U126/Y (NAND2X0_RVT)                                0.0459     0.0466     0.1488 r
ctrl/add_x_7_n101 (net)                        2     2.1347      0.0000     0.1488 r
ctrl/add_x_7_U116/A1 (NOR2X0_RVT)                                0.0459     0.0000 *   0.1488 r
ctrl/add_x_7_U116/Y (NOR2X0_RVT)                                 0.0247     0.0590     0.2078 f
ctrl/add_x_7_n93 (net)                         2     2.9734      0.0000     0.2078 f
ctrl/add_x_7_U95/A2 (NAND2X2_RVT)                                0.0247     0.0001 *   0.2079 f
ctrl/add_x_7_U95/Y (NAND2X2_RVT)                                 0.0184     0.0533     0.2611 r
ctrl/add_x_7_n76 (net)                         2     3.3858      0.0000     0.2611 r
ctrl/U778/A (INVX1_RVT)                                          0.0184     0.0001 *   0.2612 r
ctrl/U778/Y (INVX1_RVT)                                          0.0268     0.0224     0.2836 f
ctrl/add_x_7_n75 (net)                         4     3.4106      0.0000     0.2836 f
ctrl/add_x_7_U73/A1 (NAND2X0_RVT)                                0.0268     0.0000 *   0.2837 f
ctrl/add_x_7_U73/Y (NAND2X0_RVT)                                 0.0358     0.0351     0.3188 r
...
ctrl/lt_x_13_n2 (net)                          1     1.2469      0.0000     0.8804 r
ctrl/lt_x_13_U1/A2 (NOR2X2_RVT)                                  0.0327     0.0000 *   0.8804 r
ctrl/lt_x_13_U1/Y (NOR2X2_RVT)                                   0.0178     0.0509     0.9313 f
ctrl/T192 (net)                                1     2.6165      0.0000     0.9313 f
ctrl/U1253/A1 (NAND2X0_RVT)                                      0.0178     0.0001 *   0.9313 f
ctrl/U1253/Y (NAND2X0_RVT)                                       0.0607     0.0433     0.9747 r
ctrl/n599 (net)                                3     3.0593      0.0000     0.9747 r
ctrl/U1324/A1 (NAND2X0_RVT)                                      0.0607     0.0000 *   0.9747 r
ctrl/U1324/Y (NAND2X0_RVT)                                       0.0355     0.0199     0.9946 f
ctrl/n591 (net)                                1     0.5392      0.0000     0.9946 f
ctrl/U1325/A1 (AND2X1_RVT)                                       0.0355     0.0000 *   0.9946 f
ctrl/U1325/Y (AND2X1_RVT)                                        0.0191     0.0389     1.0335 r
ctrl/N402 (net)                                2     1.4986      0.0000     1.0335 r
ctrl/U733/A2 (OR2X1_RVT)                                         0.0191     0.0000 *   1.0335 r
ctrl/U733/Y (OR2X1_RVT)                                          0.0164     0.0262     1.0597 r
ctrl/N400 (net)                                1     0.4812      0.0000     1.0597 r
ctrl/clk_gate_mem_s_reg/EN (SNPS_CLOCK_GATE_HIGH_CtrlModule_8)              0.0000     1.0597 r
ctrl/clk_gate_mem_s_reg/EN (net)                     0.4812      0.0000     1.0597 r
ctrl/clk_gate_mem_s_reg/latch/EN (CGLPPRX2_RVT)                  0.0164     0.0000 *   1.0597 r
data arrival time                                                                      1.0597

clock clk (rise edge)                                                       1.2500     1.2500
clock network delay (ideal)                                                 0.0000     1.2500
clock uncertainty                                                          -0.0400     1.2100
ctrl/clk_gate_mem_s_reg/latch/CLK (CGLPPRX2_RVT)                            0.0000     1.2100 r
clock gating setup time                                                    -0.0583     1.1517
data required time                                                                     1.1517
------------------------------------------------------------------------------------------------
data required time                                                                     1.1517
data arrival time                                                                     -1.0597
------------------------------------------------------------------------------------------------
slack (MET)                                                                            0.0920
```

AREA

- Breakdown of area per nameable unit

- Summary at top

- Combinational vs Noncombinational

- Units typically μm²

```
Number of ports:                        2117
Number of nets:                         2012
Number of cells:                         417
Number of combinational cells:           415
Number of sequential cells:                0
Number of macros:                          0
Number of buf/inv:                       219
Number of references:                     14

Combinational area:         45291.002973
Buf/Inv area:               10445.572885
Noncombinational area:      20570.924212
Net Interconnect area:         undefined  (Wire load has zero net area)

Total cell area:            65861.927185
Total area:                    undefined

Hierarchical area distribution
------------------------------
```

	Global cell area		Local cell area			
Hierarchical cell	Absolute Total	Percent Total	Combi-national	Noncombi-national	Black boxes	Design
Sha3Accel	65861.9272	100.0	969.5594	0.0000	0.0000	Sha3Ac
ctrl	19413.2980	29.5	9716.6876	9532.9417	0.0000	CtrlMo
ctrl/clk_gate_buffer_0_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_buffer_10_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_buffer_11_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_buffer_12_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
..						
ctrl/clk_gate_buffer_8_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_buffer_9_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_buffer_count_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_hash_addr_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_hashed_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_mem_s_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_msg_addr_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_msg_len_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_read_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_rindex_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_windex_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
ctrl/clk_gate_words_filled_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
dpath	45479.0698	69.1	8780.6754	10862.6231	0.0000	DpathM
dpath/ChiModule	9767.0082	14.8	9767.0082	0.0000	0.0000	ChiMod
dpath/RhoPiModule	1735.8036	2.6	1735.8036	0.0000	0.0000	RhoPiM
dpath/ThetaModule	10984.3579	16.7	10984.3579	0.0000	0.0000	ThetaM
dpath/clk_gate_state_24_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
dpath/clk_gate_state_3_reg	5.8453	0.0	0.0000	5.8453	0.0000	SNPS_C
dpath/iota	3336.9109	5.1	3336.9109	0.0000	0.0000	IotaMo
Total			45291.0030	20570.9242	0.0000	

POWER

- Operating point listed at top

- Power per module

- Dynamic (Switching + Internal)

- Static (Leak)

- Careful of units (defined at top)

```
Library(s) Used:

    saed32rvt_tt1p05v25c (File: /home/ff/cs250/stdcells/synopsys-32nm/typical_rvt/db/cells.db)


Operating Conditions: tt1p05v25c   Library: saed32rvt_tt1p05v25c
Wire Load Model Mode: Inactive.


Global Operating Voltage = 1.05
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW     (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------------------
                                 Switch    Int     Leak     Total
Hierarchy                        Power     Power   Power    Power    %
--------------------------------------------------------------------------------
Sha3Accel                        2.61e+03 8.75e+03 9.35e+09 2.07e+04 100.0
  dpath (DpathModule)            1.18e+03 4.27e+03 6.80e+09 1.23e+04  59.2
    iota (IotaModule)               3.989    6.275 8.25e+08  835.481   4.0
    ChiModule (ChiModule)           5.527    9.202 9.84e+08  998.644   4.8
    RhoPiModule (RhoPiModule)       4.357    2.847 4.60e+08  467.565   2.3
    ThetaModule (ThetaModule)      17.057   25.012 1.58e+09 1.62e+03   7.8
  ctrl (CtrlModule)              1.33e+03 4.44e+03 2.35e+09 8.12e+03  39.2
```

CLOCK GATING

- Simple results of tools attempt to clock gate everything

- Does a very good job for our accelerator

```
                Clock Gating Summary
-----------------------------------------------------------
| Number of Clock gating elements  |        30           |
|                                  |                     |
| Number of Gated registers        |   2897 (96.25%)     |
|                                  |                     |
| Number of Ungated registers      |    113 (3.75%)      |
|                                  |                     |
| Total number of registers        |       3010          |
-----------------------------------------------------------
```

REFERENCE

- Shows which standard cells were used in each module


```
Attributes:
    b - black box (unknown)
    bo - allows boundary optimization
    d - dont_touch
    mo - map_only
    h - hierarchical
    n - noncombinational
    r - removable
    s - synthetic operator
    u - contains unmapped logic
```

Reference	Library	Unit Area	Count	Total Area	Attributes
AND2X1_RVT	saed32rvt_tt1p05v25c	2.033152	1	2.033152	
AND2X2_RVT	saed32rvt_tt1p05v25c	2.287296	1	2.287296	
AO22X1_RVT	saed32rvt_tt1p05v25c	2.541440	128	325.304321	
CtrlModule		19413.298048	1	19413.298048	b, h, n
DpathModule		45479.069757	1	45479.069757	b, h, n
INVX1_RVT	saed32rvt_tt1p05v25c	1.270720	31	39.392320	
NBUFFX2_RVT	saed32rvt_tt1p05v25c	2.033152	113	229.746188	
NBUFFX4_RVT	saed32rvt_tt1p05v25c	2.541440	54	137.237761	
NBUFFX8_RVT	saed32rvt_tt1p05v25c	3.812160	15	57.182400	
NBUFFX16_RVT	saed32rvt_tt1p05v25c	6.099456	6	36.596735	
NOR2X0_RVT	saed32rvt_tt1p05v25c	2.541440	1	2.541440	
NOR2X2_RVT	saed32rvt_tt1p05v25c	2.795584	1	2.795584	
OR2X1_RVT	saed32rvt_tt1p05v25c	2.033152	47	95.558149	
OR2X2_RVT	saed32rvt_tt1p05v25c	2.287296	17	38.884033	

```
Total 14 references                    65861.927185
```

```
******************************************
Design: CtrlModule
******************************************
```

Reference	Library	Unit Area	Count	Total Area	Attributes
AND2X1_RVT	saed32rvt_tt1p05v25c	2.033152	520	1057.239094	
AND2X2_RVT	saed32rvt_tt1p05v25c	2.287296	26	59.469697	
AND2X4_RVT	saed32rvt_tt1p05v25c	2.795584	5	13.977920	
AND3X1_RVT	saed32rvt_tt1p05v25c	2.287296	22	50.320513	
AND3X2_RVT	saed32rvt_tt1p05v25c	2.541440	2	5.082880	
AND4X1_RVT	saed32rvt_tt1p05v25c	2.541440	13	33.038720	
AO21X1_RVT	saed32rvt_tt1p05v25c	2.541440	47	119.447680	
AO21X2_RVT	saed32rvt_tt1p05v25c	2.795584	9	25.160256	
AO22X1_RVT	saed32rvt_tt1p05v25c	2.541440	1118	2841.329931	
AO22X2_RVT	saed32rvt_tt1p05v25c	2.795584	9	25.160256	
AO221X1_RVT	saed32rvt_tt1p05v25c	3.049728	5	15.248640	
AO222X1_RVT	saed32rvt_tt1p05v25c	3.303872	43	142.066501	
AOI21X1_RVT	saed32rvt_tt1p05v25c	3.049728	36	109.790205	
AOI22X1_RVT	saed32rvt_tt1p05v25c	3.049728	91	277.525240	
DFFX1_RVT	saed32rvt_tt1p05v25c	6.607744	985	6508.628054	n
DFFX2_RVT	saed32rvt_tt1p05v25c	7.116032	425	3024.313653	n
HADDX1_RVT	saed32rvt_tt1p05v25c	3.303872	26	85.900675	r
INVX1_RVT	saed32rvt_tt1p05v25c	1.270720	399	507.017282	
...					
SNPS_CLOCK_GATE_HIGH_CtrlModule_24		5.845312	1	5.845312	b, h
SNPS_CLOCK_GATE_HIGH_CtrlModule_25		5.845312	1	5.845312	b, h
SNPS_CLOCK_GATE_HIGH_CtrlModule_26		5.845312	1	5.845312	b, h
SNPS_CLOCK_GATE_HIGH_CtrlModule_27		5.845312	1	5.845312	b, h
XNOR2X1_RVT	saed32rvt_tt1p05v25c	4.320448	72	311.072250	
XOR2X1_RVT	saed32rvt_tt1p05v25c	4.320448	75	324.033594	

```
Total 79 references                    19413.298048
```

RESOURCES

- Synopsys provides implementations of many basic blocks (DesignWare)

- Shows which modules use these components, their parameters, and how the tools decided to optimize them (area, speed, etc)

```
******************************************
Design : CtrlModule
******************************************

Resource Report for this hierarchy in file
        /scratch/cs250-fa14/lab-templates/lab2/build/vlsi/generated-src/Sha3Accel.v
=============================================================================
| Cell           | Module     | Parameters  | Contained Operations        |
=============================================================================
| add_x_1        | DW01_inc   | width=5     | add_1133                    |
| lte_x_2        | DW_cmp     | width=64    | lte_1170                    |
| ash_3          | DW_leftsh  | A_width=4   | sll_1194                    |
|                |            | SH_width=2  |                             |
| sub_x_4        | DW01_dec   | width=2     | sub_1197                    |
...
| eq_x_16        | DW_cmp     | width=64    | eq_1339                     |
| ash_17         | DW_leftsh  | A_width=17  | sll_1345                    |
|                |            | SH_width=5  |                             |
| sub_x_18       | DW01_dec   | width=5     | sub_1347                    |
| ash_20         | DW_leftsh  | A_width=17  | sll_1353                    |
|                |            | SH_width=5  |                             |
| lt_x_21        | DW_cmp     | width=5     | lt_1361                     |
| ash_22         | DW_leftsh  | A_width=17  | sll_1366                    |
|                |            | SH_width=5  |                             |
| lte_x_29       | DW_cmp     | width=5     | lte_1514                    |
...
| add_x_8        | DW01_inc   | width=5     | add_1263 add_1264 add_1355  |
| DP_OP_467_127_5122            |             |                             |
|                | DP_OP_467_127_5122 |      |                             |
=============================================================================

Datapath Report for DP_OP_467_127_5122

=============================================================================
| Cell                | Contained Operations                                |
=============================================================================
| DP_OP_467_127_5122  | add_2072 add_2081                                   |
=============================================================================

=============================================================================
|      |      | Data     |       |                                          |
| Var  | Type | Class    | Width | Expression                               |
=============================================================================
| I1   | PI   | Unsigned | 32    |                                          |
| I2   | PI   | Unsigned | 8     |                                          |
| O1   | PO   | Unsigned | 32    | I1 + I2                                  |
=============================================================================

Implementation Report

=============================================================================
|                    |            | Current           | Set               |
| Cell               | Module     | Implementation    | Implementation    |
=============================================================================
| add_x_1            | DW01_inc   | apparch (area)    |                   |
| lte_x_2            | DW_cmp     | apparch (area)    |                   |
| ash_3              | DW_leftsh  | astr (area)       |                   |
| lt_x_11            | DW_cmp     | pparch (area,speed)|                  |
| ash_20             | DW_leftsh  | astr (area)       |                   |
| lt_x_21            | DW_cmp     | apparch (area)    |                   |
| ash_22             | DW_leftsh  | astr (area)       |                   |
| add_x_50           | DW01_inc   | apparch (area)    |                   |
| add_x_56           | DW01_add   | pparch (area,speed)|                  |
| add_x_7            | DW01_add   | pparch (area,speed)|                  |
| add_x_8            | DW01_inc   | apparch (area)    |                   |
| DP_OP_467_127_5122 | DP_OP_467_127_5122 | str (area,speed)|              |
=============================================================================
```

LAB 2 QUESTIONS?