Quiz/PS 3 Review

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Section 9

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Agenda

- Quiz Review
  - Register Renaming
  - ROB
  - Branch Prediciton
  - Memory in OoO
- Problem Set Questions/Review

Register Renaming

- What are we doing?
  - Mapping Architectural Register to Physical Registers to eliminate WAW and WAR hazards
- Example on board

ROB

- What are we doing?
  - Tracking instructions that have been decoded but not committed
  - Program order is maintained from in-order decode and in-order commit
- Example on board

Branch Prediction

- What are we trying to do?
  - Predict the control flow direction
  - Supserscalar concerns?
    - how do we handle multiple branches per fetch packet
  - Out of order concerns
    - Machine will be bottlenecked by fetch if we don't do a good job
- Example with on board

OoO Memory operations

- What are we trying to do?
    - Allow memory operations to execute out of order
    - What are our constraints?
        - Cannot make store data visible to memory before instruction commits
        - Loads must get the right value
- Example on board

Problem Set Review

Questions