Out of Order and Super Scalar

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Section 8

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Agenda

- Complex Pipelines
 - Hazards
- Out of Order
 - ROB vs Issue Window
 - Speculative store buffer
- Superscalar
 - Renaming
 - Branch Prediction
- Lab 3

Complex Pipeline Hazards

- What are the types of data hazards?
 - Why do we care?
 - Example code?
 - Solutions?
- What else limits our throughput
 - Respecting program-order
 - Inherent ILP of program (max width of CFG)

Reorder Buffer

- Why?
 - cheat sheet so we don't get caught
- What?
 - Tracking info on instructions decoded but not committed yet
- How?

Issue Window

- Why?
 - Can more efficiently use resources
 - Allocation times?
- What?
 - Tracking yet to be issued instructions
- How?

Rollback

- Why?
 - Branch mispredict
 - Exception
- What?
 - Mechanism to return to previous state
- How?
 - What do we want it to look like after rollback
 - Where is the info?

Speculative Memory

- Why?
 - Can't rewrite to memory before commit
- What?
 - Speculative store buffer holds tags, and data
- How
 - Bypass to load if tags match

Superscalar

- Why?
 - ILP in code can be exploited
- What?
 - Fetch, decode, issue, execute, commit multiple instructions per cycle
 - At minimum issue and execute
- How?
 - Many mechanisms

Superscalar Register Renaming

- Why?
 - RAW hazards between consecutive instructions
- What?
 - Parallel read and write ports in rename table during decode
- How?
 - Compare destination and sources

Superscalar Fetch

- Why?
 - Need to feed the beast
 - Out of order machines only work well if they have lots of instructions to schedule
- What?
 - Tight next line prediction coupling with I\$
 - Predict multiple branches per fetch packet
- How?
 - Many ways

Questions?

Lab3

- Experimenting with BOOM
- Directed portion should be straight forward data collection and inference
- Open-ended again split into hw/sw
 - HW+SW: Branch prediction
 - HW: Issue window policy
 - SW: Torture and Parameter introspection
- Chance to finally get chiseling if you want

Paper Handback