EECS 150 Spring 2013 Final Project Proposal

Prof. John Wawrzynek

TAs: Shaoyi Cheng, Vincent Lee Department of Electrical Engineering and Computer Sciences College of Engineering, University of California, Berkeley Due At The Beginning of Lab Section 3/5 or 3/6

Revision 1

1 Project Proposal Document

Now that you have had time to consolidate and think about a you project proposal, you will need to finally put together all of your project proposal elements and your design into a final project proposal. For this document, we ask that you fully elaborate on any and all details of your project which are outlined in the following sections. Your project proposal must be written in understandable English and organized as if you are writing a lab report. Please be comprehensive, yet clear and concise when you are formulating your proposal. Also please do not include links to references or schematics in your proposal.

A hard copy of the report must be submitted at the beginning of your lab section and will later be graded. The TAs will read over your final project proposal and conduct a design review in lab. From here you are responsible for meeting the checkpoint schedule that you propose or that we revise for you. Also by this point, you should have a solid battle plan and begin working on your project if you haven't already. If you don't have a software reference model for your project, we strongly recommend that you find one before continuing to implementation (unless of course it's not relevant).

Your project proposal is required to address the following points:

1.1 Motivation

- The practical problem(s) that you are trying to solve.
- Why should anyone care about you project? Where and/or when would your project be used?
- The high level functional specification of your project. What does will it be able to do when you are done?

1.2 Technical Approach

• The algorithm you are going to use as your reference gold standard.

- A mathematical description of your algorithm or pseudocode.
- If you are implementing a processor system, a complete ISA should go here instead of an algorithm and architectural decisions that you will make or need to implement. You should understand how each of your instructions work and how it flows through your architecture.
- If you are implementing a game in hardware, you should incude a complete set of the rules you will be implementing. This should include aspects such as objective, scoring, and end game. Also you should include the algorithms for any graphics engines that you will be implementing.

1.3 High Level Block Diagrams

- A high level diagram showing all of your peripherals, cores, and functional modules in your system and how they are connected. This includes components such as the resources on the FPGA you will be using (ex. audio port), core generated components such a the Microblaze CPU, and additional modules or accelerators that you will be implementing. This also includes any external devices such as ADCs or microcontrollers that you will interface to the FPGA.
- A description of what each block in the high level diagram does.
- The signal names and data that is being transferred between your high level modules and the purpose that they serve.
- A specification of what parts of the system you will expect from the Xilinx Core Generator and what parts of the system you will be implementing.

1.4 System Block Diagram

- A detailed block diagram for each of the modules that you will be implementing.
- This should show exactly how the registers, ALUs, and memories are connected in your design and how your control and datapath will be abstracted.
- It is recommended that you draw this using a CAD tool such as Microsoft Visio with is available for free from IEEE. The Visio stencils for our class can be found on the course webpage under Resources

1.5 If Time Permits...

- Additional functionality that you will implement if you complete your project early.
- A brief explanation of why adding such a functionality would be useful or enhance your project
- Clearly define what additional hardware you would need and how your high level block diagram changes.
- This can be anything from applying optimization to adding new features.

1.6 If All Else Fails...

- A description of the fall back escape plan in the event that you're in way over your head. This can involve falling back to the MIPS processor design project.
- A description of the absolute minimum functionality that you would consider acceptable for your project or fall back plan.

1.7 Checkpoint Schedule

- The checkpoint by checkpoint schedule of what you expect to accomplish each week. You may space these checkpoints however you would like but no further than 3 weeks apart each. You must on average have one checkpoint scheduled very two weeks. The schedule of your checkpoints must demonstrate reasonable progress towards the end goal.
- The deliverables you will present at each checkpoint date and how you will prove that your design accomplishes the functionality you claim
- We will review your checkpoints to ensure that they are reasonable. If you propose a checkpoint schedule that is too hard, we will try and make it more feasible. If you propose a checkpoint schedule that is too easy, we will make it harder. The stronger projects tend to be more substantial anyways.
- If you don't have a software solution already, you may want to spend the first week developing it as a preliminary checkpoint.
- Remember that the checkpoints are a way for you to convince us that you are making significant progress on your project and are important when we assess your project grade.

2 Design Review

During sections next week, you will be required to meet with the TAs in lab to review your final project proposal. You will turn in your proposals at the beginning of the lab section and we will review your proposals one final time. We will then meet with you and give you feedback on your design, and make sure your checkpoints are reasonable. Make sure you understand your block diagrams and any architectural decisions you made as you may be asked to justify aspects of your design during the review.