

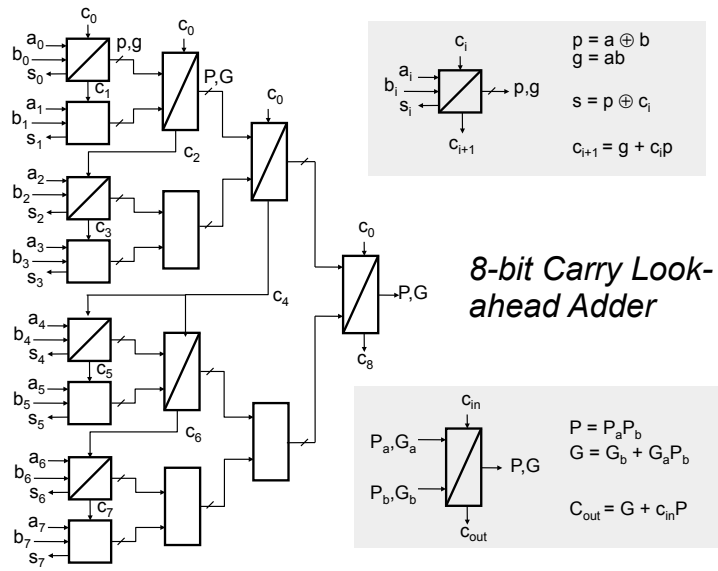
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2013

Homework Assignment 9: FSM, Adders, Multiplier and Shifter
Due April 16th, 2pm

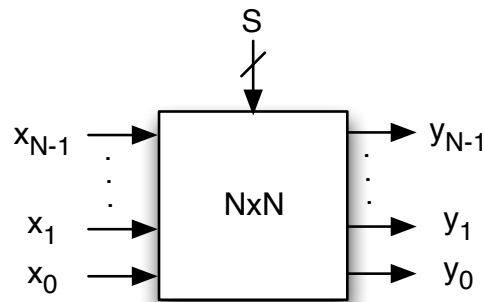
1. You are to design an FSM circuit that has three inputs, clk, reset, and in, and an output, out. Your FSM would detect the sequences 0110 and 0101. The FSM continuously inspects its input and assert out for one cycle when either input sequence has been detected, otherwise it outputs a 0. Sequences can overlap. For instance, the input sequence 010110 will output a pulse for one cycle, and another pulse one cycle after that.
 - (a) Show the state transition diagrams for both the Moore and Mealy implementations of this circuit.
 - (b) For each implementation, show the gate level diagrams of the FSM using one-hot encoding, make sure you include the logic for generating the output as well.

2. The diagram below shows an 8-bit carry-look ahead adder.
 - (a) Highlight the path with the longest delay, circle the starting signal and the ending signal.
 - (b) If you are to implement this circuit with 6LUT, how many LUTs would you need. Assume each 6 LUT has a delay of 1ns, what is the delay of your circuit?



3. Carry-select adders.

- (a) Assuming that the select groups are all of the same number of bits, and the carry delay through a full-adder cell is equal to the delay of a 2-to-1 mux, what is the optimal size select group for a 32-bit adder?
- (b) Consider the possibility of applying the carry-select idea hierarchically. The idea is that a ripple adder of n -bits can be split and implemented as a carry-select adder with group size $n/2$ (implemented as three ripple adders of size $n/2$ along with muxes). Then each of the three adders of size $n/2$ could be split and implemented as a carry-select adder with group size $n/4$, etc. By continuing this process, eventually the adder size would be 1-bit and the process ends. Discuss the worst-case delay through this adder. Again using big O notation, how does the delay scale with n ? How does the cost (amount of hardware - number of gates or transistors) scale with n ?
4. Design an unsigned combinational multiplier (no flip-flops or controller) for multiplying the unsigned constant value 3900 by the variable X ($X_3X_2X_1X_0$). Using only full-adder cells and inverters, draw a circuit that implements the multiplier, minimizing the total amount of hardware and the delay from input to output. **Hint: think about carry-save addition.** What is the total number of FA cells used?
5. A $N \times N$ cross-bar switch is a circuit that can be configured so that each of its N outputs is connected to one of its N inputs:



- (a) Using simple logic gates and multiplexors, draw the internal circuitry for a 2×2 cross-bar switch. Label all inputs and outputs.
- (b) Show how to use the 2×2 switch to design a 4×4 switch
6. Design a controller for a shift-and-add multiplier which works for 2's complement multiplication. Use a Mealy FSM & one-hot encoding. You should first list out the necessary control signals to be generated by your controller and briefly explain what each does to the datapath. Then show your state transition diagram and the gate level circuit for your FSM as well as the output logic.