University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2013

Homework Assignment 8: Timing
Due April 2^{nd}, 2pm

1. Consider a CMOS OR gate implemented as a NOR gate followed by an inverter. Assume the inverter delay is as follows (unit in ps):

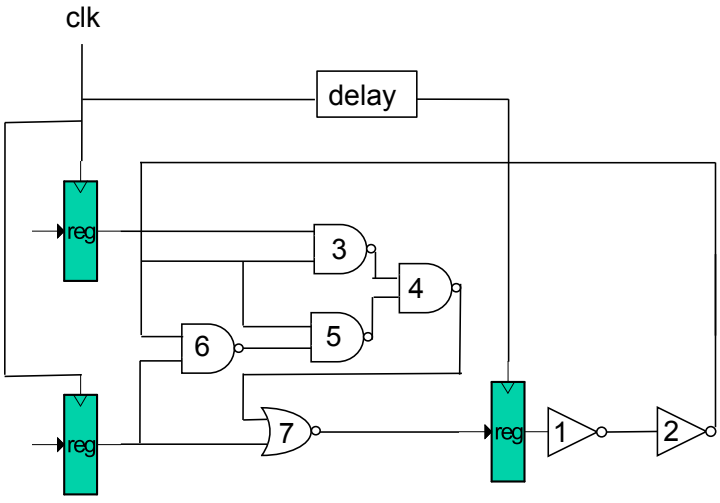
$$\tau_p = 40 + 90f$$

where f is the fanout of the inverter, expressed in number of transistor gate inputs. For instance, an inverter that drives another inverter would have a fanout of 2. You can assume the inverter has the same propagation delay for both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions. The NOR gate propagation delay is expressed as (in ps):

$$\tau_{p0\rightarrow1} = 100 + 125f$$
$$\tau_{p1\rightarrow0} = 100 + 75f$$

For the $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions, respectively, write the expression for the $0 \rightarrow 1$ and $1 \rightarrow 0$ propagation delays of the OR gate.

2. In the circuit below:



• the propagation delay (for both high to low & low to high transitions) of the inverters is $\tau = 50 + 100f$ (in ps)

• the propagation delay (for both kinds of transitions of the NAND and NOR gates are $\tau = 100 + 150f$ (in ps)

• the register has $t_{setup} = t_{clk-q} = 50ps$, $t_{hold} = 50ps$

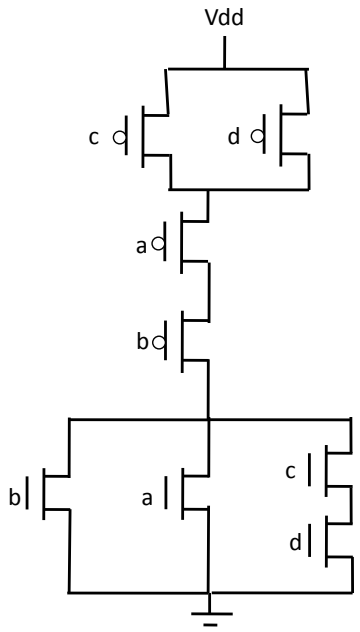
(a) Highlight the critical path, assume the clock skew (the delay block in the diagram) is 0.

(b) List the propagation delay of the gates(by gate number), remember to account for the fanout (expressed in number of transistor gate inputs).

(c) What is the minimum clock period when the clock skew is 0?

(d) Assume we want to run the circuit with a clock period = 3 ns, what is an acceptable range of the clock skew in the circuit? (the delay can be positive or negative)

3. The circuit below has all NMOS being the same size, and PMOS being the same size



when the input to the circuit changes, the output may change as well. For instance when the input pattern $abcd = 0000$ changes to $abcd = 1111$, the output would change from 1 to 0.

(a) Which input pattern change would result in the fastest/slowest $1 \rightarrow 0$ transition at the output?

(b) Which input pattern change would result in the fastest/slowest $0 \rightarrow 1$ transition at the output?

4. Sometimes the hardware designers can increase the throughput of a circuit by adding pipeline registers. The marginal benefit of an additional pipeline stage decreases as more pipeline stages are added (i.e. the improvement is less significant if many pipeline stages are already added). In general, do you think this decrease in marginal return happens more quickly in FPGA or in ASIC? Why?

5. The timing parameters for the circuit below is the same as in question 2, can you get better clock period with register retiming (balancing pipeline stage delay, i.e., shortening the critical path while lengthening the non-critical path)? If you do, show the circuit after the retiming and

calculate the new clock period. If not, briefly explain why. You are not allow to move any logic before reg1 in the process.