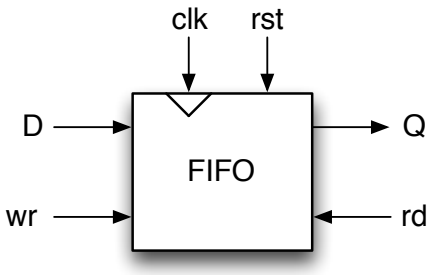
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2013

Homework Assignment 5: Component Interfacing & SRAM
Due March 5^{th}, 2pm

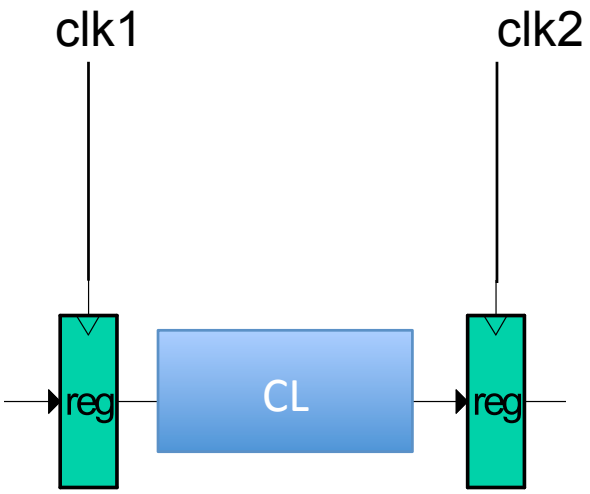
1. Design a 2-entry N-bit wide FIFO (queue) circuit. The circuit has interface signals as shown below. The operation is controlled by the wr and rd signals. The three outputs empty, half, and full, indicate whether the FIFO is empty, half-full, for full, respectively. A read operation when the FIFO is empty results in all zeros on the output. A write operation when the FIFO is full results in no operation. The rst signal is a synchronous control that results in the FIFO being empty.



   Your design should take the form of a data-path and a FSM-based controller. Using flip-flops, simple logic-gates and multiplexors, draw the data-path part of your design. Clearly label all input, output, and control signals (with names of your choice). Use hierarchy.

2. In a system, there are two clock domains, one running at 90MHz and the other running at 100MHz. There is one signal coming out of the 90MHz clock domain, which would be high for one cycle (90MHz cycle) from time to time. We want to capture this event and translate it to a one cycle pulse in the 100MHz clock domain, design a circuit to do that.

3. In the circuit below, clk1 is running at 100MHz, clk2 is running at 75MHz, both registers have $T_{setup} = T_{hold} = 1ns, T_{c2q} = 1.5ns$. Also, it is known the CL block has a delay of $5ns$. Assume at time=0, both clk1 and clk2 are having a rising edge, is there a possibility of flip-flop failure due to metastability? If so, when might that occur? If not, explain why.



4. Consider the organization of a 256K $\times$ 4-bit memory. Assume we desire a square array(same number of rows as columns)

   (a) How many address bits total are required?

   (b) How many of the address bits are used for the row decoder?

   (c) How many of the address bits are used for the column muxing?

   Now assume that we desire this memory to be "configurable", in the sense that with some extra control we could use it as 512K $\times$ 2-bit. Briefly describe what changes would need to be made to the memory block to allow the flexibility.

5. Suppose you are given a collection of configurable memory blocks. Each block can be configured as a 16K $\times$ 1, or a 8K $\times$ 2, ..., 512 $\times$ 32. Your design problem requires a large memory that is 2K X 32. Which collection of smaller memory blocks would you choose? You should attempt to minimize the extra circuitry external to the RAM blocks. Show a block diagram of your design.