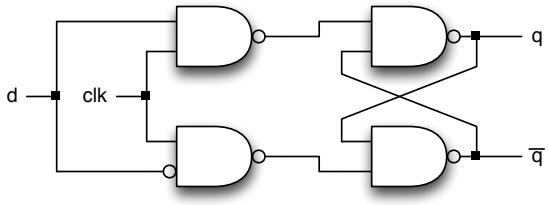
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2013

Homework Assignment 11: Flip-flops Revisited
Due April 30^{th}, 2pm

1. A positive level sensitive latch design is shown below



   (a) Draw a circuit diagram showing how you would use the design principle of this latch as a building block to implement a NEGATIVE edge triggered flip-flop.

   (b) Assume a gate delay of 1ns for inverters and 2ns for NAND gates, what is the setup and clock-to-q times for your flip-flop.

   (c) What is the ratio of transistor counts for your flip-flop versus the standard transmission gate version?

   (d) Show the least expensive modification you could make to your flip-flop circuit to add an asynchronous reset input.

2. Implement a JK flip-flop using D flip-flop and simple gates. Try to minimize the cost.

3. Design a SEC, DED Hamming code for 8 bit data, if during transmission, the 2nd bit is flipped, what would be the check bits produced.