University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2013

Homework Assignment 1: Digital Design Basics, Combinational Logic Review and FPGAs
Due Feb 5^{th}, 2pm

1. Consider the wide range of computer systems in current production, from the embedded controllers in electrical appliances to super-computers in national labs. a) sketch a curve showing performance of all these systems as a function of their cost. Put performance on the y-axis, and cost on the x-axis, using arbitrary units. b) similarly, show a curve that relates performance to system power consumption, with performance on the y-axis, and power consumption on the x-axis. (Your x-axis should span all systems from the lowest cost/power to the highest).

2. After a design is described using HDL, what are the necessary steps for it to become an actual circuit implementation on a FPGA device? What are the input and output for each of the steps?

3. Assume the delay of a gate is d = 2+0.5n, where n is the number of inputs. For each of the following Boolean equations, construct the circuit with the smallest worst case delay. Also compute the delay. (You may use AND, OR, NAND, NOR, XOR, and NOT gates with an arbitrary number of inputs. The available inputs for your circuits are A, B, C, and D).

   (a) $Y = (AC + BC + BD + AD)E$
   (b) $Y = (A + C)B + A(C + B)$
   (c) $Y = (\overline{(AB)} + \overline{C}) + \overline{D}$

4. Implement each of the circuits in question 3 using 2-LUTs, clearly show connection between LUTs and specify the function for each LUT using a truth table for each. Assuming every LUT has a delay of 2ns, what is the delay for each circuit now?

5. Repeat question 4 using 3-LUTs.

6. Find the truth table for equation (c) in question 3.

7. Draw a gate level circuit for a 4-bit adder using NOR gates, and highlight the path with the longest delay. Use hierarchy so you can reuse subcircuits in your design.

8. Show the Sum of Products and Product of Sums forms corresponding to the following truth tables, then simplify them if you can.

(a)

a b	c d	out
00	00	1
00	01	0
00	10	0
00	11	1
01	00	0
01	01	1
01	10	1
01	11	0
10	00	0
10	01	1
10	10	1
10	11	0
11	00	1
11	01	0
11	10	0
11	11	1

(b)

a b	c d	out
00	00	1
00	01	0
00	10	0
00	11	0
01	00	1
01	01	0
01	10	0
01	11	0
10	00	1
10	01	1
10	10	1
10	11	1
11	00	1
11	01	0
11	10	0
11	11	0

(c)

a b	c d	out
00	00	0
00	01	0
00	10	0
00	11	0
01	00	0
01	01	1
01	10	1
01	11	1
10	00	0
10	01	1
10	10	1
10	11	1
11	00	0
11	01	1
11	10	1
11	11	1

9. One-hot encoding is an alternative to binary encoding. For example, in 8-bit one-hot encoding, the number 0 is represented as 00000001, the number 1 is 00000010, 2 is 00000100, 3 is 00001000, ..., 7 is 10000000. It is called "one-hot" because only 1 bit is ever on at a time. Consider a circuit to convert a 2-bit binary numbers to one-hot code. Complete the truth table for the circuit, and construct the circuit using only 2-input gates.

10. A hypothetical LUT has 7 inputs and 2 outputs, it can either be used as one 7-input LUT or two 6-input LUTs, how many different configurations does it have, how many bits would be needed to configure it.

11. Draw a diagram showing how would you construct the LUT in question 10 with 5-LUTs.

12. Prove or disprove the following. A 2-input multiplexor circuit is a universal logic element (in the same sense as a NAND or NOR gate)

13. Implement a one-hot code to binary number converter. This converter takes in 4 bits and output 3 bits. If the input is a legal one-hot code, the lower 2 bits of the output are the corresponding binary number and the 3rd bit is set to 0. If the input is not a legal one-hot code, we do not care about the lower two bits, and the 3rd bit is set to 1. Use Verilog continuous assignment to describe the circuit.